

STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	Voltage Regulator with Watchdog Timer Reset
PRODUCT SERIES	B D 3 0 0 5 H F P
FEATURES	<ol style="list-style-type: none"> 1. High output voltage precision: $5V \pm 2\%$ ($T_a=25^\circ\text{C}$) / Low dropout voltage type / Low quiescent current: $80 \mu\text{A}$. 2. Watchdog Timer inhibit function / Built-in Thermal shutdown circuit / Overcurrent protection circuit / Reverse polarity circuit.

○ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Supply Voltage	Vcc	-15~+50 ※1	V
INH Pin Voltage	VINH	-0.3~+15	V
Regulator Output Pin Voltage	VOUT	-0.3~+15	V
Reset Output Pin Voltage	VRO	-0.3~+15	V
Watchdog Input Pin Voltage	VCLK	-0.3~+15	V
Reset Delay Setting Pin Voltage	VCT	-0.3~+15	V
Power Dissipation	Pd	1.6 ※2	W
Operating Temperature Range	Topr	-40~+125	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	150	°C

※1 Not to exceed Pd.

※2 Reduced by $12.8\text{mW}/^\circ\text{C}$ over $T_a=25^\circ\text{C}$, when mount on a glass epoxy board: $70\text{mm} \times 70\text{mm} \times 1.6\text{mm}$.

○OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	5.5 *	36 **	V
Output Current	Io	—	500	mA

* For the output voltage, consider the voltage dropout arising from the output current.

** Not to exceed Pd.

NOTE) The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

○ELECTRICAL CHARACTERISTICS(Unless otherwise specified, Ta=-40~125°C, VCC=13.5V, Io=200mA)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	Typ	MAX		
[Overall]						
Bias Current 1	Icc1	—	80	130	μA	Io=0mA
Bias Current 2	Icc2	—	80	—	μA	Io=200mA
Bias Current 3	Icc3	—	80	130	μA	VINH=0V, Io=0mA
[Regulator]						
Output Voltage	VOUT	4.90	5.00	5.10	V	
Line Regulation	Line.Reg	—	10	20	mV	Vcc=6.2~25V
Load Regulation	Load.Reg	—	15	30	mV	Io=5~200mA
Dropout Voltage	ΔVd	—	0.78	1.1	V	Vcc=4.75V, Io=200mA
Output Current	Iomax	500	—	—	mA	VOUT=4.9V
Ripple Rejection	R.R.	45	55	—	dB	f=120Hz, ein=1Vrms, Io=200mA
[Reset]						
Detection Voltage	Vdet	4.40	4.50	4.60	V	
Hysteresis Width	VHS	50	100	150	mV	
Output Delay Time L→H	TdLH	12	21	40	ms	CT=0.1 μF ※1
Output Low Voltage	VRST	—	0.2	0.5	V	IRST=2mA
Minimum Operating Voltage	VOPL	1.0	—	—	V	
[Watchdog Timer]						
CT Switching Threshold Voltage High	VthH	1.16	1.26	1.36	V	Vo:ON
CT Switching Threshold Voltage Low	VthL	0.20	0.24	0.28	V	Vo:ON
Discharge Current	Ictc	1	2	3	μA	Vo:ON
Charge Current	Icto	3	6	10	μA	Vo:ON
Watchdog Monitor Time	TWH	32	51	90	ms	CT=0.1 μF ※2
Watchdog Reset Time	TWL	10	17	30	ms	CT=0.1 μF ※3
Clock Pulse Width	TWCLK	500	—	—	ns	
[INH]						
WDT Off Voltage	VUINH	3.2	—	8.0	V	
WDT On Voltage	VLINH	0	—	1.8	V	

※1 TdLH can be varied by changing the CT capacitance value.

$$TdLH(s) \approx (1.26 \times CT(\mu F)) / Icto(\mu A) \quad (\text{Calculation uses Typ. value.})$$

※2 TWH can be varied by changing the CT capacitance value.

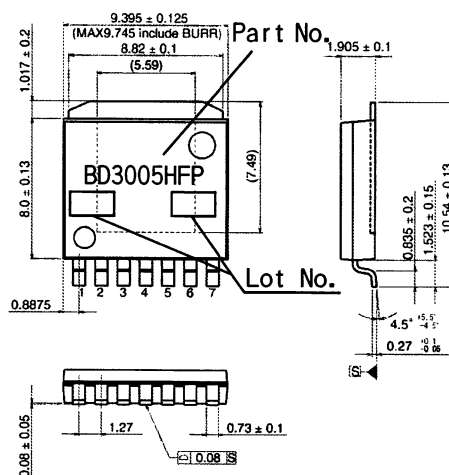
$$TWH(s) \approx (1.02 \times CT(\mu F)) / Ictc(\mu A) \quad (\text{Calculation uses Typ. value.})$$

※3 TWL can be varied by changing the CT capacitance value.

$$TWL(s) \approx (1.02 \times CT(\mu F)) / Icto(\mu A) \quad (\text{Calculation uses Typ. value.})$$

This product is not designed for protection against radio active rays.

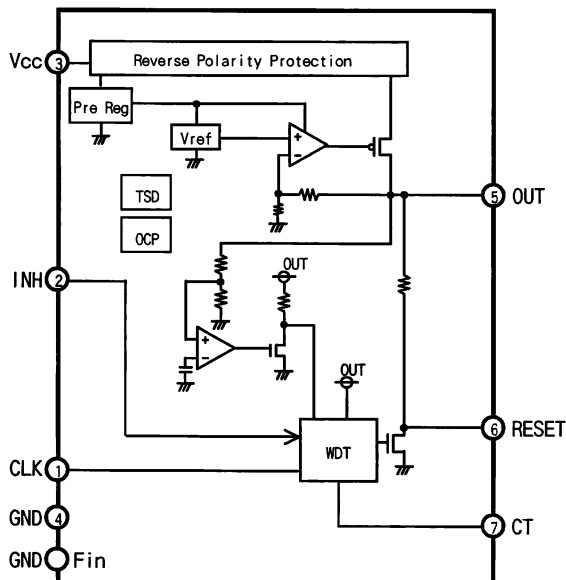
○PHYSICAL DIMENSIONS • MARKING



HRP-7 (Unit : mm)

Rev.C

○BLOCK DIAGRAM



○PIN No. • PIN NAME

Pin No.	Pin Name
1	CLK
2	INH
3	Vcc
4	GND
5	OUT
6	RESET
7	CT
Fin	GND

※Refer to the Technical Note about the details of the application.

○OPERATING NOTES

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake mounting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5) Actions in strong magnetic field

Keep in mind that the IC may malfunction in strong magnetic fields.

6) Testing on application boards

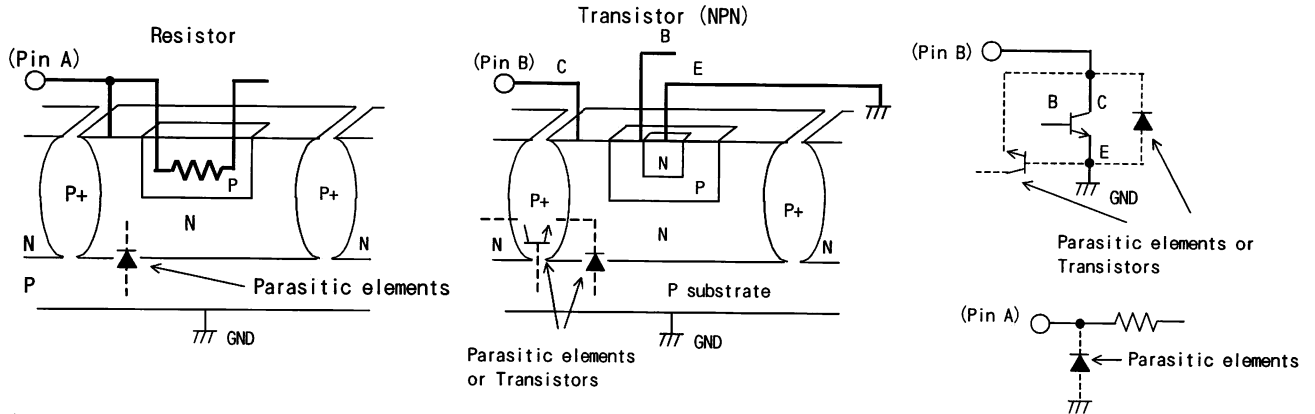
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,

○The P/N junction functions as a parasitic diode when $GND > Pin A$ for the resistor or $GND > Pin B$ for the transistor (NPN).

○Similarly, when $GND > Pin B$ for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.



8) Ground patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation

limits, the attendant rise in the junction temperature (T_j) will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature (T_j) drops. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

10) Overcurrent protection circuit (OCP)

The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

11) Negative surge application to Vcc pin

The IC incorporates a built-in reverse connection breakdown prevention circuit that prevents IC damage even if Vcc carries a lower voltage than the GND pin. However, note that the absolute maximum rating for the negative power supply voltage is $-15V$.

12) Back current flow when the Vcc power supply is suddenly interrupted

These ICs limit generation of back current flow when the Vcc power supply is suddenly interrupted to protect the IC from damage. Sinking current is also limited, making the series compatible with designs where high-capacitance capacitors are used to lengthen the amount of time over which the output voltage can be maintained.

Appendix

Notes

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