# 12-Bit, 20/40/65/80 MSPS, 1.8V Dual Analog-to-Digital Converter

Preliminary Technical Data

# AD9231

## FEATURES

**1.8 V analog supply operation**
**1.8 V to 3.3 V output supply**
**SNR = 70 dBFs up to 170 MHz input**
**SFDR = 85 dBc up to 70 MHz input**
**Low ADC Core power:**
**33 mW/ch @ 20MSPS**
**73 mW/ch @ 80MSPS**
**Differential input with 650 MHz bandwidth**
**On-chip voltage reference and sample-and-hold amplifier**
**DNL = ±0.5 LSB**
**Flexible analog input: 1 V p-p or 2 V p-p differential**
**Offset binary, Gray code, or twos complement data format**
**Clock duty cycle stabilizer**
**Programmable Clock Divider**
**Data output clock**
**Serial port control**
**Built-in selectable digital test pattern generation**
**Programmable clock and data alignment**

## APPLICATIONS

**IF sampling and direct conversion in communications receivers: 3G, 4G, TDS-CDMA, CDMA2000, LTE, Wimax**
**Test and measurement portable instruments**
**Hand-held scope meters**
**Automotive Radar**

## GENERAL DESCRIPTION

The AD9231 is a monolithic, dual channel 1.8 V supply, 12-bit, 20/40/65/80 MSPS analog-to-digital converter (ADC), featuring a high performance sample-and-hold circuit and on-chip voltage reference. The product uses a multi-stage differential pipeline architecture with output error correction logic to provide 12-bit accuracy at 80 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input controls all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

## FUNCTIONAL BLOCK DIAGRAM

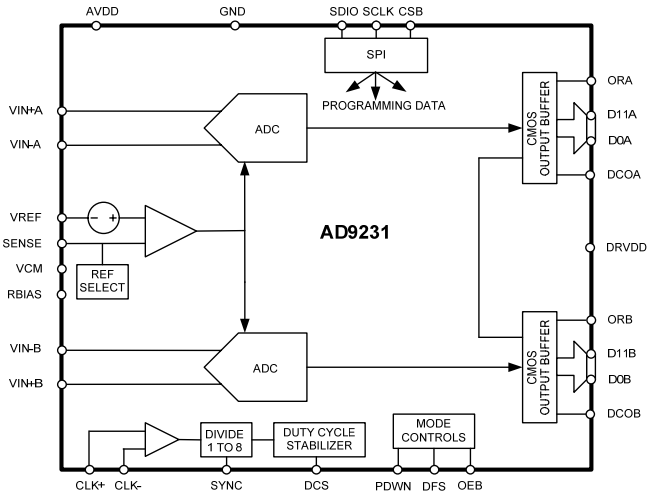


*Figure 1.*

The digital output data is available in Offset Binary, Gray Code, or Twos Complement formats. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic.

The AD9231 is available in a 64-lead Pb-free LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

## PRODUCT HIGHLIGHTS

1. The AD9231 operates from a single 1.8 V power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The patented sample and hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power and ease of use.
3. The clock Duty Cycle Stabilizer (DCS) maintains overall ADC performance over a wide range of clock pulse widths.
4. A standard serial port interface (SPI) supports various product features and functions, such as data formatting (offset binary, twos complement, or Gray coding), enabling the clock DCS, power-down, and voltage reference mode.
5. The AD9231 is pin compatible with the 10bit AD9204 and 14bit AD9251, allowing for a simple migration between 10 bits and 14 bits.

**Rev. PrC**
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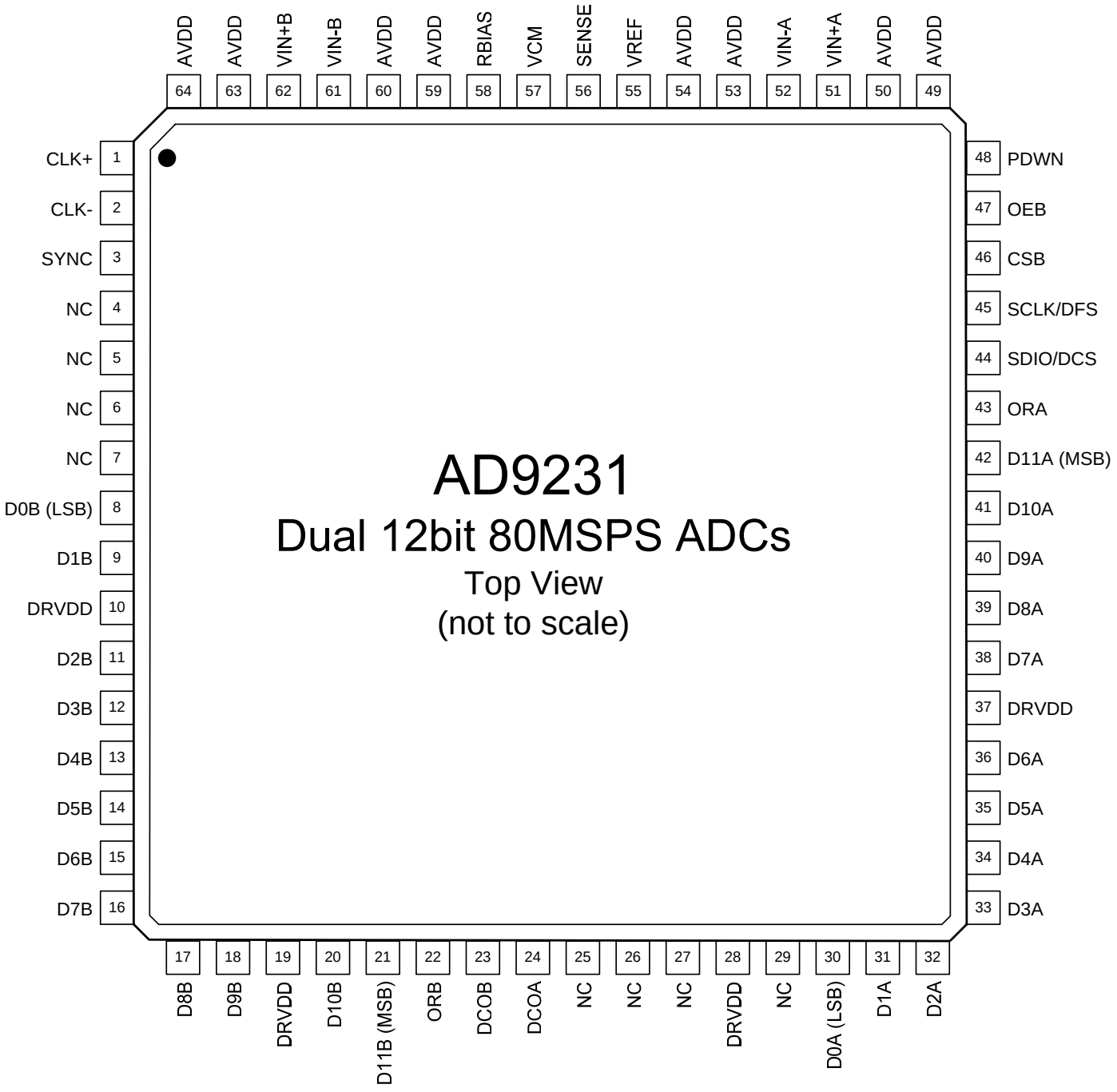


*Figure 2. Device Pin Map*



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| Pin # | Name | Description |
|---|---|---|
| 0 | GND | Exposed paddle is the only ground connection for the chip. Must be connected to PCB AGND. |
| 49, 50, 53, 54, 59, 60, 63, 64 | AVDD | 1.8V Analog supply pins. |
| 10, 19, 28, 37 | DRVDD | Digital Output Driver Supply (1.8V to 3.3V) |
| 51, 52 | AINA+/- | Channel "A" analog inputs. |
| 62, 61 | AINB+/- | Channel "B" analog inputs. |
| 1, 2 | CLK+, CLK- | Differential encode clock; PECL, LVDS or 1.8V CMOS inputs. |
| 58 | RBIAS | Sets analog current bias. Connect to 10kohm (1% tolerance) resistor to ground. |
| 57 | VCM | Analog output voltage at mid supply to set common mode of the analog inputs. |
| 56 | SENSE | Reference Mode Selection |
| 55 | VREF | Voltage Reference Input/Output |
| 46 | CSB | SPI chip select; active low enable. 50Kohm internal pullup. |
| 45 | SCLK/DFS | SPI clock. Static control of data output format, DFS, if not in SPI mode.<br>If "high": twos complement.<br>If "low": offset binary.<br>50Kohm internal pulldown. |
| 44 | SDIO/DCS | SPI data in/out. Static enable for Duty Cycle Stabilizer if not in SPI mode. 50Kohm internal pulldown in SPI mode. 50Kohm internal pullup in non-SPI mode. |
| 3 | SYNC | Digital input. SYNC input to clock divider. 50Kohm internal pulldown. |
| 47 | OEB | Digital input. Enable channel "A" & "B" digital outputs if "low"; tri-state outputs if "high". 50Kohm internal pulldown. |
| 48 | PDWN | Digital input. Powerdown chip if "high". 50Kohm internal pulldown. |
| 8-9, 11-18, 20, 21 | D0B-D11B | Channel B digital outputs. D11B = MSB |
| 30-36, 38-42 | D0A-D11A | Channel A digital outputs. D11A = MSB |
| 22 | ORB | Channel B Out-of-Range digital output. |
| 43 | ORA | Channel A Out-of-Range digital output. |
| 23 | DCOB | Channel B Data Clock digital output. |
| 24 | DCOA | Channel A Data Clock digital output. |
| 4-7, 25-27, 29 | DNC | Do Not Connect |



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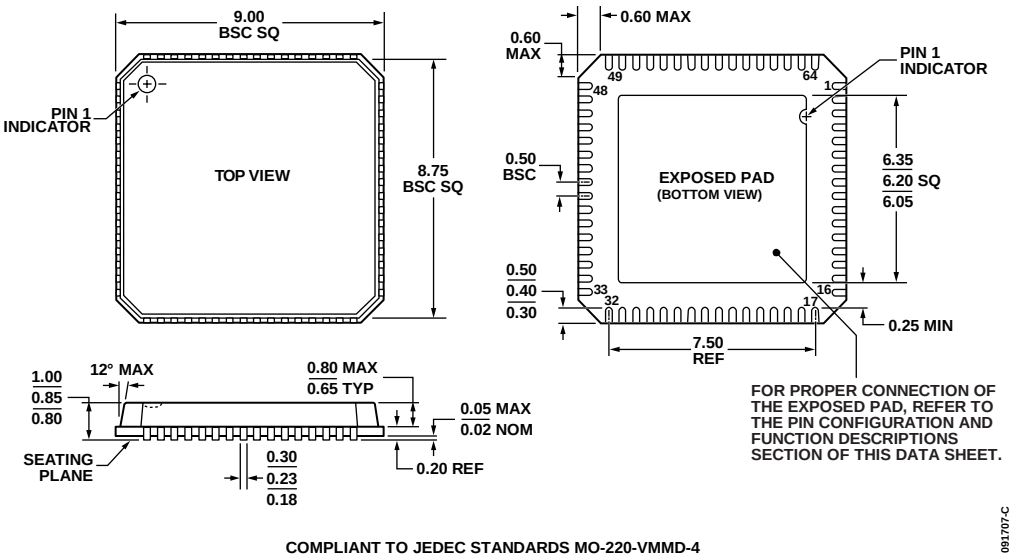
# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

*Figure 3. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*9 mm × 9 mm Body, Very Thin Quad (CP-64-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9231BCPZ-80[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZRL7–80[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZ-65[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZRL7–65[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZ-40[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZRL7–40[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZ-20[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231BCPZRL7–20[1,2] | –40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9231Z-80EB[1] | | Evaluation Board | |
| AD9231Z-65EB[1] | | Evaluation Board | |
| AD9231Z-40EB[1] | | Evaluation Board | |
| AD9231Z-20EB[1] | | Evaluation Board | |

[1] Z = Pb-free part.
[2] The exposed paddle is the only GND connection on the chip and must be connected to the PCB AGND.

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