PRELIMINARY

14-CHARACTER 2-LINE DOT MATRIX LCD CONTROLLER DRIVER WITH SMOOTH SCROLL FUNCTION

■ GENERAL DESCRIPTION

The NJU6520 is a Dot Matrix LCD controller driver for 14-character 2-line with icon display in single chip.

It contains voltage tripler, bleeder resistor, CR oscillator, serial interface circuit, instruction decoder controller, character generator ROM/RAM, high voltage operating common and segment drivers.

The internal voltage converter generates high voltage (about 8V) from the voltage supply voltage(3V) for high contrast LCD. The contrast control function realizes 16 steps V_{LCD} adjustable by the internal Electrical Voltage Resistor.

The CR oscillator incorporates C and R, therefore no external components for oscillation are required.

The serial interface circuits which operate by 1MHz, can be connected directly to serial port of the microprocessor.

The character generator consists of 7,680 bits ROM and 64 x 6 bits RAM.

The 18-common (16 for character, 2 for icon) and 84-segment drives up to 14-character 2-line, and the icon common driver display up to 84-icon display.

As an outstanding feature, NJU6520 realizes the horizontal smooth scroll of characters by combination of instructions.

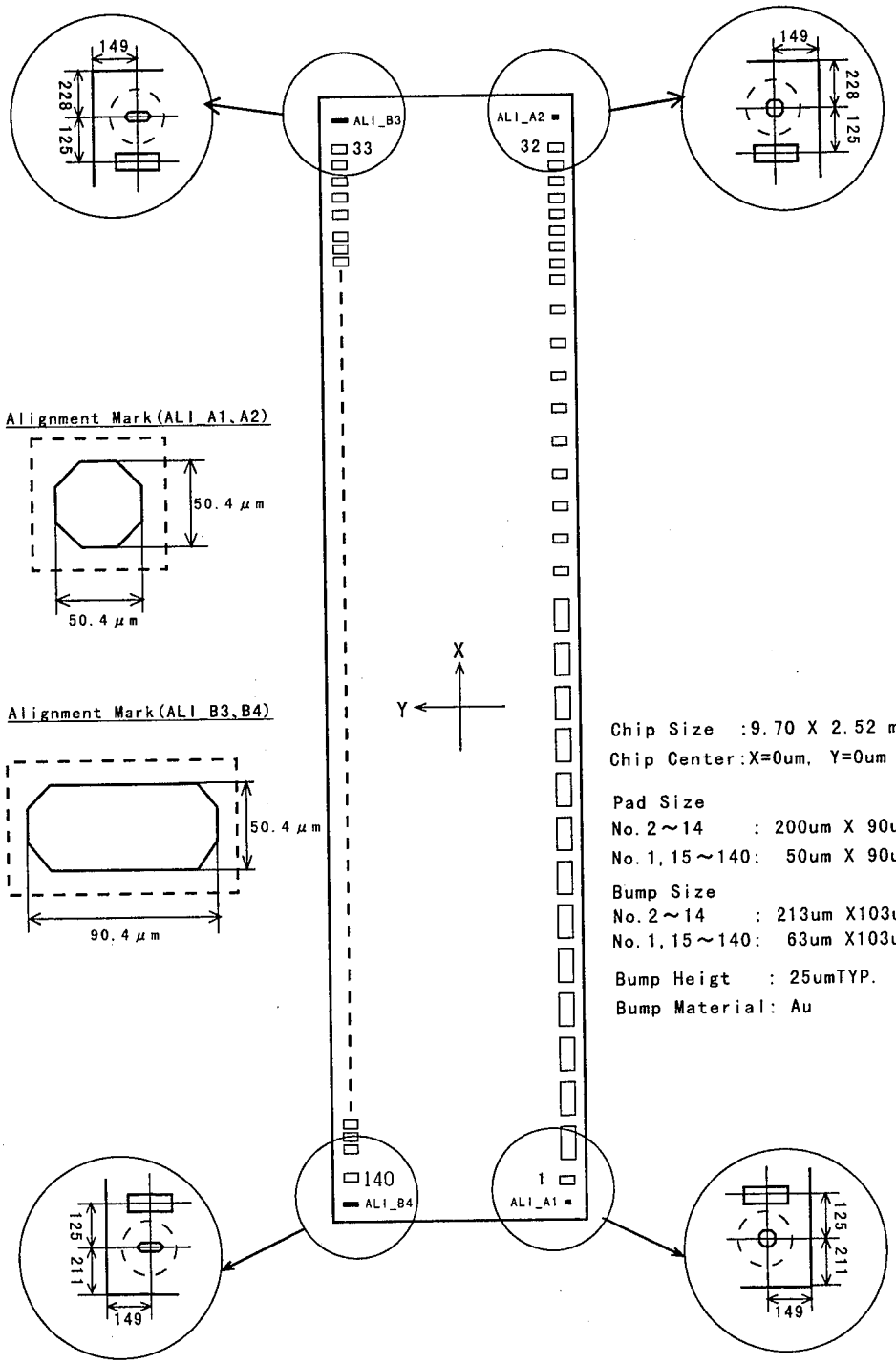
■ PACKAGE OUTLINE

NJU6520CH

■ FEATURES

- 14-character 2-line Dot Matrix LCD Controller Driver
- Maximum 84-icon Display
- Serial Interface
- Display Data RAM - 30 x 8 bits : Maximum 14-character 2-line Display
- Character Generator ROM - 7,680 bits : 192 Characters (5 x 7 Dots)
- Character Generator RAM - 64 x 6 bits : 8 Patterns (6 x 8 Dots)
- Icon Display RAM - 14 x 6 bits : 84-icons display
- High Voltage LCD Driver : 18-common / 84-segment
- Duty Ratio : 1/18 or 1/9 Duty by instruction
- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Control, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift, Dot Shift
- Power On Initialize / Hardware Reset Function
- Electrical Variable Resistor On-chip
- Oscillation Circuit On-chip
- Voltage Tripler and bleeder Resistor On-chip
- Low Power Consumption
- Operating Voltage --- 2.4 to 3.6 V (Except LCD Driving Voltage)
- Package Outline --- Bump-Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Size :9.70 X 2.52 mm
Chip Center:X=0um, Y=0um

Pad Size
No.2～14 : 200um X 90um
No.1,15～140: 50um X 90um

Bump Size
No.2～14 : 213um X103um
No.1,15～140: 63um X103um

Bump Heigt : 25umTYP.
Bump Material: Au

■ TERMINAL DESCRIPTION

CHIP SIZE 9.70 × 2.52mm(Chip Center X=0μm, Y=0μm)

PAD No.	PAD NAME	X=(μm)	Y=(μm)
1	DUMMY1	-4514	-1111
2	V_1	-4236	-1111
3	V_2	-3831	-1111
4	V_3	-3397	-1111
5	V_4	-2992	-1111
6	V_5	-2562	-1111
7	VR	-2230	-1111
8	V_{SS}	-1799	-1111
9	V_{5OUT}	-1467	-1111
10	C_2^-	-1134	-1111
11	C_2^+	-730	-1111
12	C_1^-	-299	-1111
13	C_1^+	106	-1111
14	V_{DD}	536	-1111
15	OSC_1	833	-1111
16	OSC_2	1087	-1111
17	TEST	1370	-1111
18	SIO	1625	-1111
19	SCL	1908	-1111
20	$\overline{CS}$	2163	-1111
21	R/W	2454	-1111
22	RS	2709	-1111
23	$\overline{RESET}$	3000	-1111
24	DUMMY2	3217	-1111
25	DUMMY3	3377	-1111
26	DUMMY4	3537	-1111
27	DUMMY5	3697	-1111
28	DUMMY6	3857	-1111
29	DUMMY7	4017	-1111
30	DUMMY8	4177	-1111
31	DUMMY9	4337	-1111
32	DUMMY10	4497	-1111
33	DUMMY11	4497	1111
34	DUMMY12	4337	1111
35	DUMMY13	4177	1111
36	DUMMY14	4017	1111
37	DUMMY15	3857	1111
38	$COMMK_1$	3685	1111
39	COM_1	3605	1111
40	COM_2	3525	1111
41	COM_3	3445	1111
42	COM_4	3365	1111
43	COM_5	3285	1111
44	COM_6	3205	1111
45	COM_7	3125	1111
46	COM_8	3045	1111
47	SEG_1	2965	1111
48	SEG_2	2885	1111
49	SEG_3	2805	1111
50	SEG_4	2725	1111

PAD No.	PAD NAME	X=(μm)	Y=(μm)
51	SEG_5	2645	1111
52	SEG_6	2565	1111
53	SEG_7	2485	1111
54	SEG_8	2405	1111
55	SEG_9	2325	1111
56	SEG_{10}	2245	1111
57	SEG_{11}	2165	1111
58	SEG_{12}	2085	1111
59	SEG_{13}	2005	1111
60	SEG_{14}	1925	1111
61	SEG_{15}	1845	1111
62	SEG_{16}	1765	1111
63	SEG_{17}	1685	1111
64	SEG_{18}	1605	1111
65	SEG_{19}	1525	1111
66	SEG_{20}	1445	1111
67	SEG_{21}	1365	1111
68	SEG_{22}	1285	1111
69	SEG_{23}	1205	1111
70	SEG_{24}	1125	1111
71	SEG_{25}	1045	1111
72	SEG_{26}	965	1111
73	SEG_{27}	885	1111
74	SEG_{28}	805	1111
75	SEG_{29}	725	1111
76	SEG_{30}	645	1111
77	SEG_{31}	565	1111
78	SEG_{32}	485	1111
79	SEG_{33}	405	1111
80	SEG_{34}	325	1111
81	SEG_{35}	245	1111
82	SEG_{36}	165	1111
83	SEG_{37}	85	1111
84	SEG_{38}	5	1111
85	SEG_{39}	-75	1111
86	SEG_{40}	-155	1111
87	SEG_{41}	-235	1111
88	SEG_{42}	-315	1111
89	SEG_{43}	-395	1111
90	SEG_{44}	-475	1111
91	SEG_{45}	-555	1111
92	SEG_{46}	-635	1111
93	SEG_{47}	-715	1111
94	SEG_{48}	-795	1111
95	SEG_{49}	-875	1111
96	SEG_{50}	-955	1111
97	SEG_{51}	-1035	1111
98	SEG_{52}	-1115	1111
99	SEG_{53}	-1195	1111
100	SEG_{54}	-1275	1111

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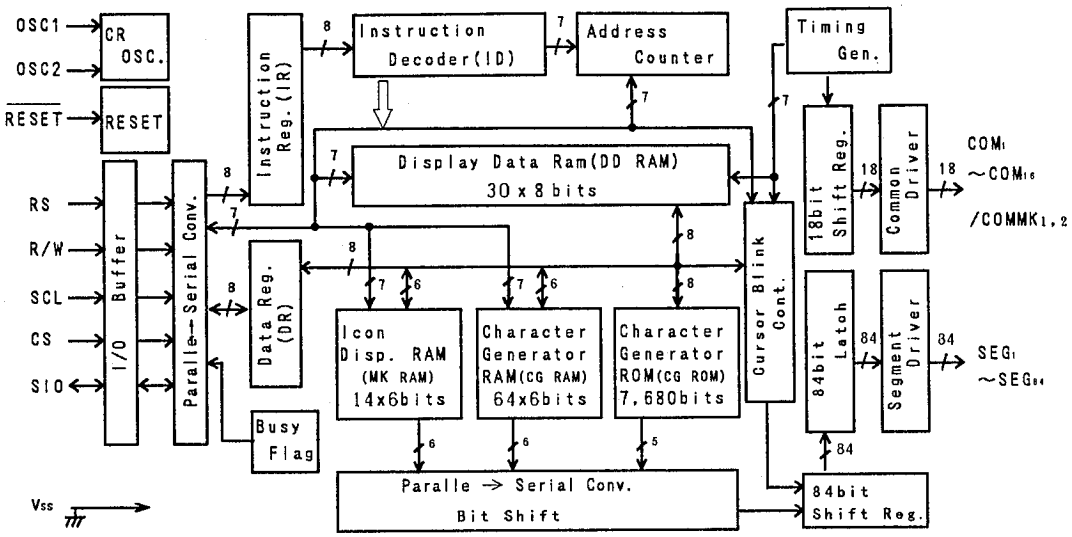
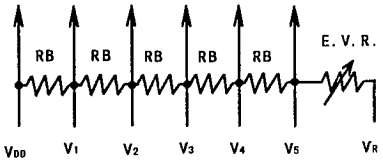
PAD No.	PAD NAME	X=(μm)	Y=(μm)
101	SEG_{55}	-1355	1111
102	SEG_{56}	-1435	1111
103	SEG_{57}	-1515	1111
104	SEG_{58}	-1595	1111
105	SEG_{59}	-1675	1111
106	SEG_{60}	-1755	1111
107	SEG_{61}	-1835	1111
108	SEG_{62}	-1915	1111
109	SEG_{63}	-1995	1111
110	SEG_{64}	-2075	1111
111	SEG_{65}	-2155	1111
112	SEG_{66}	-2235	1111
113	SEG_{67}	-2315	1111
114	SEG_{68}	-2395	1111
115	SEG_{69}	-2475	1111
116	SEG_{70}	-2555	1111
117	SEG_{71}	-2635	1111
118	SEG_{72}	-2715	1111
119	SEG_{73}	-2795	1111
120	SEG_{74}	-2875	1111
121	SEG_{75}	-2955	1111
122	SEG_{76}	-3035	1111

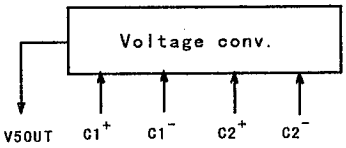
PAD No.	PAD NAME	X=(μm)	Y=(μm)
123	SEG_{77}	-3115	1111
124	SEG_{78}	-3195	1111
125	SEG_{79}	-3275	1111
126	SEG_{80}	-3355	1111
127	SEG_{81}	-3435	1111
128	SEG_{82}	-3515	1111
129	SEG_{83}	-3595	1111
130	SEG_{84}	-3675	1111
131	$COMMK_2$	-3755	1111
132	COM_{16}	-3835	1111
133	COM_{15}	-3915	1111
134	COM_{14}	-3995	1111
135	COM_{13}	-4075	1111
136	COM_{12}	-4155	1111
137	COM_{11}	-4235	1111
138	COM_{10}	-4315	1111
139	COM_9	-4395	1111
140	DUMMY16	-4514	1111
Alignment Mark	ALI_A1	-4639	-1111
Alignment Mark	ALI_A2	4622	-1111
Alignment Mark	ALI_B3	4622	1111
Alignment Mark	ALI_B4	-4639	1111

5

■ BLOCK DIAGRAM







- Internal Bleeder Resistors(RB)
  RB(10 kΩ) × 5 = 50 kΩ typ.

- Electrical Variable Resistor(E.V.R)
  E.V.R. $(00)_H$ (DB_3, DB_2, DB_1, DB_0 = 0,0,0,0) = 0 Ω typ.
  E.V.R. $(FF)_H$ (DB_3, DB_2, DB_1, DB_0 = 1,1,1,1) = 25 kΩ typ.

■ TERMINAL DESCRIPTION

PAD No.	SYMBOL	I/O	F U N C T I O N
14 8	V_{DD} V_{SS}	— —	Power Source V_{DD}=+3V , V_{SS}=0V
2～6	V_1～V_5	I	LCD Driving Voltage Terminals.
15 16	OSC_1 OSC_2	I O	Oscillation Frequency Adjust Terminals. Normally open. (Oscillation C and R are incorporated, f_{OSC}=125kHz) For external clock operation, the clock should be input on OSC_1.
18	SIO	I/O	Serial Data I/O Terminal.
19	SCL	I	Shift Clock Input Terminal
20	$\overline{CS}$	I	Chip Select Signal Input Terminal
21	R/W	I	Read/Write Selection Signal Input Terminal. (Pull-up) "0" : Write , "1" : Read
22	RS	I	Register Selection Signal Input Terminal. (Pull-up) "0" : Instruction Register (Writing) Busy Flag, Address Counter (Reading) "1" : Data Register (Writing / Reading)
39～46 139～132	COM_1～COM_8 COM_9～COM_{16}	O	LCD Common Driving Signal output terminals.
38 131	COMMK1 COMMK2	O	Icon Display Common Driving Signal output terminals.
47～130	SEG_1～SEG_{84}	O	LCD Segment Driving Signal output terminals.
13、12 11、10	$C1^+$, $C1^-$ $C2^+$, $C2^-$	I/O	Step up voltage capacitor connecting terminals. In case of tripler operation, connect the capacitor between C_1^+ and C_1^-, C_2^+ and C_2^-. In case of doubler operation, connect the capacitor between C_2^+ and C_2^-, connect C_2^+ to C_1^+, and C_1^- should be open.
9	V_{5OUT}	O	Step up voltage output terminal.
7	VR	I	E.V.R. Terminal. The contrast control is practiced by E.V.R. between V_5 and VR terminal.
23	$\overline{RESET}$	I	Reset Terminal. When "L" level over than 1.2ms inputs to this terminal, the system will be reset (f_{OSC}=125kHz).
17	TEST	O	Maker testing terminal. Normally Open.
1 24～37 140	DUMMY1 DUMMY2～15 DUMMY16	-	Dummy terminal. Normally Open.

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■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Register

The NJU6520 incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift", and address data for Display Data RAM(DD RAM), Character Generator RAM (CG RAM) and Icon Display RAM(MK RAM).

The MPU can write the instruction code and address data to the Register (IR), but it cannot read out from the Register(IR).

The Register(DR) is a temporary stored register, the data stored in the Register (DR) is written into the DD RAM, CG RAM or MK RAM and read out from the DD RAM, CG RAM or MK RAM. The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation. When the address data for the DD RAM, CG RAM or MK RAM is written into the Register (IR), the addressed data in the DD RAM, CG RAM or MK RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely. After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM, CG RAM or MK RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below.

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter(DB_0～DB_6)
1	0	DR	Write (Register(DR) to DD RAM, CG RAM or MK RAM)
1	1		Read (DD RAM, CG RAM or MK RAM to Register(DR))

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(1-2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag (BF) is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in Table 1.

The next instruction should be written after the busy flag(BF) goes to "0".

(1-3) Address Counter (AC)

The address counter(AC) addressing the DD RAM, CG RAM and MK RAM.

When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.

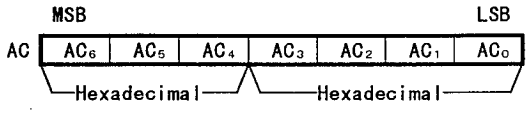
After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter (AC) increments (or decrements) automatically.

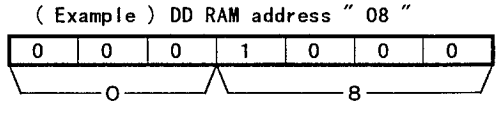
The address data in the Counter(AC) is output from DB_6～DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1-4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 30 x 8 bits stores up to 30-character display data represented in 8-bit code. (2 out of the 30characters are used for scroll RAM.)

The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.





・2-line display

	1ch.	2	3	4	5	6	7	8	9	10	11	12	13	14	
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

← Display Position

← DD RAM address (Hex.)

Scroll RAM

When the display shift is performed, the DD RAM address changes as follows:

(1st line Left Shift Display)

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	00
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

(1st and 2nd line Left Shift Display)

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	00
11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	10

(1st line Right Shift Display)

0E	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

(1st and 2nd line Right Shift Display)

0E	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D
1E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D

(1-5) Character Generator ROM (CG ROM)

The Character Generator ROM(CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.

The storage capacity is up to 192 kinds of 5 x 7 dots character pattern.

The correspondence between character code and standard character pattern of NJU6520 is shown in Table 2.

User-defined character patterns (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version -01)

Lower 4 bit (HEX.) \ Upper 4 bit (HEX.)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(05)															
5	(06)															
6	(07)															
7	(08)															
8	(01)															
9	(02)															
A	(03)															
B	(04)															
C	(05)															
D	(06)															
E	(07)															
F	(08)															

Character code $(1X)_H$, $(8X)_H$, $(9X)_H$ don't exist.

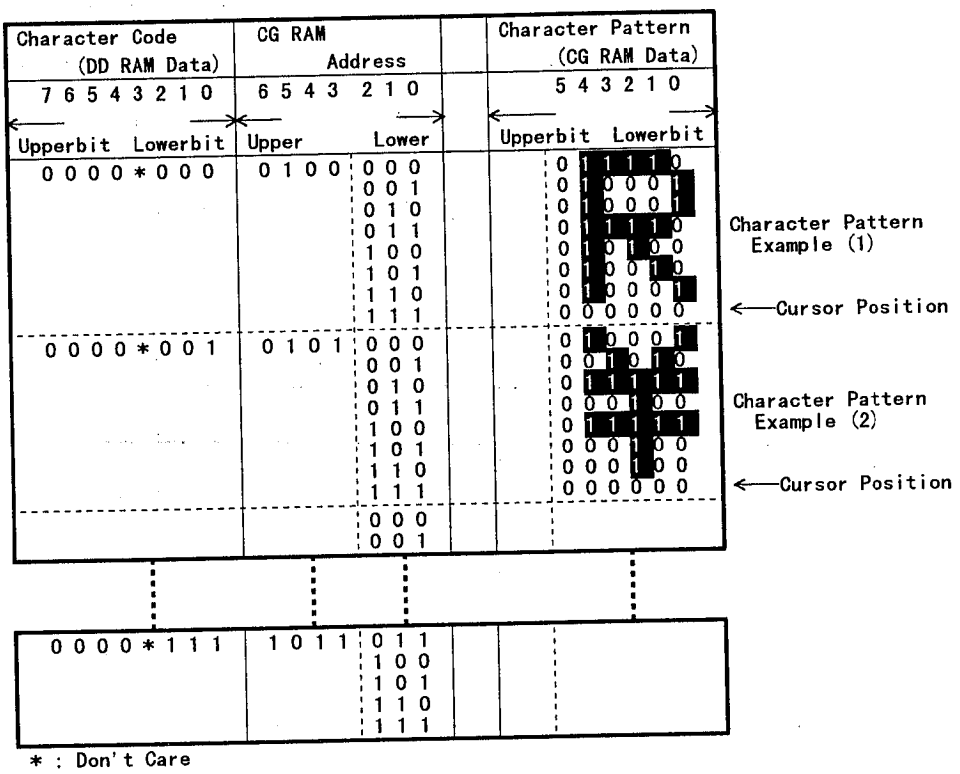
(1-6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 6 x 8 dots written by the user program to display user's original character pattern. The CG RAM can store 8 kinds of character in 6 x 8 dot.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(07)_H$ or $(08)_H$ - $(0F)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(6 x 8 dots).



* : Don't Care

NOTE 1. Character code bit 0, 1, 2 correspond to the CG RAM address 3, 4, 5, 6 (4bits:8 patterns).

2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0".
   If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 5 are shown above.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 and 1. Therefore, the address $(00)_H$ and $(08)_H$ select the same character pattern as shown in Table 2.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-7) Icon Display RAM (MK RAM)

The NJU6520 can display maximum 84-icon display.

The icon display is controlled by writing data to MK RAM.

Correspondence between MK RAM and icon display position is shown as the following fig.1 and table3.

fig.1 Icon display example

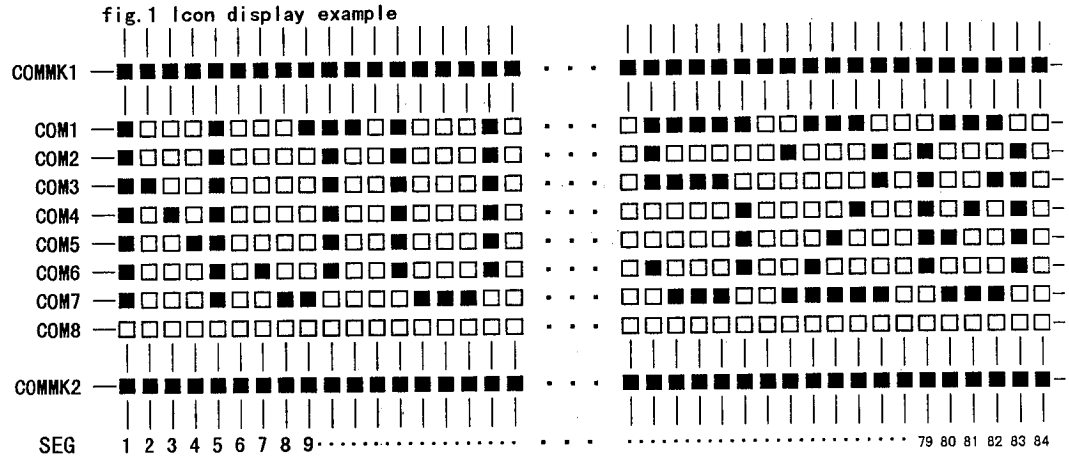


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table3 Correspondence between MK RAM and icon display position.

MK RAM address (60_H～$6D_H$)		Icon display position (SEGn)							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0110 0000	60_H	*	*	1	2	3	4	5	6
0110 0001	61_H	*	*	7	8	9	10	11	12
0110 0010	62_H	*	*	13	14	15	16	17	18
0110 0011	63_H	*	*	19	20	21	22	23	24
0110 0100	64_H	*	*	25	26	27	28	29	30
:	:	:							
0110 1010	$6A_H$	*	*	61	62	63	64	65	66
0110 1011	$6B_H$	*	*	67	68	69	70	71	72
0110 1100	$6C_H$	*	*	73	74	75	76	77	78
0110 1101	$6D_H$	*	*	79	80	81	82	83	84

NOTE 1. When using the icon display function, write all "0" data to MK RAM before the display ON instruction.

2. The icon display don't shift by the display shift instruction.

3. 2 icons, which intersect on the COMMK1, COMMK2 and 1line-segment, correspond to same MK RAM address. According to LCD design, 2 icons are displayed at the same time.

(1-8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, MK RAM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-9) LCD Driver

LCD driver consist of 18-common driver and 84-segment driver.

When the line number is selected by a program, the required common drivers output the common driving waveform and the other common drivers output non-selection waveform automatically.

The 84 bits of character pattern data are shifted in the shift-register and latched when the 84 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1-10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	1	0	0	0

2 line Display

	1桁	2	3	4	5	6	7	8	9	10	11	12	13	14	←Display position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	←DD RAM address (Hexadecimal)
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	

Cursor position

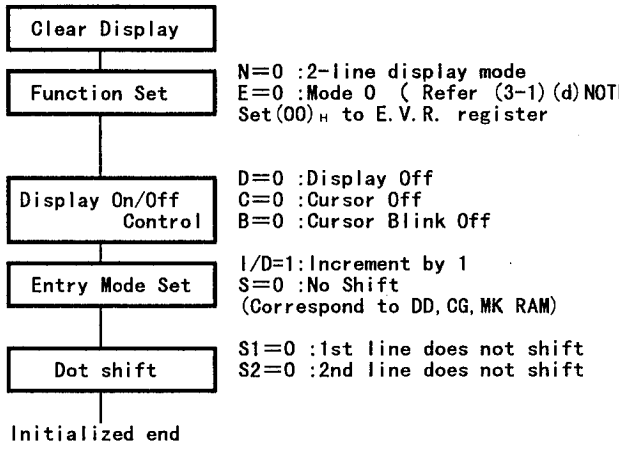
Note: The cursor or blinks also appear when the address counter (AC) selects the CG RAM. But the displayed cursor and blink are meaningless.
Cursor Blinking display is dependence under 5bit in address counter (AC)

(2) Power on Initialization by internal circuits

(2-1) Initialization By Internal Reset Circuits

The NJU6520 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 2.4V.

Initialization flow is shown below:



NOTE

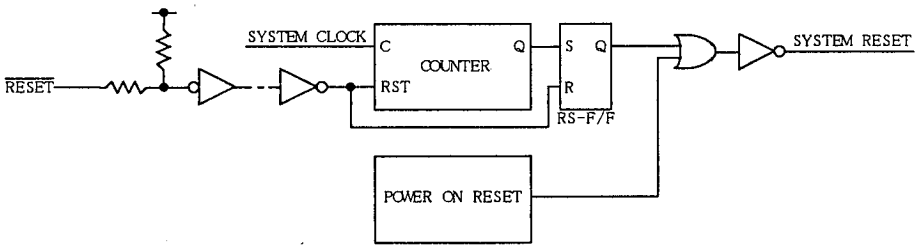
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

5

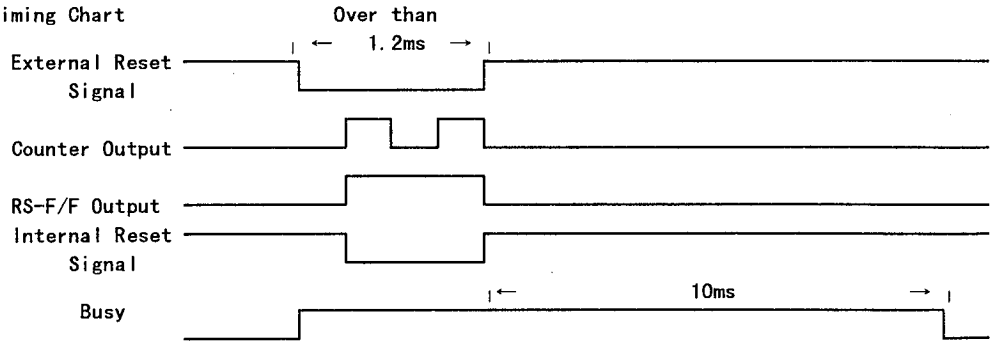
(2-2) Initialization By Hardware

The NJU6520 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over than 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

• Reset Circuit



• Timing Chart



(3) Instructions

The NJU6520 incorporates two registers, an Instruction Register(IR) and a Data Register (DR).

These two registers store control information temporarily to allow interface between NJU6520 and MPU or peripheral ICs operating different cycles. The operation of NJU6520 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data I/O signals (DB_0 to DB_7 by SIO terminal).

Table 4. shows each Instruction and its operating time

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DESCRIPTION	EXEC TIME
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	-
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address "0" in AC.	1.585 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address "0" in AC and returns display being shifted to original position. DD RAM contents remain unchanged	97us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift(NOTE2)	97us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	97us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	Shift line		Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left Lower 2bits determine shift-line	146us
Dot Shift	0	0	0	0	1	S2	S1	←Number→ of dot-shift			S2 : 2nd line S1 : 1st line Lower 3bits set the number of dot-shift.	97us
Function Set	0	0	0	1	N	E	←	E.V.R. value	→		N : Set 1-line display mode E=1 : mode 1, E=0 : mode 0 (NOTE2) Lower 4bits set E.V.R. register for the contrast control	97us
RAM Address Set	0	0	1	←—	—	Address			—→		Sets DD RAM, CG RAM and MK RAM address.	97us
Read Busy Flag & Address	0	1	BF	←—	—	AC			—→		Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
Write Data to CG & DD RAM	1	0	←— Write Data (DD RAM) —→								Writes data into DD, CG or MK RAMs	97us
	1	0	*	*	←—	Write Data (CG RAM)			—→			
	1	0	*	*	←—	Write Data (MK RAM)			—→			
Read Data from CG or DD RAM	1	1	←— Read Data (DD RAM) —→								Reads data from DD, CG or MK RAMs	146us
	1	1	*	*	←—	Read Data (CG RAM)			—→			
	1	1	*	*	←—	Read Data (MK RAM)			—→			
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM MK RAM : Icon Display RAM AC : Address counter used for both of DD, CG and MK RAMs * = Don't care											

NOTE1 f_{OSC}=125KHz. Change frequency, change execute time too.
NOTE2 Refer to (3-1) (d) NOTE3

(3-1) Description of each instructions

(a) Maker Testing

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code writing twice is using for device testing mode (only for maker). Therefore, please do not normally use this instruction.

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

The clear display instruction is executed when the code "1" is written into DB_0.
When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set increment.
If the cursor or blink are displayed, they are returned to the left end of the LCD.
The S of entry mode does not change, the contents of CG RAM and MK RAM do not change either.
Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

* = Don't care

The return home instruction is executed when the code"1" is written into DB_1. When this instruction is executed, the DD RAM address $(00)_H$ is set into the address counter.
Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD, if the cursor or blink are on the display.
The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

The entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.
Setting address in the address counter is the only factor to decide which RAM, DDRAM CGRAM or MKRAM, is valid by this instruction.

I/D	Function
1	Address increment: The address of the DD RAM, CG RAM or MK RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM, CG RAM or MK RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

NOTE1) In case of using the smooth scroll function, set I/D=1, S=0.

NOTE2) Setting address in the address counter is the only factor to decide Which RAM is valid by the Entry Mode Set instruction.

Address counter (AC)	Valid RAM
Any of $(00)_H$～$(0E)_H$	DDRAM(1st line)
Any of $(10)_H$～$(1E)_H$	DDRAM(2nd line)
Any of $(20)_H$～$(5F)_H$	CGRAM
Any of $(60)_H$～$(6D)_H$	MKRAM

NOTE3) In case of the combination, E=1, S=1(for 1st line) and S=1(for 2nd line), 1st and 2nd lines shift when writing data to the DD RAM.
The other combinations are mentioned as follows.

	Set Function	Entry Mode Set		FUNCTION
	E	S(1st line)	S(2nd line)	
mode 1	1	1	1	When writing data to 1st or 2nd line, 1st and 2nd line shifts.
		1	0	Forbidden combination
		0	1	Forbidden combination
		0	0	No Shift
mode 0	0	1	1	When writing data to 1st line, only 1st line shifts. When writing data to 2nd line, only 2nd line shifts.
		1	0	When writing data to 1st line, only 1st line shifts. When writing data to 2nd line, no shift.
		0	1	When writing data to 1st line, no shift. When writing data to 2nd line, only 2nd line shifts.
		0	0	No shift.

(e) Display On/Off Control

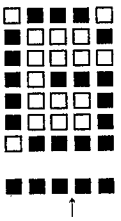
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

The display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

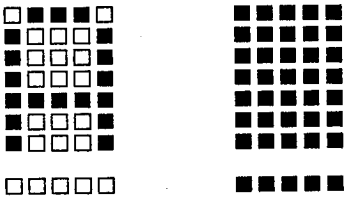
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 520ms at f_{OSC}=125kHz for 14-character 2-line. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	D	D

Shift line

The cursor/display Shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display.
The contents of address counter(AC) does not change by operation of the display shift only.
In case the cursor and display Shift instruction is executed at the same time, if the display shift-line is different from the cursor-line, the display shift is executed but the cursor shift is not.

S/C	R/L	DB_1	DB_0	Function
0	0	*	*	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	*	*	Shifts the cursor position to the right((AC) is incremented by 1)
1	0	0	1	Shifts the entire 1st line to the left, the cursor follows it.
1	1	0	1	Shifts the entire 1st line to the right, the cursor follows it.
1	0	1	0	Shifts the entire 2nd line to the left, the cursor follows it.
1	1	1	0	Shifts the entire 2nd line to the right, the cursor follows it.
1	0	1	1	Shifts the entire 1st and 2nd line to the left, the cursor follows it.
1	1	1	1	Shifts the entire 1st and 2nd line to the right, the cursor follows it.

*:Don't Care

5

(g) Dot Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	S2	S1	D	D	D

Number of dot-shift

The dot shift instruction sets shift line and the number of dot-shift.
Combination of this instruction and the display shift instruction realize the horizontal smooth scroll.
Refer to the following table.

S2	S1	Function
1	1	1st and 2nd line are dot-shifted.
1	0	1st line is dot-shifted.
0	1	2nd line is dot-shifted.
0	0	No control.

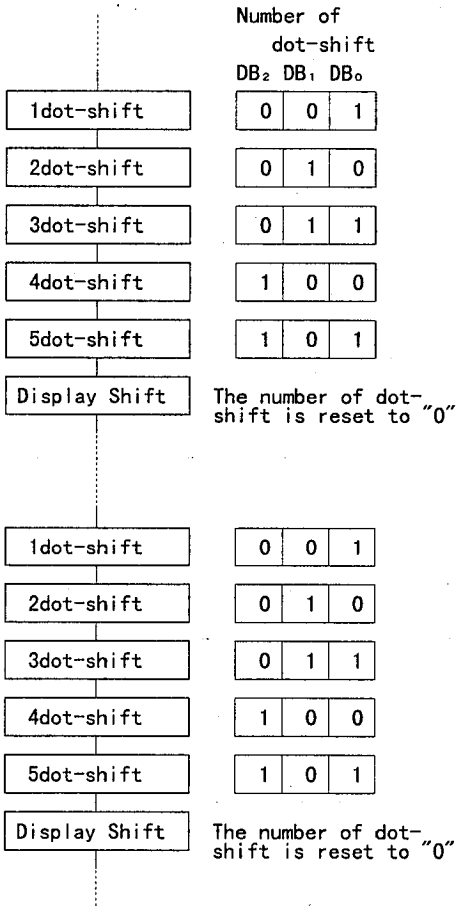
DB_2	DB_1	DB_0	Function
0	0	0	No shift.
0	0	1	1dot-shift to the left.
0	1	0	2dot-shift to the left.
0	1	1	3dot-shift to the left.
1	0	0	4dot-shift to the left.
1	0	1	5dot-shift to the left.
1	1	0	Don't Care
1	1	1	

NOTE1) In case of S1=1, S2=1, the 1st and 2nd lines dot-shift.
NOTE2) Set 1/D=1, S=0, in the entry mode set, for the line using the smooth scroll function.
NOTE3) The number of dot-shift is reset to "0" by the execution of the Display Shift instruction.

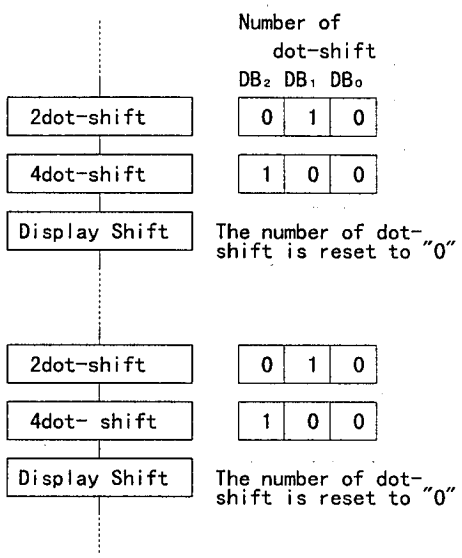
• Smooth scroll sequence

One out of the following three types of smooth scroll can be selectd by the instructions.

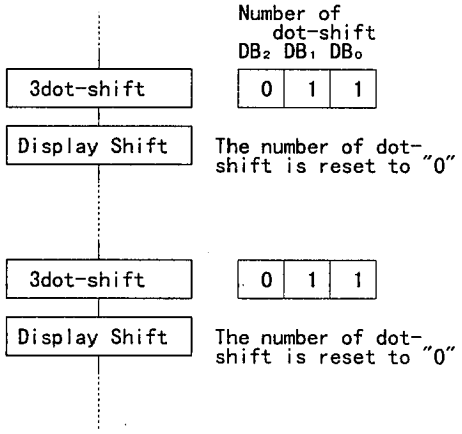
1 dot smooth scroll



2 dot smooth scroll



3 dot smooth scroll



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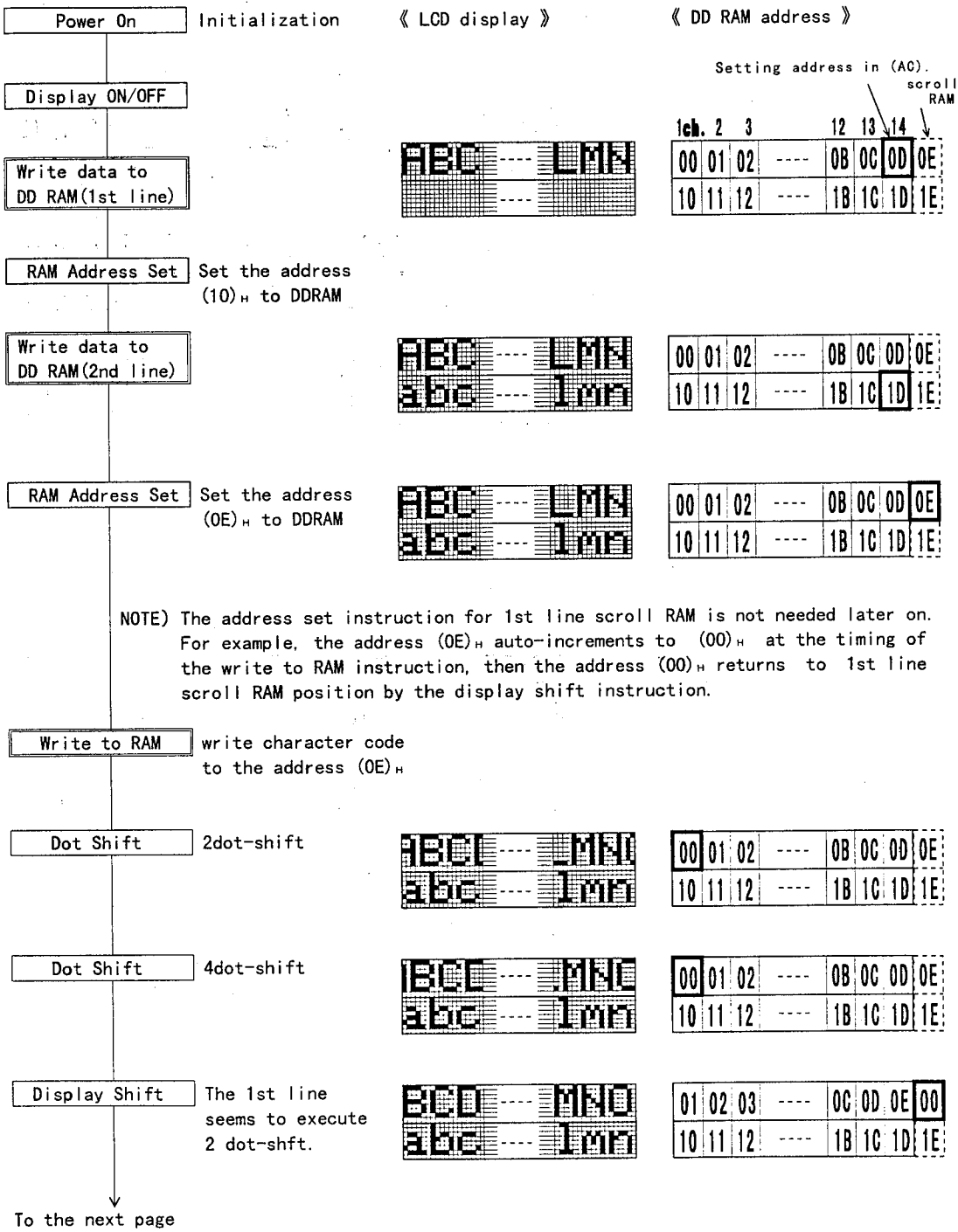
・Example of 2 dot smooth scroll (14-character, 2-line Display and only 1st line scroll)

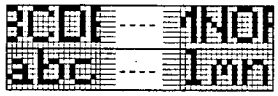
The 1st line smooth scroll sequence, which is executed by the 2 dot-shift instruction, LCD display and DD RAM address movement are shown as follows.



From the last page

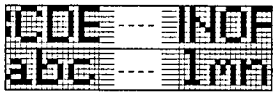
Write to RAM — write character code to the address $(00)_H$

Dot Shift — 2dot-shift



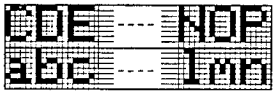
01	02	03	----	0C	0D	0E	00
10	11	12	----	1B	1C	1D	1E

Dot Shift — 4dot-shift



01	02	03	----	0C	0D	0E	00
10	11	12	----	1B	1C	1D	1E

Display Shift — The 1st line seems to execute 2 dot-shift.

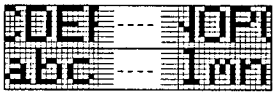


02	03	04	----	0D	0E	00	01
10	11	12	----	1B	1C	1D	1E

5

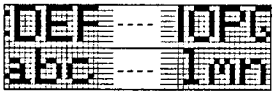
Write to RAM — write character code to the address $(01)_H$

Dot Shift — 2dot-shift



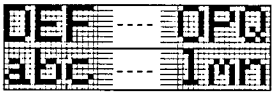
02	03	04	----	0D	0E	00	01
10	11	12	----	1B	1C	1D	1E

Dot Shift — 4dot-shift



02	03	04	----	0D	0E	00	01
10	11	12	----	1B	1C	1D	1E

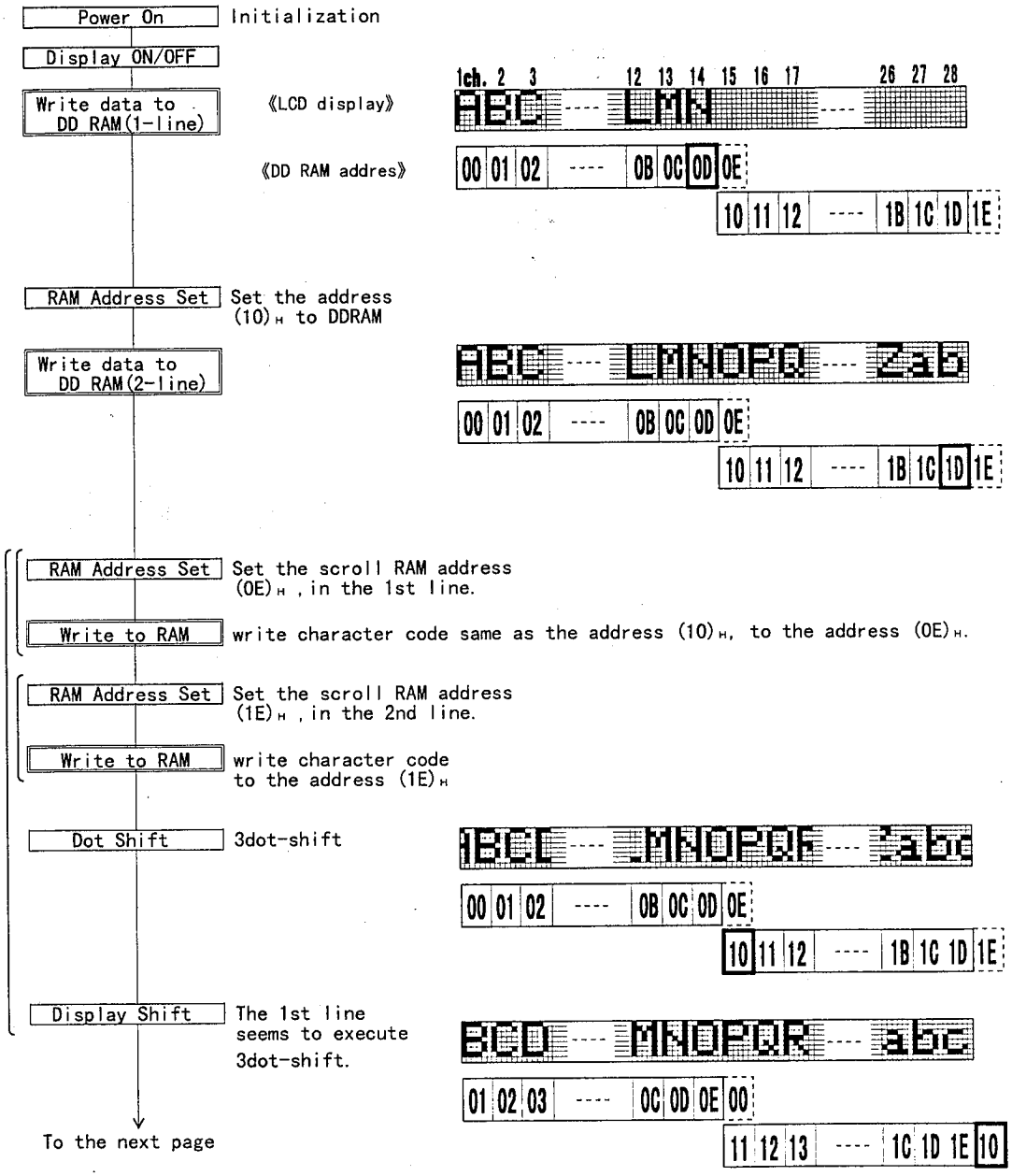
Display Shift — The 1st line seems to execute 2 dot-shift.



03	04	05	----	0E	00	01	02
10	11	12	----	1B	1C	1D	1E

・Example of 3 dot smooth scroll (28-character, 1-line Display)

The smooth scroll sequence, which is executed by the 3 dot-shift instruction, LCD display and DD RAM address movement are shown as follows.



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From the last page

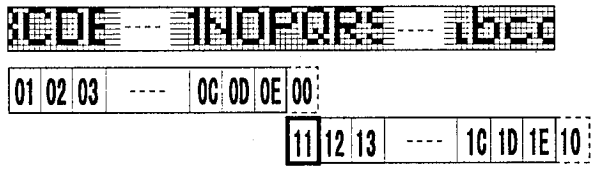
RAM Address Set — Set the scroll RAM address $(00)_H$, in the 1st line.

Write to RAM — write character code same as the address $(11)_H$, to the address $(00)_H$.

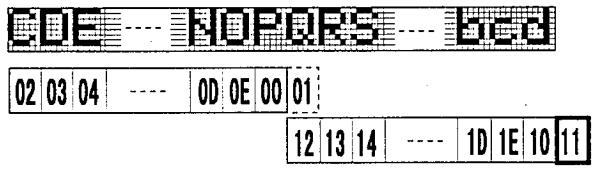
RAM Address Set — Set the scroll RAM address $(10)_H$, in the 2nd line.

Write to RAM — write character code the address to $(10)_H$

Dot Shift — 3dot-shift



Display Shift — The 1st line seems to execute 3dot-shift.



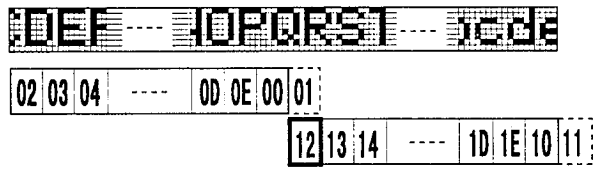
RAM Address Set — Set the scroll RAM address $(01)_H$, in the 1st line.

Write to RAM — write character code same as the address $(12)_H$, to the address $(01)_H$.

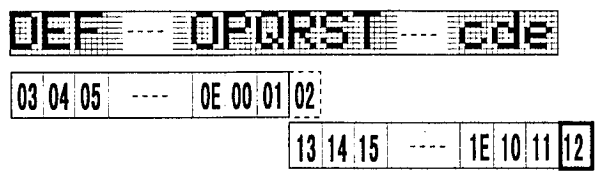
RAM Address Set — Set the scroll RAM address $(11)_H$, in the 2nd line.

Write to RAM — write character code to the address $(11)_H$

Dot Shift — 3dot-shift



Display Shift — The 1st line seems to execute 3dot-shift.



(h) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	1	N	E	D	D	D	D
							E.V.R. Value			

This instruction sets which is the display mode for 1 line or 2 lines, and which is the entry mode "S" for 1 line or 2 lines.

N	Function
1	1 line display mode. Duty: 1/9 duty.
0	2 lines display mode. Duty: 1/18 duty.

E	Function
1	Entry Mode Set "S(Entire Display shift)" for 2 lines.
0	Entry Mode Set "S(Entire Display shift)" for 1 line. Setting address in the address counter(AC) decides which line is selected.

The contrast control is performed by the internal Electrical Variable Resistor(E.V.R.), The E.V.R. is controlled by setting data to DB_3 ~ DB_0 in this instruction.

DB_3	DB_2	DB_1	DB_0	V_{LCD} (V_{DD}-V_5)
0	0	0	0	V_{DD}-6V HIGH
	:			:
1	1	1	1	V_{DD}-4V LOW

(i) RAM Address Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1			ADDRESS				

The RAM address set instruction set the address data of DD RAM, CG RAM and MK RAM. The address data wraps around within each RAM, in which the address is set by this instruction.

DD RAM(1st line) → 00_H ←→ $0E_H$ ←

DD RAM(2nd line) → 10_H ←→ $1E_H$ ←

CG RAM → 20_H ←→ $5F_H$ ←

MK RAM → 60_H ←→ $6D_H$ ←

NOTE) The Set RAM Address instruction is required when the writing/reading data "to 1st line" turns to "to 2nd line", or 2nd line to 1st line.

(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A

←Higher order bit Lower order bit→

This instruction reads out the internal status of the NJU6520. When this instruction is executed, the busy flag (BF) which indicate internal operation is read out from DB_7 and the address of the CG RAM, DD RAM and MK RAM is read out from DB_6 to DB_0 (the address for the CG RAM, DD RAM or MK RAM is determined by the previous instruction). (BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation. address counter(AC) used CG RAM, DD RAM, is dependence before function.

(k) Write Data to DD RAM, CG RAM or MK RAM

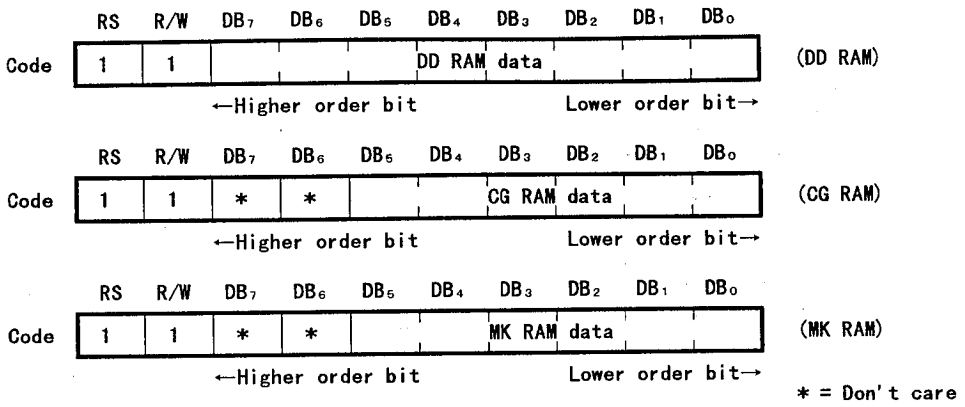
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	0	DD RAM data								(DD RAM)
Code	1	0	*	*	CG RAM data						(CG RAM)
Code	1	0	*	*	MK RAM data						(MK RAM)

←Higher order bit Lower order bit→

* = Don't care

By the execution of this instruction, the RAM data of CG RAM, DD RAM or MK RAM is written into the CG RAM, DD RAM or MK RAM.
The selection of the RAM is determined by previous instruction (the RAM written must be selected before). After this instruction execution, the address increment (+1) or decrement (-1) is performed automatically according to the entry mode set.
And the display shift is also executed according to the previous entry mode set.

(I) Read Data to DD RAM, CG RAM or MK RAM

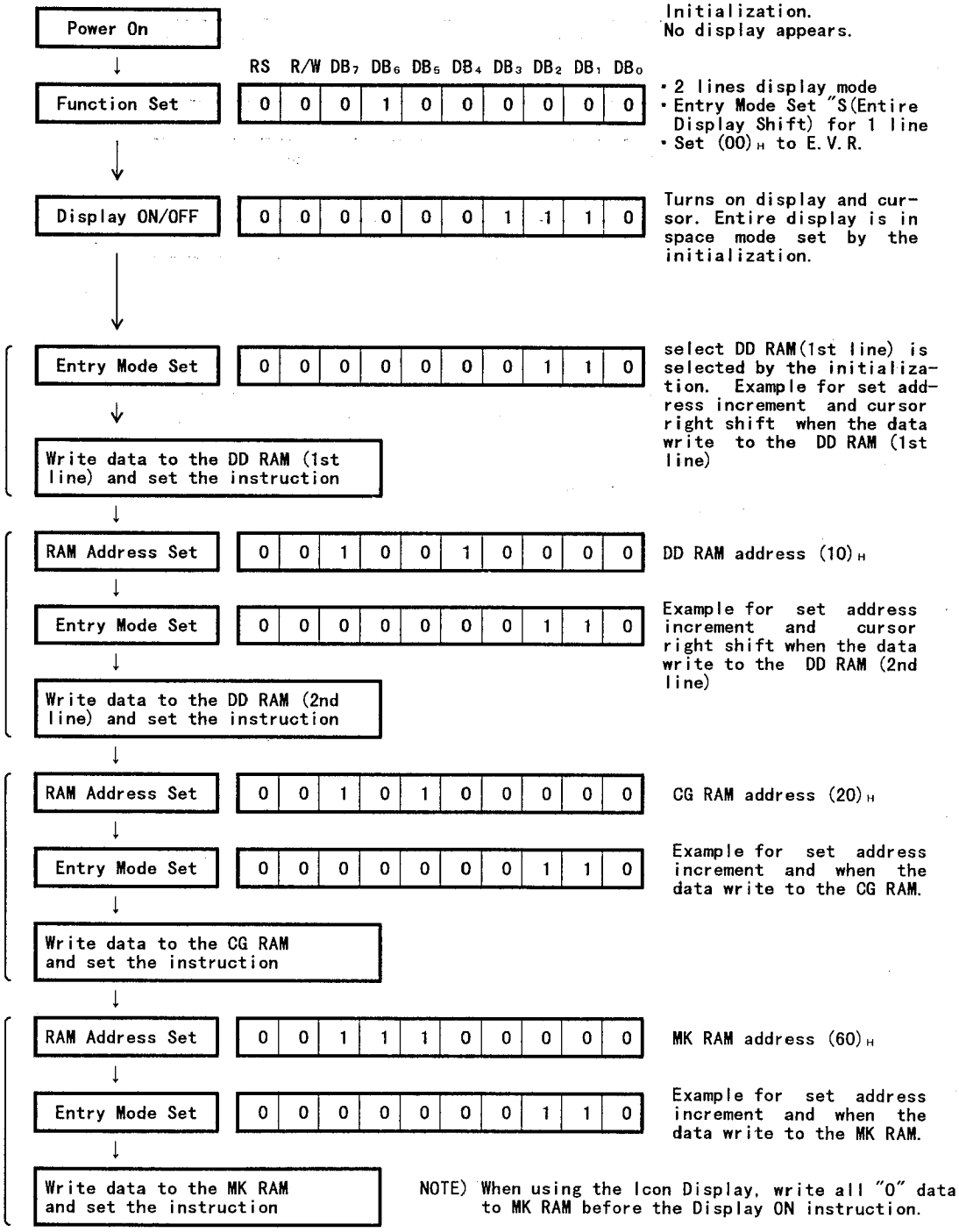


The CG RAM, DD RAM or MK RAM is determined by previous instruction.
Before executing this instruction, either the CG RAM address set, DD RAM address or MK RAM set must be executed, otherwise the first read out data are invalidated.
When this instruction is serially executed, the next address data is normally read from the second read.
The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading). The cursor shift instruction has same function as the DD RAM address set.
After reading the RAM, the address increment or decrement is executed automatically according to the entry mode. But display shift does not occur regardless of the entry mode.

(3-2) Initialization using the internal reset circuits

14-character 2-line display (Using internal reset circuits).

The Function set, display On/Off control and entry mode set instruction must be executed before the data input, as shown below.



NOTE) When using the Icon Display, write all "0" data to MK RAM before the Display ON instruction.

5

(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6520 must be initialized by the instruction.

Power On → Initialization. No display appears.

↓

Wait more than 15ms after V_{DD} rises to 2.4V

↓

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Function Set	0	0	0	1	0	0	0	0	0	0	• 2 lines display mode • Entry Mode Set "S(Entire Display Shift) for 1st line • Set $(00)_H$ to E.V.R.
Display OFF	0	0	0	0	0	0	1	0	0	0	
Clear Display	0	0	0	0	0	0	0	0	0	1	
RAM Address Set	0	0	1	0	0	0	0	0	0	0	DD RAM address $(00)_H$
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data write to the DD RAM (1st line)
RAM Address Set	0	0	1	0	0	1	0	0	0	0	DD RAM address $(10)_H$
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data write to the DD RAM (2nd line)
RAM Address Set	0	0	1	0	1	0	0	0	0	0	CG RAM address $(20)_H$
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and when the data write to the CG RAM.
RAM Address Set	0	0	1	1	1	0	0	0	0	0	MK RAM address $(60)_H$
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and when the data write to the MK RAM.
RAM Address Set	0	0	1	0	0	0	0	0	0	0	DD RAM address $(00)_H$
Dot Shift	0	0	0	0	1	1	1	0	0	0	Set "0" to the number of Dot Shift

↓

Initialized end

NOTE) When using the Icon Display, write all "0" data to MK RAM before the Display ON instruction.

(4) LCD display

(4-1) Power Supply for LCD Driving

NJU6520 incorporates Voltage converter (tripler or doubler) to generate high LCD driving voltage, and it possible to display high contrast characters.

(a) Voltage converter

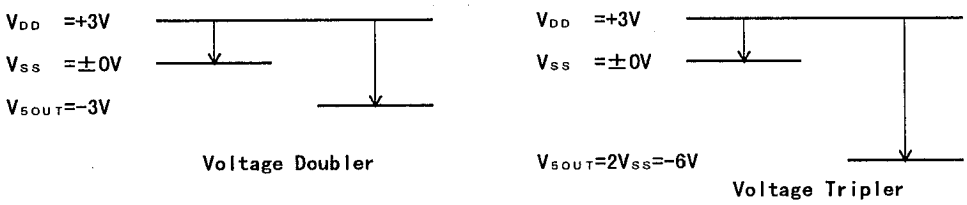
· Voltage tripler

By connecting the capacitor between C_1^+ and C_1^-, C_2^+ and C_2^-, V_{SS} and V_{SOUT} respectively, two times negative voltage of $V_{DD} - V_{SS}$ output from V_{SOUT}.

· Voltage doubler

By connecting the capacitor between C_2^+ and C_2^-, V_{SS} and V_{SOUT} respectively, and connecting the C_1^+ terminal to C_2^+ terminal, and C_1^- terminal being open, negative voltage of $V_{DD} - V_{SS}$ output from V_{SOUT}.

The voltage relation for Voltage tripler/doubler



5

(b) Contrast control function by using E.V.R.

The LCD driving voltage, controlling LCD display contrast, is adjusted by this instruction.

The contrast control function realizes 16 steps V_{LCD} adjustable by writing 4-bit data, DB_3, DB_2, DB_1 and DB_0, in the function set instruction.

In case the contrast control function in not used, write data $(DB_3, DB_2, DB_1, DB_0) = (0, 0, 0, 0)$ in the Function Set.

DB_3	DB_2	DB_1	DB_0	V_{LCD} (V_{DD}-V_5)
0	0	0	0	V_{DD}-6V HIGH
		⋮		⋮
1	1	1	1	V_{DD}-4V LOW

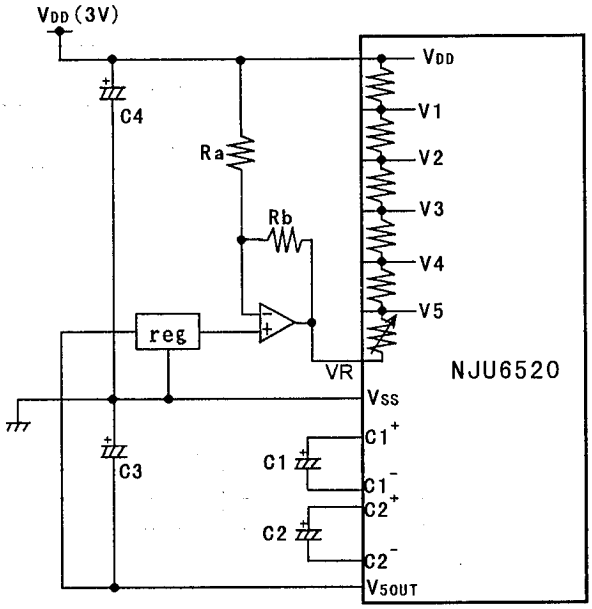
NOTE) In condition "$V_R = V_{DD}$-6V", V_{LCD} is selected one out of 16step voltages between V_{DD}-4V and V_{DD}-6V.

(4-2) LCD driving voltage generation circuit

V_1, V_2, V_3, V_4, these LCD driving Voltage are generated by the internal bleeder resistors. Capacitor sizes in the following figure should be determined by test using actual LCD module.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/18
	Bias	1/5
V_{LCD}		$V_{DD}-V_5$



Typical value : C1~C4=1.0~10μF

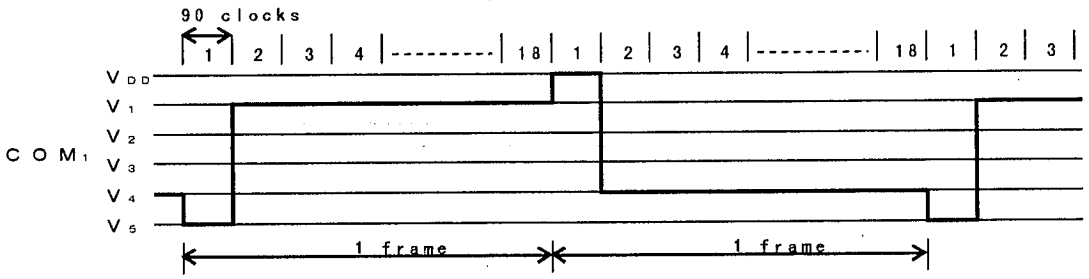
(a) Typical application for the LCD driving voltage and contrast control function.

NOTE) This voltage generation circuit is designed for small size LCD, not for large size LCD. If the contrast is low quality for large size LCD, connect capacitors between each LCD driving voltage terminals (V1, V2, V3, V4) and V_{DD}, or supply external voltage to these terminals.

(4-3) Relation between oscillation frequency and LCD frame frequency

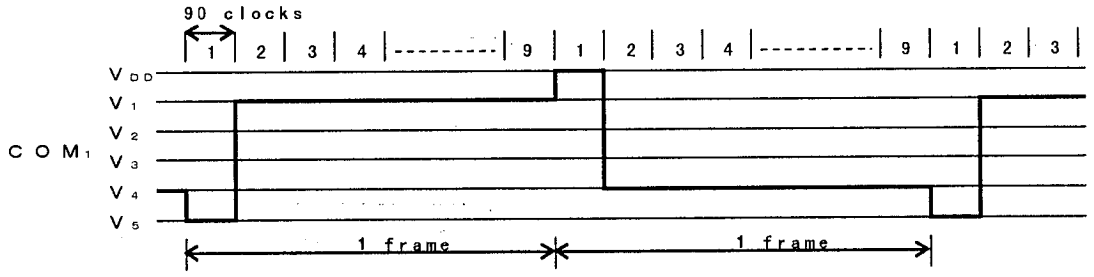
As the NJU6520 incorporate oscillation capacitor and resistor for CR oscillation, 125kHz oscillation is available without any external components.
The LCD frame frequency example mentioned below is based on 125kHz oscillation.
(1 clock = 8.0us)

1/18 duty ratio



1frame = 8(μs) × 90 × 18=12960(μs)=12.96(ms)
Frame frequency = 1/12.96(ms)=77.16(Hz)

1/9 duty ratio



1frame = 8(μs) × 90 × 9=6480(μs)=6.48(ms)
Frame frequency = 1/16.48(ms)=154.32(Hz)

NOTE) The change of surrounding temperature influences to the frame frequency, and then LCD contrast might be unstable.

(5) Serial Interface with MPU

Serial interface circuit is activated when the chip select terminal (CS) goes to "L" level.

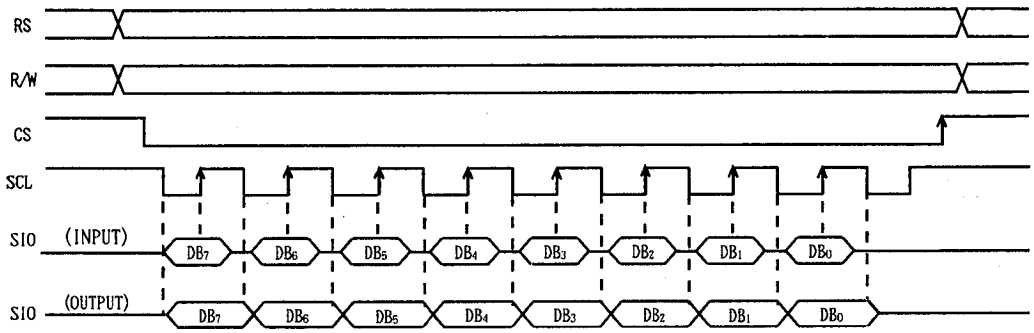
The data input/output is MSB first like as the order of DB_7, DB_6 ···· DB_0. The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input.

In case of entering over than 8-bit data, valid data is last 8-bit data.

The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.

The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



MSB LSB

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Input/Output data format

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	− 0.3 ～ + 7.0	V
Supply Voltage (2)	V_5	V_{DD}−13.5 ～ V_{DD}+0.3	V
Input Voltage	V_{IN}	− 0.3 ～ V_{DD}+0.3	V
Operating Temperature	Topr	− 30 ～ + 80	°C
Storage Temperature	Tstg	− 55 ～ + 125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) Decoupling capacitor should be connected between V_{DD} and V_{SS}, V_{DD} and V_5 due to the stabilized operation for the LSI.

Note 3) All voltage values are specified as V_{SS} = 0V

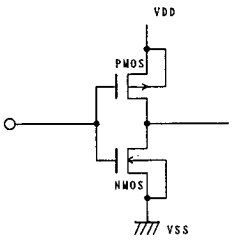
Note 4) The relation : $V_{DD} \geqq V_{SS}$, $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$, V_{SS}=0V must be maintained.
Turn on V_{DD} and V_5 at same time or turn on V_{DD} first then turn on V_5 must be required.
If the turn on sequence does not meet above conditions, latch up will occur.

■ ELECTRICAL CHARACTERISTICS (V_{DD}=3V±20%, V_{SS}=0V, Ta=−20～+75°C)

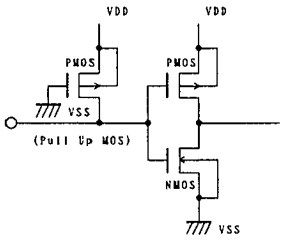
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Operating Voltage (1)	V_{DD}		2.4	—	3.6	V	
Operating Voltage (2)	V_5		V_{DD}−3.0	—	V_{DD}−13.5	V	
Input Voltage	V_{IH}		0.8V_{DD}	—	V_{DD}	V	5
	V_{IL}		—	—	0.2V_{DD}	V	5
Output Voltage	V_{OH}	$-I_{OH}$=0.205mA	2.0	—	—	V	6
	V_{OL}	I_{OL}=1mA	—	—	0.5	V	6
Driver On-resist. (COM)	R_{COM1}	±I_d=50uA (All COM terminal) Vo=V_{DD}, V_5	—	—	20	kΩ	
Driver On-resist. (SEG)	R_{SEG1}	±I_d=50uA (All COM terminal) Vo=V_{DD}, V_5	—	—	30	kΩ	
Driver Output resistor (COM)	R_{COM2}	±I_d=50uA (All COM term. Vo=V_1, V_2, V_3, V_4	—	—	40	kΩ	
Driver Output resistor (SEG)	R_{SEG2}	±I_d=50uA (All COM) term. Vo=V_1, V_2, V_3, V_4	—	—	50	kΩ	
Input Leakage Current	I_{LI}	V_{IN}=0～V_{DD}	-1	—	1	μA	7
Pull-up Resistance Current	$-I_p$	V_{DD}=3V, V_{IN}=0V	10	25	50	μA	
Operating Current	I_{DD}	V_{DD}=3V、INT. f_{OSC}		250	500	μA	8
Oscillation Frequency	f_{osc}	V_{DD}=3V, Ta=25°C	65	125	180	kHz	
Tripler Output Voltage	V_{SOUT}	V_{DD}=3V, Ta=25°C I_{OUT}=100μA C1～C5=1μF	-4.6	-5.8		V	
Bleeder Resistance	R_B	V_{DD}−V_5=3V, RB×5		50		kΩ	9
E.V.R. Resistance	VR	V_5−VR=3V, DB_1～DB_3=1		25		kΩ	
Output Current	I_5	V_{DD}=3V, V_5=−6V		250	500	μA	10

Note 5) Input/Output structure except LCD driver are shown below:

Input Terminal Structure

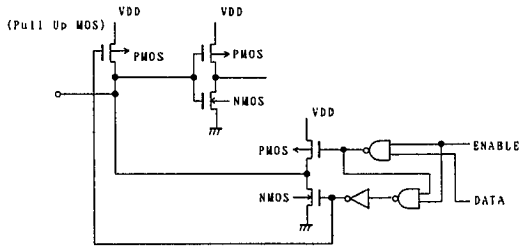


CS, SCL Terminals
(No Pull-Up MOS)



RS, R/W, RESET Terminals
(Pull-Up MOS)

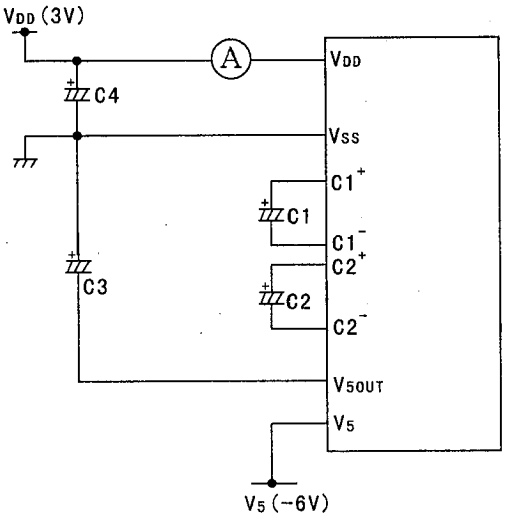
Input/Output Terminal Structure



SIO Terminal

Note 6) Apply to the Input/Output Terminal.
Note 7) Except pull-up MOS current and output driver current.

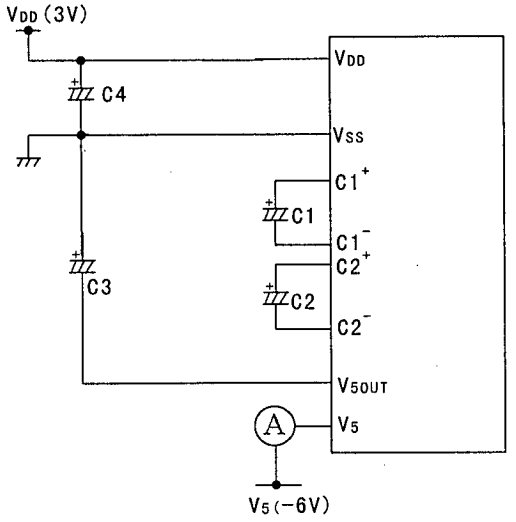
Note 8) Except Input/output current. If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L". Output drivers should be open. Connect 1.0~10uF capacitors to C1, C2, C3 and C4.



5

Note 9) Apply to total resistance(RB×5) between V_{DD} and V5 terminals.

Note 10) Except Input/output current. If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L". Output drivers should be open. Connect 1.0~10uF capacitors to C1, C2, C3 and C4.



• Serial Interface Sequence

(V_{DD}=3V±20%, V_{SS}=0V, Ta=-20~+75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial Clock Cycle Time		t_{CYCE}	1	—	図1	μs
Serial Clock Width	"High" level	t_{SCH}	700	—	図1	ns
	"LOW" level	t_{SCL}	300	—	図1	ns
Serial Clock rise and fall Time		t_{SCR}, t_{SCF}	—	20	図1	ns
Chip Select Pulse Width		PW_{CS}	500	—	図1	ns
Chip Select Setup Time		t_{CSU}	200	—	図1	ns
Chip Select Hold Time		t_{CH}	200	—	図1	ns
Chip Select rise and fall Time		t_{SCR}, t_{CSF}	—	20	図1	ns
Setup Time	RS, R/W - CS	t_{AS}	200	—	図1	ns
Address Hold Time		t_{AH}	200	—	図1	ns
Serial Input Data Setup Time		t_{SISU}	200	—	図1	ns
Serial Input Data Hold Time		t_{SIH}	200	—	図1	ns
Serial Output Data Delay Time		t_{SOD}	—	500	図1	ns
Serial Output Date Hold Time		t_{SOH}	0	—	図1	ns

•SIO Load Condition : CL=100pF

Serial Interface Timing Characteristics

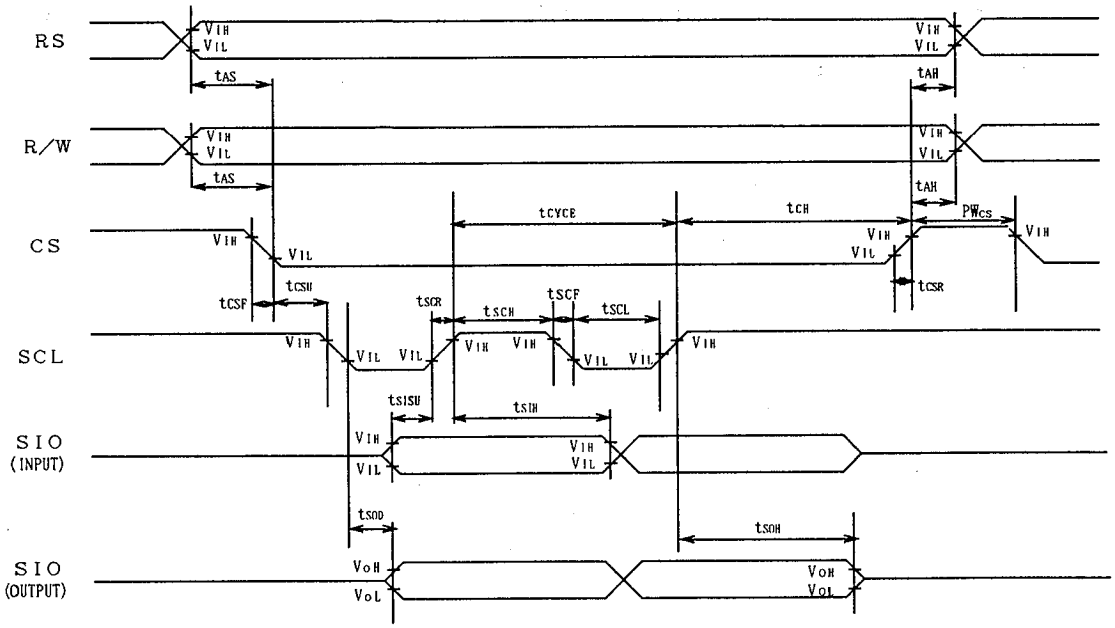
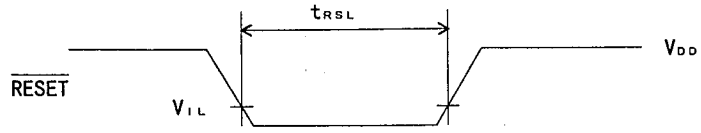


fig.1 The timing characteristics of the serial bus write/read operating sequence.

• The Input Condition when using the Hardware Reset Circuit

Input Timing



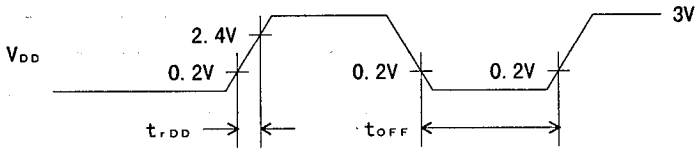
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Reset Input "L"Level Width	t_{RSL}	f_{OSC}=45kHz	1.2	—	—	ms

• Power Supply Condition when using the internal initialization circuit

(Ta=-20～+75°C)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Rise Time	t_{rDD}		0.1	—	5	ms
Power Supply OFF Time	t_{OFF}		1	—	—	ms

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
(Refer to initialization by the instruction)

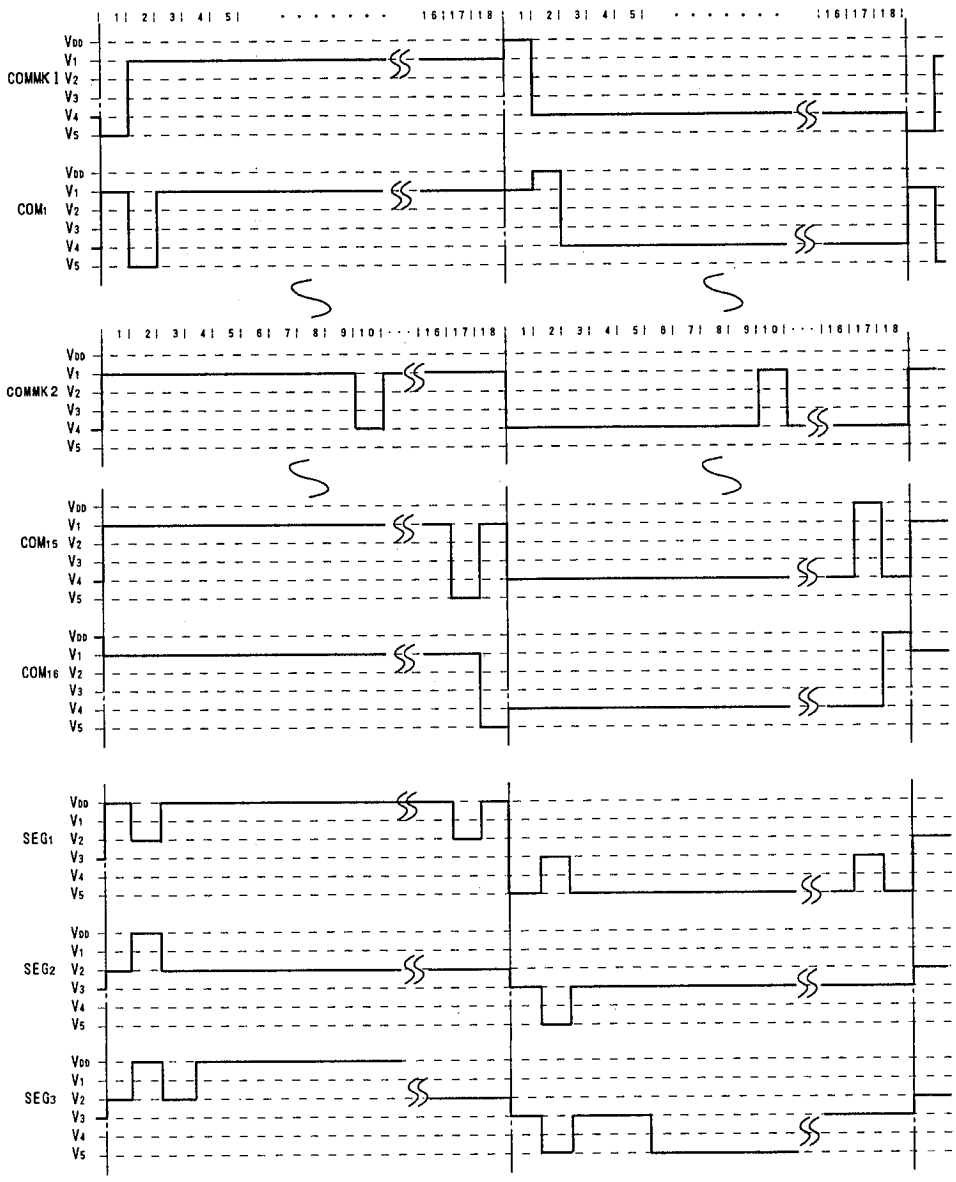


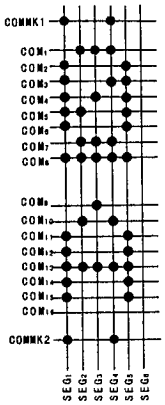
0.1ms≦t_{rDD}≦5ms　　t_{OFF}≧1ms

t_{OFF} specifies the power off time in a short period off or cyclical on/off.

■ LCD DRIVING WAVE FORM

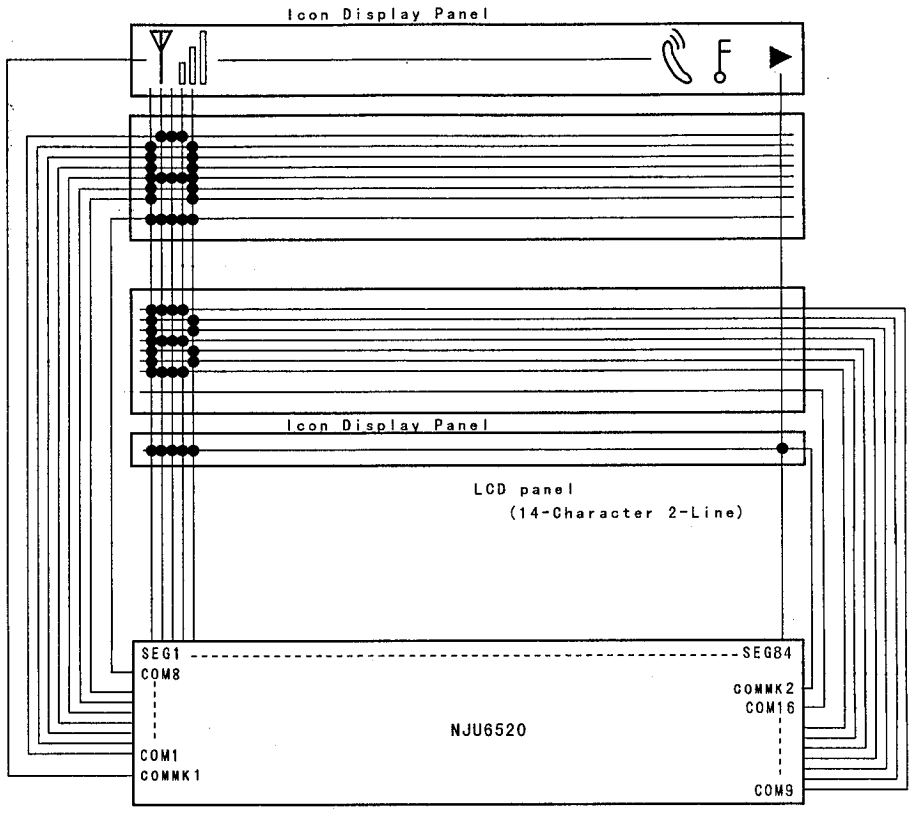
1/18 Duty Driving



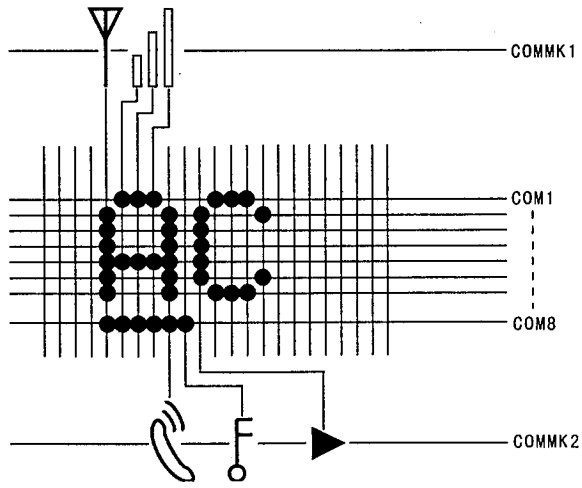


■ APPLICATION CIRCUITS

14-Character 2-Line With Icon Display Example



Icon Display Example



MEMO