PRELIMINARY

DOT MATRIX LCD 80-OUT SEGMENT DRIVER

■ GENERAL DESCRIPTION

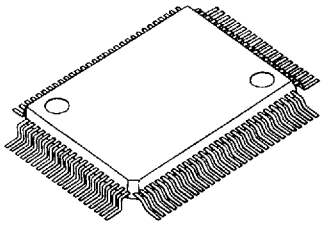
The NJU6419 is a serial input, 80-out segment driver for dot matrix LCDs.

In combination with the common driver NJU6418, it can drive large scale dot matrix LCD panels, such as 640 x 480 or 640 x 400 dots.

The wide and highly precise LCD driving voltage of -8 to -26V separated from the logic operating voltage can be supplied from the external power source to drive various LCD panels.

Furthermore, the enable chain which is effctive for the low power operation, can be made without any instruction from the controller, therefore it performs simple interface between NJU6419 and LCD controller or microprocessor.

■ PACKAGE OUTLINE



NJU6419F

■ FEATURES

- 80 Segment Drivers
- Large Scale Dot Matrix LCD panel
- 80-bit Bidirectional Shift Register
- 4 bit Bus enable chain
- External Power Supply for LCD Driving Voltage
- Enable Chain Function
- High Speed Data Transmssion
  --- Shift Clock 6MHz
- Two of Shift Direction Select Terminal
- Offset Bias for the LCD Driving Voltage Adjustable
- Display Off Mode --- $\overline{\text{DISPOFF}}$
- LCD Driving Voltage --- -8V ~ -26V
- Operating Voltage --- 5.0 V ± 10 %
- Package Outline --- QFP100/TAB/Chip
- C-MOS Technology

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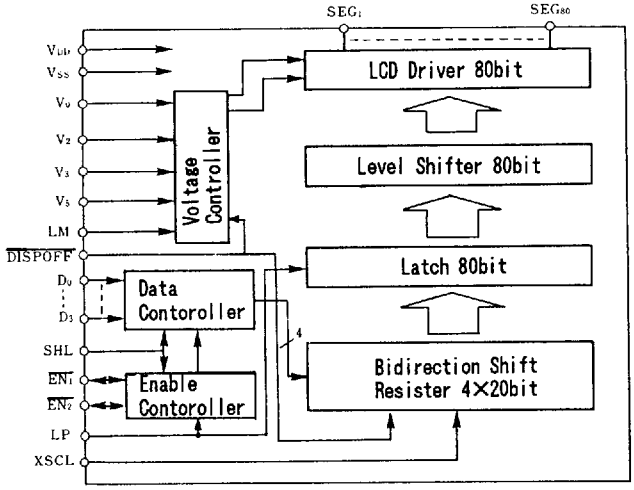
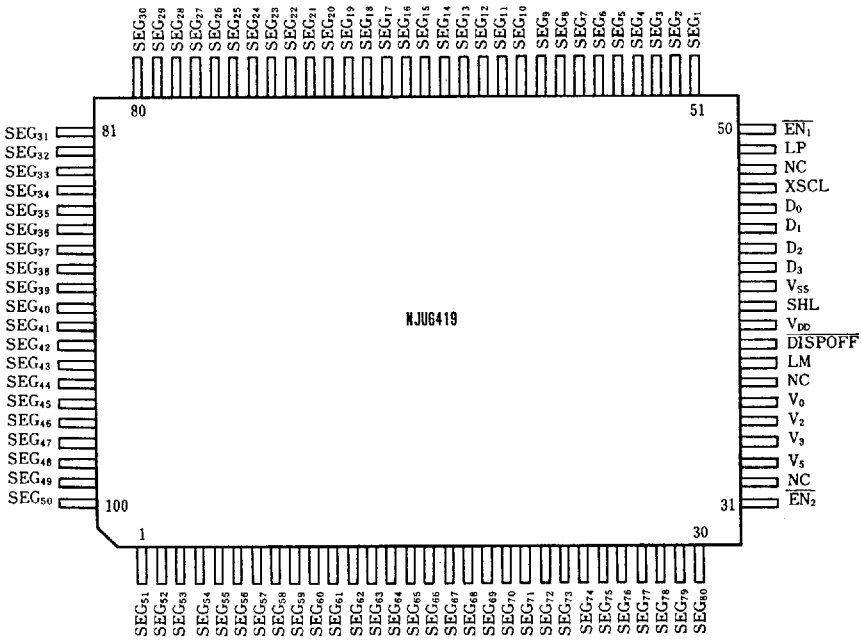
■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
40,42	V_{DD},V_{SS}	Logic operating voltage supply terminals.
36,35,34,33	V_0,V_2,V_3,V_5	LCD driving bias level supply terminals. $V_{DD} \geqq V_0 > V_2 > V_3 > V_5$, V_5=-8～26V
39	$\overline{DISPOFF}$	Display off. (All segment output level fixed to V_0.)
47	XSCL	Shift clock terminal. (The data shift by falling edge.)
49	LP	Latch pulse terminal. (The data latch by falling edge.)
38	LM	Alternate signal input for LCD driveing.
41	SHL	Shift direction and input/output selecting terminal.
43～46	D_3～D_0	Display data input terminal.
50,31	$\overline{EN_1}$,$\overline{EN_2}$	Enable signal input/output terminal.Input/Output mode is determind by SHL level. Output is reset by LP terminal. When 80 bit data are read, this terminal fall to "L" level automatically.
51～100 1～30	SEG_1～SEG_{80}	LCD segment driving terminal. Output signal change by falling edge of LP terminal.
32,37,48	NC	Non Connection

SHL	$\overline{EN_1}$	$\overline{EN_2}$	COM signal shift direction
L	output	input	$SEG_1 \leftarrow SEG_{80}$
H	input	output	$SEG_1 \rightarrow SEG_{80}$

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■ FUNCTIONAL DESCRIPTION

(1)Data Control Circuits

Arrenge the display data input from D_0~D_3 according to SHL status and send to the internal bus. When the enable signal is disable condition, the internal bus is fixed to "L" level.

(2)Enable Control Circuits

When the enable signal is disable condition, the internal clock live and data bus are fixed to "L" level and becomes power-saving mode.

In case of the plural segment driver connection,cascade the each $\overline{EN}$ terminal and the $\overline{EN}$ terminal of first segment driver connect to the V_{SS}.

After read the 80 bit, enable control circuits output the enable signal to the next segment driver automatically after read the 80 bit of display data.

Therefore no need to send a enable signal to each segment driver by controller.

(3)Shift register

The 80-bit shift register is a bidirectional register.

The shift direction of 80-bit bidirectional shift register is shown below:

Control Terminal	Input	Shift Direction
SHL	L	1 → 80
	H	1 ← 80

(4)Latch

The display data in the shift register is transferd to the latch by falling edge of LP signal and send to the LCD driver through level shifter.

(5)Level shifter

80-bit level shifters changes the logic operating voltage to LCD driving voltage.

(6)LCD driver output truth table

80-bit LCD driver output following level according to display data, LM signal and $\overline{DISPOFF}$.

Display Data	LM	$\overline{DISPOFF}$	Driver Output (SEG_1 to SEG_{80})
H	H	H	V_5
	L	H	V_0
L	H	H	V_3
	L	H	V_2
-	-	L	V_0

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■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	(1)	V_{DD}	- 0.3 ~ +6.0	V
Supply Voltage	(2)	V_{DD}-V_5	-30.0 ~ +0.3	V
Supply Voltage	(2)	V_0,V_2,V_3	V_5-0.3 ~ V_{DD}+0.3	V
Input Voltage	(1)	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Output Voltage	(1)	V_{OUT}	-0.3 ~ V_{DD}+0.3	V
Output Current	(1)	I_{OUT}	20	V
Output Current	(2)	I_{OSEG}	20	V
Power Dissipation		P_D	300	mW
Operating Temperature		Topr	-20 ~ +75	℃
Storage Temperature		Tstg	-40 ~ +125	℃

Note 1) The relation : $V_{DD} \geqq V_{SS} \geqq V_5$ must be maintained.

2) The relation : $V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5$ must be maintained.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Ta=-20～+75℃)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}			4.5	5.0	5.5	V
LCD Driving Voltage	V_5	Recommendation		-23		-14	V
		Maximum				-3	V
LCD Driving Voltage	V_0			2.5		5.0	V
LCD Driving Voltage	V_2			5/9·V_5		V_1	V
LCD Driving Voltage	V_3			V_5		4/9·V_5	V
Input Voltage	V_{IH}	$\overline{EN_1}$, $\overline{EN_2}$, D_0～D_3, $\overline{DISPOFF}$ XSCL, LP, SHL, LM, Terminals		0.8V_{DD}			V
	V_{IL}	XSCL, SHL, LM Terminals				0.2V_{DD}	V
Output Voltage	V_{OH}	I_{OH}=-0.6mA	$\overline{EN_1}$, $\overline{EN_2}$ Terminals	V_{DD}-0.4			V
	V_{OL}	I_{OL}= 0.6mA				V_{SS}+0.4	V
Input Leakage Current	L_{LI}	V_{IN}=V_{DD} or 0V	D_0～D_3, XSCL, LP, SHL, LM, $\overline{DISPOFF}$			2.0	μA
	L_{LLO}		$\overline{EN_1}$, $\overline{EN_2}$			5.0	μA
Stand-by Current	I_{DSS}	V_5=-8～-26V, V_{IH}=V_{DD}, V_{IL}=V_{SS}				25	μA
Output Resistance	R_{SG}	|ΔV$_{ON}$|=0.5V SEG Terminal	V_5=-20V		1.4	3.5	kΩ
			V_5=-14V		1.7	4.5	kΩ
			V_5= -8V (1)		2.7	8.0	kΩ
Operating Current (1)	I_{SS1}	V_{DD}=5V, V_{IH}=V_{DD}, V_{IL}=V_{SS} f_{XSCL}=1.92MHz, f_{LP}=12kHz frame f=60Hz, Input "H" every 1/128duty No Load, V_{SS} Terminal			120	500	μA
Operating Current (2)	I_{SS2}	V_2= -4V, V_3=-16V, V_5=-20V V_{DD}=5V, V_{IH}=V_{DD}, V_{IL}=V_{SS} f_{XSCL}=1.92MHz, f_{LP}=12kHz frame f=60Hz, Input "H" every 1/128duty No Load, V_5 Terminal			20	100	μA
Input Terminal Capacitance	C_I	D_0～D_3, XSCL, LP, SHL, LM Terminals				8.0	pF
	C_I/$_O$	freq=1MHz $\overline{EN_1}$, $\overline{EN_2}$ Terminals				15.0	pF

Note 1) This value is reference. not subject to test.

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• AC Characteristics

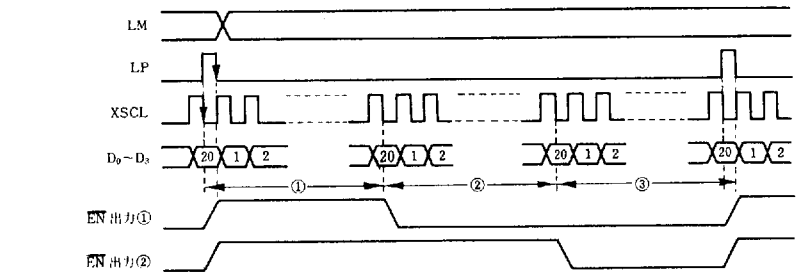
(Ta=-20~75℃, V_{DD}=5V±10%)

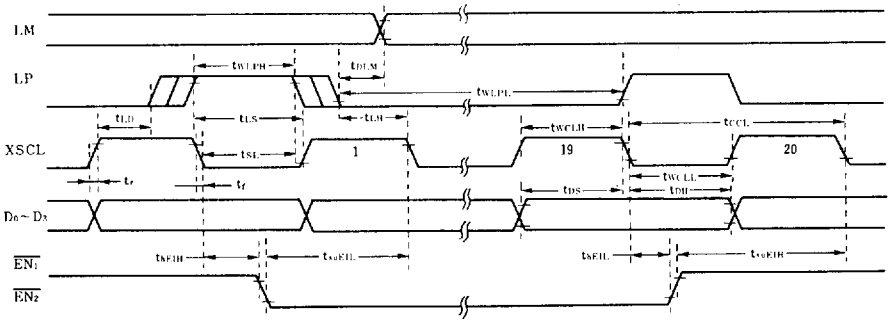
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Rise Time (1)	tr				50	ns
Fall Time (1)	tf				50	ns
XSCL Cycle	t_{CCL}	tr,tf≦10ns	166			ns
XSCL "H" Pulse Width	t_{WCLH}		70			ns
XSCL "L" Pulse Width	t_{WCLL}		70			ns
Data Set up Time	t_{DS}		60			ns
Data Hold Time	t_{DH}		40			ns
XSCL rise → LP rise delay	t_{LD}		70			ns
XSCL fall → LP fall delay	t_{SL}		70			ns
LP rise → XSCL rise delay	t_{LS}		70			ns
LP fall → XSCL fall delay	t_{LH}		70			ns
LP "H" Pulse Width	t_{WLPH}		70			ns
LP "L" Pulse Width	t_{WLPL}		230			ns
LM Transition Time	t_{DLM}		-500		500	ns
Enable "H" Set up Time	t_{SUEIH}		0			ns
Enable "H" Hold Time	t_{HEIH}		0			ns
Enable "L" Set up Time	t_{SUEIL}		40			ns
Enable "L" Hold Time	t_{HEIL}		0			ns

Note 1) Whenh high speed operation, the tr and tf should be satisfied as following formula.

$$t_r, t_f < \frac{t_{CCL}-(t_{WCLH}+t_{WCLL})}{2}$$

• INPUT TIMING CHART



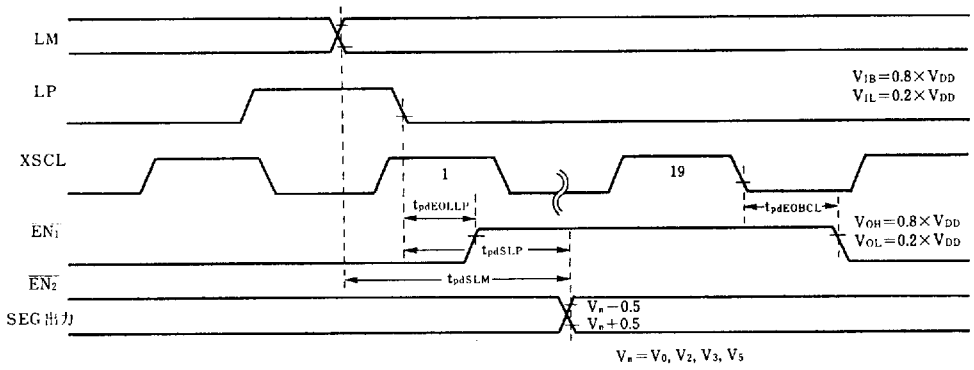


V_{IH} = 0.8 V_{DD}
V_{IL} = 0.2 V_{DD}

(Ta=-20～75℃, V_{DD}=5V±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LP fall→Disable time	$t_{pdEOLLP}$	XSCL="L"			70	ns
XSCL fall→Enable time	$t_{pdEOHCL}$	C_L=15pF			100	ns
LP fall→SEG output time	t_{pdSLP}	V_5=-8～26V			4.5	μs
LM→SEG output delay time	t_{pdSLM}	C_L=100pF			4.5	μs

• OUTPUT TIMING CHART



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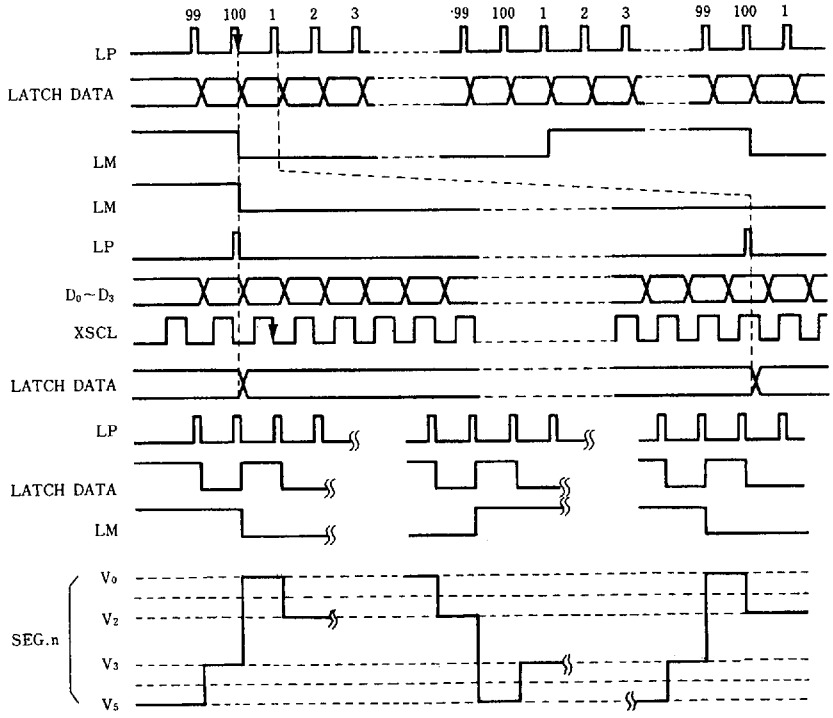
■ TIMING DIAGRAM (For example : 1/100 duty)



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■ LCD DRIVING SUPPLY VOLTAGE

(1)LCD Driving Bias Level

The simple method to get the LCD driving bias level is using a bleeder resistance shown below. To get the high quality display, the high accurate and high stability of bias level are required. Therefor, the smaller bleeder resistance have to use within allowable range by system power capacitance.

If the system required low power application, higher bleeder resistance and voltage follower is better way.

To avoide the LCD driving capability down, V_{DD}-V_O showld be use 0～2.5V. And if the voltage follower does not use, V_O have to connect to the V_{DD}.

(2)Notice for the Power ON/OFF

If the LCD driving voltage supply in flowing condition of logic operating voltage V_{DD}, the latch up will occur and the NJU6419 may be destroy.

Therefor, please follow below items when power is turned on and off.

・When TURN ON

Logic Operating Voltage "ON" first then LCD driving voltage "ON" or turn "ON" both voltage at same time.

・When TURN OFF

LCD Driving voltage "OFF" first then logic operating voltage "OFF" or turn off both voltage at same time.

To avoid the over current, connecting the resistance (about 22Ω) between V_5 and V_{SSH} terminal is required.

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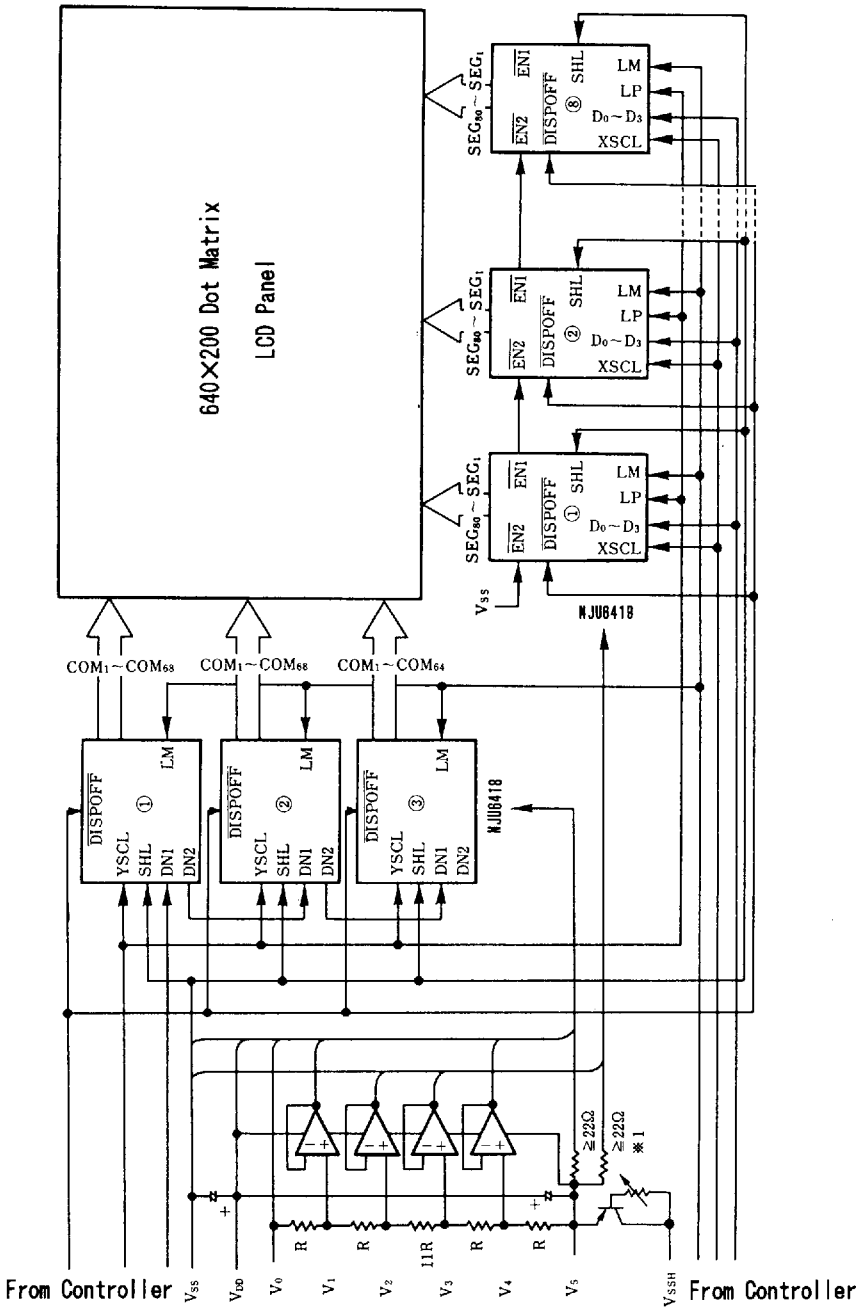
■ APPLICATION CIRCUIT

640 x 200 Dot Matrix LCD Example



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