PRELIMINARY

DOT MATRIX LCD 68-OUT COMMON DRIVER

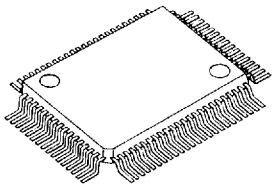
■ GENERAL DESCRIPTION

The NJU6418 is a serial input, 68-out common driver for dot matrix LCDs.

In combination with the segment driver NJU6419, it can drive large scale dot matrix LCD panels, such as 640 x 480 dots.

The wide and highly precise LCD driving voltage of -7 to -23V separated from the logic operating voltage can be supplied from the external power source to drive various LCD panels.

■ PACKAGE OUTLINE

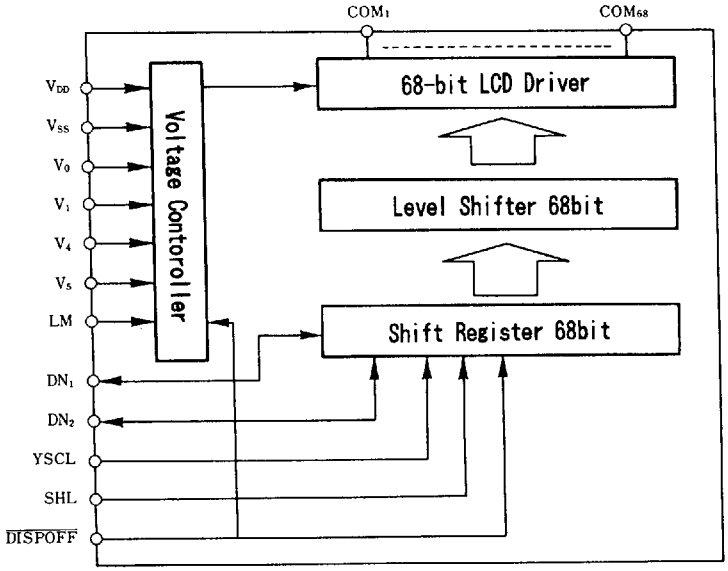


NJU6418F

■ FEATURES

- 68 Common Drivers
- Large Scale Dot Matrix LCD panel
- 68-bit Bidirectional Shift Register
- Two of Shift Direction Select Terminal
- Offset Bias for the LCD Driving Voltage Adjustable
- External Power Supply for LCD Driving Voltage
- Display Off Mode --- $\overline{DISPOFF}$
- Wide LCD Driving Voltage --- -8V ~ -26V
- Logic Operating Voltage --- 5.0 V ± 10 %
- Package Outline --- QFP80/TAB/Chip
- C-MOS Technology

■ BLOCK DIAGRAM



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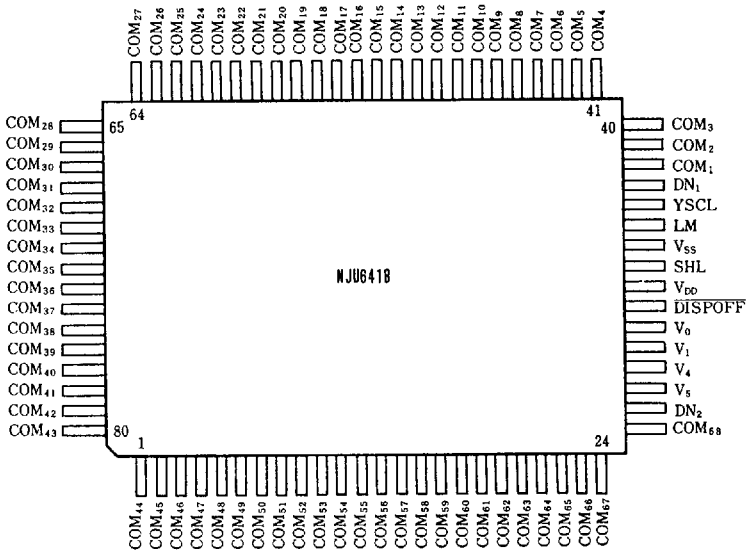
■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
32,34	V_{DD},V_{SS}	Logic operating voltage supply terminals.
30,29,28,27	V_0,V_1,V_4,V_5	LCD driving bias level supply terminals. $VDD \geqq V_0 > V_1 > V_4 > V_5$, V_5=-8～-26V
31	$\overline{DISPOFF}$	Display Off (All common output level fixed to V_0).
36	YSCL	Shift clock terminal. (The data shift by falling edge.)
35	LM	Alternate signal input for LCD driveing.
33	SHL	Shift direction and input/output selecting terminal.
26,37	DN_2,DN_1	Data input/output terminal. Input/Output mode is determind by SHL level. Output signal change by falling edge of YSCL terminal.
1～25,38～80	COM_1～COM_{68}	LCD common driving terminal. Output signal change by falling edge of YSCL terminal.

SHL	DN_1	DN_2	COM signal shift direction
L	input	output	$COM_1 \rightarrow COM_{68}$
H	output	input	$COM_1 \leftarrow COM_{68}$

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■ FUNCTIONAL DESCRIPTION

(1)Shift register control

The 68-bit shift register is a bidirectional register.
The shift direction of 68-bit bidirectional shift register is shown below:

Control Terminal	Input	Shift Direction
SHL	L	1 → 68
	H	1 ← 68

(2)Level shifter

68-bit level shifters changes the logic operating voltage to LCD driving voltage.

(3)Voltage controller

Voltage controller output V_0～V_5 level according to display data and alternate signal LM.

(4)LCD driver output

68-bit LCD driver output following level according to display data, LM signal and $\overline{DISPOFF}$.

Display Data	LM	$\overline{DISPOFF}$	Driver Output (COM_1 to COM_{68})
H	H	H	V_0
	L	H	V_5
L	H	H	V_4
	L	H	V_1
-	-	L	V_0

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	(1)	V_{DD}	- 0.3 ～ +6.0	V
Supply Voltage	(2)	V_{DD}-V_5	-30.0 ～ +0.3	V
Supply Voltage	(2)	V_0,V_1,V_4	V_5-0.3 ～ V_{DD}+0.3	V
Input Voltage	(1)	V_{IN}	V_5-0.3 ～ V_{DD}+0.3	V
Output Voltage	(1)	V_{OUT}	V_5-0.3 ～ V_{DD}+0.3	V
Output Current	(1)	I_{OUT}	20	V
Output Current	(2)	I_{OCOM}	20	V
Power Dissipation		P_D	300	mW
Operating Temperature		Topr	-20 ～ +75	℃
Storage Temperature		Tstg	-40 ～ +125	℃

Note 1) The relation : $V_{DD} \geqq V_{SS} \geqq V_5$ must be maintained.
2) The relation : $V_{DD} \geqq V_0, V_1, V_4 \geqq V_5$ must be maintained.

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■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Ta=-20～+75℃)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}			4.5	5.0	5.5	V
LCD Driving Voltage	V_5	Recommendation		-23		-7	V
		Maximum				-3	V
LCD Driving Voltage	V_O			2.5		V_{DD}	V
Input Voltage	V_{IH}	DN_1, DN_2, YSCL, LM, SHL, $\overline{DISPOFF}$ Terminals		0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	
Output Voltage	V_{OH}	I_{OH}=-0.6mA	DN_1, DN_2 Terminals	V_{DD}-0.4			V
	V_{OL}	I_{OL}= 0.6mA				V_{SS}+0.4	
Input Leakage Current	I_{IN}	V_{IN}=V_{DD} or 0V	YSCL, LM, SHL, $\overline{DISPOFF}$			2.0	μA
	I_{IN}/o		DN_1, DN_2			5.0	
Stand-by Current	I_{DSS}	V_5=-8～-26V, V_{DD} Terminal V_{IH}=V_{DD} or V_{IL}=V_{SS}				25	μA
Output Resistance	R_{COM}	|ΔV$_{ON}$|=0.5V COM Terminal	V_5=-20V		1.1	1.8	kΩ
			V_5=-14V		1.2	2.0	
			V_5= -8V		2.0	4.0	
Operating Current (1)	I_{DS1}	V_{DD}=5V, V_{IH}=V_{DD}, V_{IL}=V_{SS} fYSCL=7.7MHz, frame f=60Hz Input "H" every 1/128duty No Load			7.0	15	μA
Operating Current (2)	I_{DS2}	V_1= -2V, V_4=-18V, V_5=-20V V_{DD}=5V, V_{IH}=V_{DD}, V_{IL}=V_{SS} fYSCL=7.7MHz, frame f=60Hz Input "H" every 1/128duty No Load			7.0	15	μA
Input Terminal Capacitance	C_I	DN_1, DN_2, YSCL, LM, SHL, $\overline{DISPOFF}$ Terminals				8.0	pF
	C_I/o	freq=1MHz DN_1, DN_2 Terminals				15.0	

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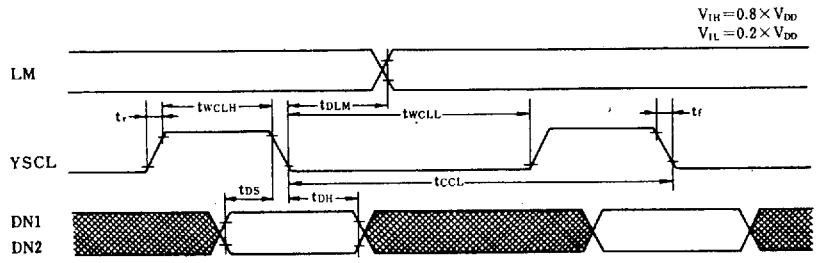
• AC Characteristics

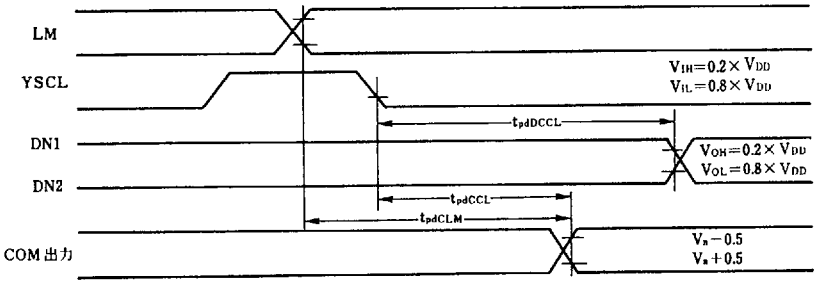
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
YSCL Cycle	t_{CCL}		500			ns
YSCL "H" Pulse Width	t_{WCLH}		70			ns
YSCL "L" Pulse Width	t_{WCLL}		330			ns
Data Set up Time	t_{DS}		100			ns
Data Hold Time	t_{DH}		10			ns
LM Transition Time	t_{DLM}		-500		500	ns
Rise Time	tr				50	ns
Fall Time	tf				50	ns

• INPUT TIMING CHART



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
YSCL fall→DN delay time	t_{pdDCCL}		30		300	ns
YSCL fall→COM delay time	t_{pdCCL}				3.0	μs
LM→COM delay time	t_{pdCLM}				3.0	μs

• OUTPUT TIMING CHART



■ LCD DRIVING SUPPLY VOLTAGE

(1)LCD Driving Bias Level

The simple method to get the LCD driving bias level is using a bleeder resistance shown below. To get the high quality display, the high accurate and high stability of bias level are required. Therefor, the smaller bleeder resistance have to use within allowable range by system power capacitance.

If the system required low power application, higher bleeder resistance and voltage follower is better way.

To avoide the LCD driving capability down, V_{DD}-V_O showld be use 0～2.5V. And if the voltage follower does not use, V_O have to connect to the V_{DD}.

(2)Notice for the Power ON/OFF

If the LCD driving voltage supply in flowing condition of logic operating voltage V_{DD}, the latch up will occur and the NJU6418 may be destroy.

Therefor, please follow below items when power is turned on and off.

- When TURN ON

Logic Operating Voltage "ON" first then LCD driving voltage "ON" or turn "ON" both voltage at same time.

- When TURN OFF

LCD Driving voltage "OFF" first then logic operating voltage "OFF" or turn off both voltage at same time.

To avoid the over current, connecting the resistance (about 100Ω) between V_5 and V_{SSH} terminal is required.

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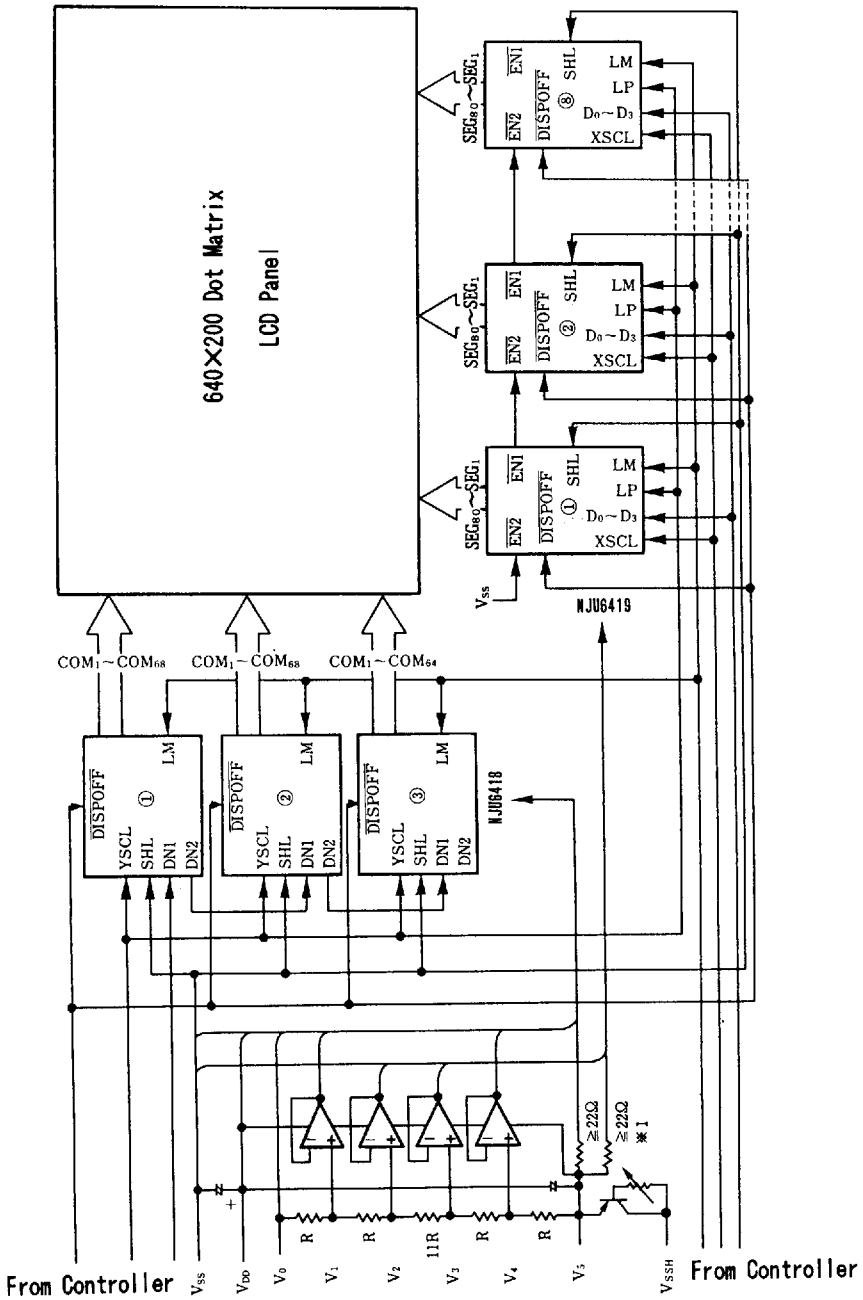
■ APPLICATION CIRCUIT

640 X 200 Dot Matrix LCD Example



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