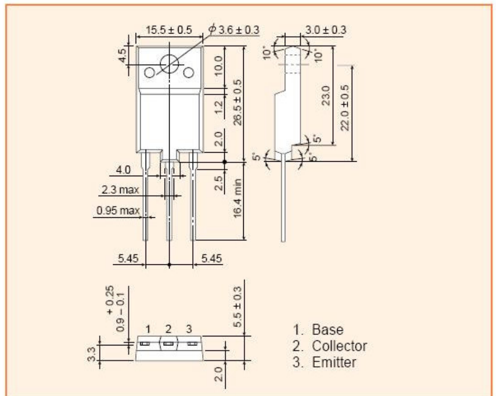
BU808DFX-LF

HIGH VOLTAGE FAST-SWITCHING NPN POWER DARLINGTON TRANSISTOR

- NPN MONOLITHIC DARLINGTON WITH INTEGRATED FREE-WHEELING DIODE
- HIGH VOLTAGE CAPABILITY (> 1400 V)
- HIGH DC CURRENT GAIN (TYP. 150)
- FULLY INSULATED PACKAGE (U.L. COMPLIANT) FOR EASY MOUNTING
- LOW BASE-DRIVE REQUIREMENTS



TO-3P(H)IS

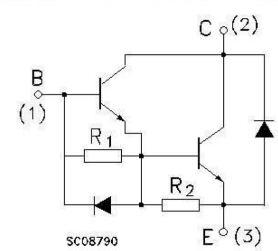
APPLICATIONS

- TV

DESCRIPTION

The BU808DFX is a NPN transistor in monolithic Darlington configuration. It is cost-effective high performance.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1400	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	10	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current (t_p < 5 ms)	6	A
P_{tot}	Total Dissipation at T_c = 25 °C	62	W
V_{isol}	Insulation Withstand Voltage (RMS) from All Three Leads to Exernal Heatsink	2500	V
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

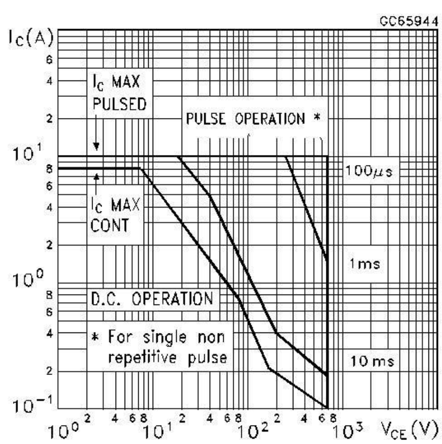
$R_{thj-case}$	Thermal Resistance Junction-case	Max	2.02	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

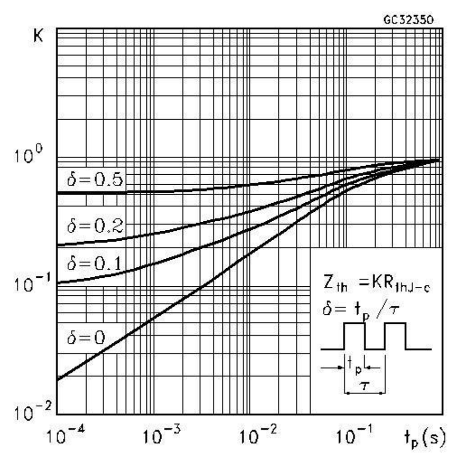
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1400 V			400	μA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	mA
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 5 A I_B = 0.5 A			1.6	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 5 A I_B = 0.5 A			2.1	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 5 V I_C = 5 A V_{CE} = 5 V T_j = 100 °C	60 20		230	
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	V_{CC} = 150 V I_C = 5 A I_{B1} = 0.5 A $V_{BE(off)}$ = -5 V		 2.3 0.2		 μs μs
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	V_{CC} = 150 V I_C = 5 A I_{B1} = 0.5 A $V_{BE(off)}$ = -5 V T_j = 100 °C		 2 0.8		 μs μs
V_F	Diode Forward Voltage	I_F = 5 A			3	V

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

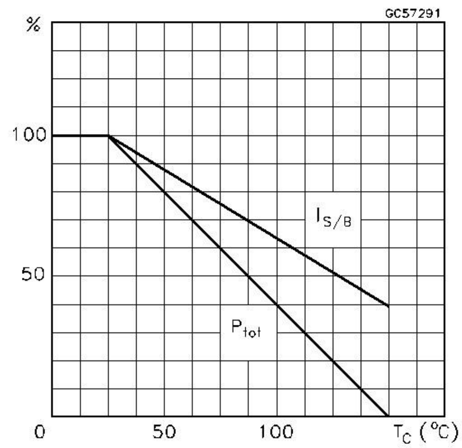
Safe Operating Area



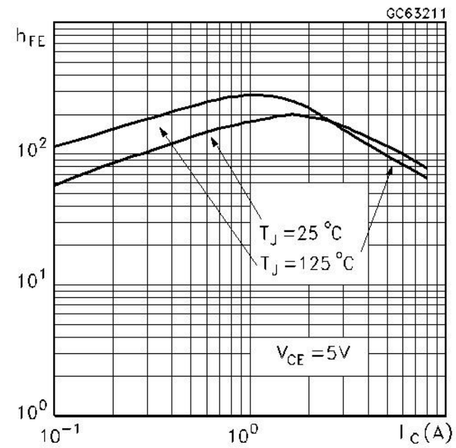
Thermal Impedance



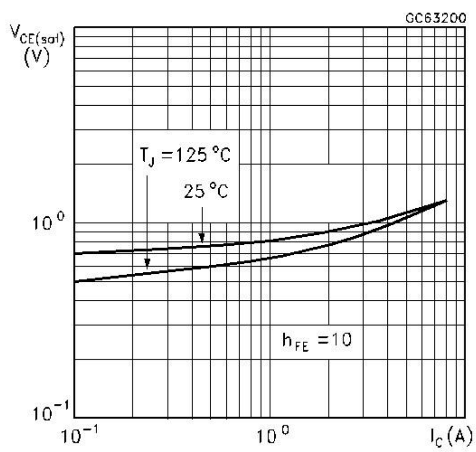
Derating Curve



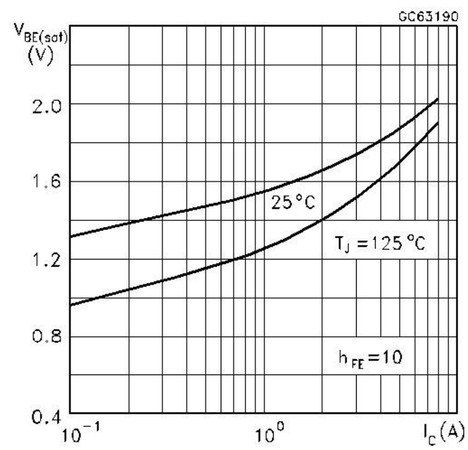
DC Current Gain



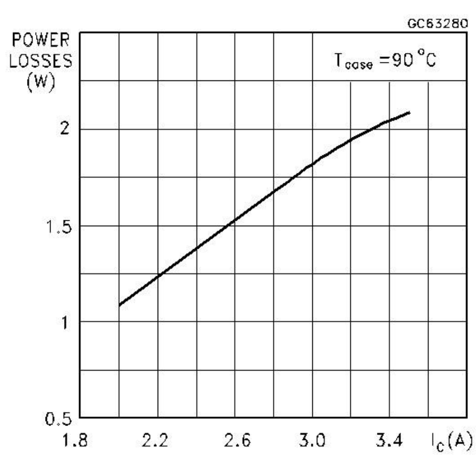
Collector Emitter Saturation Voltage



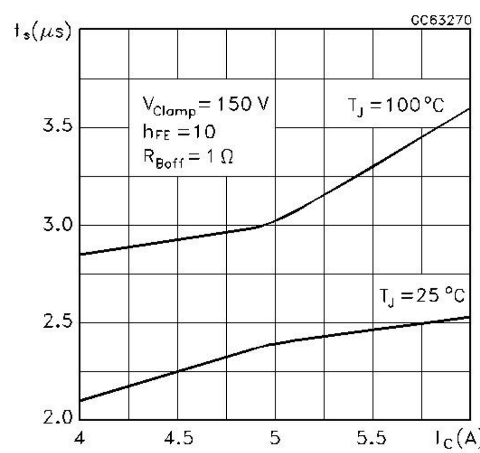
Base Emitter Saturation Voltage



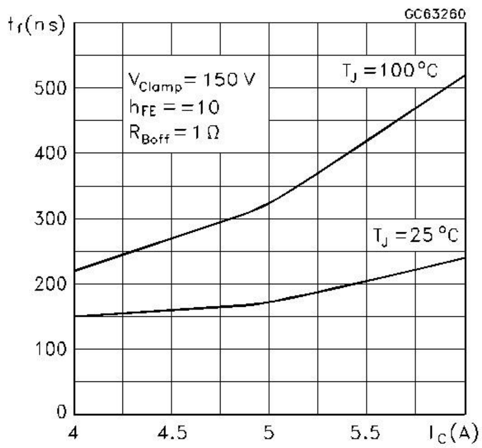
Power Losses at 16 KHz



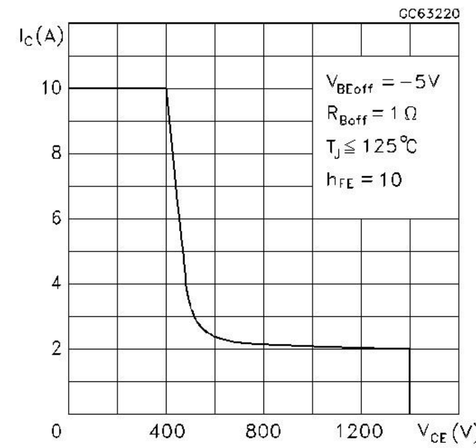
Switching Time Inductive Load at 16KHz



Switching Time Inductive Load at 16KHZ



Reverse Biased SOA



BASE DRIVE INFORMATION

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided to turn off the power transistor (retrace phase).

Most of the dissipation, in the deflection application, occurs at switch-off. Therefore it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in figure 1.

Inductance L_1 serves to control the slope of the negative base current I_{B2} to recombine the excess carrier in the collector when base current is still present, this would avoid any tailing phenomenon in the collector current.

The values of L and C are calculated from the following equations:

$$\frac{1}{2} L\,(I_C)^2 = \frac{1}{2}\,C\,(V_{CEfly})^2 \qquad \omega = 2\,\pi f = \frac{1}{\sqrt{L\,C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Inductive Load Switching Test Circuits.

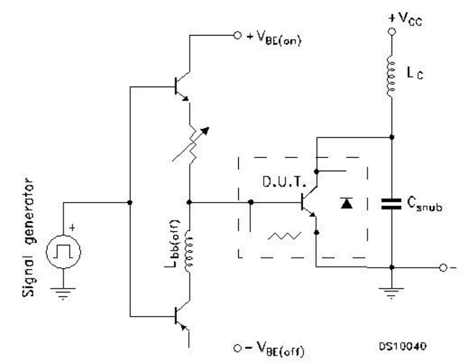


Figure 2: Switching Waveforms in a Deflection Circuit