

CS1242 Specification

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1 CS1242 DESCRIPTION

The CS1242 is precision, low power dissipation, Analog-to-Digital (A/D) converter with 24-bit resolution and up to 21-bit ENOB. The CS1242 has world wide applications in industrial process control, weigh scales, liquid/gas chemical analysis, blood analysis, smart transmitters and portable instrumentation.

1.1 CS1242 FEATURES

- 24 bits no missing code, 21 bits effective precision Analog-to-Digital converters
- Simultaneous 50Hz and 60Hz rejection (reaching -90dB)
- 0.0015% INL
- PGA gains from 1 to 128
- Single-cycle setting
- Programmable ADC data output rates
- External differential reference of 0.1V to 5V
- On-chip calibration
- Integrated compatible SPI bus interface
- Low power dissipation with 0.6mW minimum
- 3 analog single input channels and 2 differential input channels

1.2 APPLICATIONS

- Industrial process control
- Weigh scales
- liquid/gas chemical analysis
- blood analysis
- Smart transmitters
- Portable instrumentation

1.3 DESCRIPTION

The CS1242 principle block diagram is shown in Figure 1.

The CS1242 is a 24 bits Sigma-Delta analog-to-digital converter chip with high accuracy and low power dissipation. The CS1242 works from 2.7V to 5.5V power supplies with 21 bits ENOB.

The input channels are multiplexed, and analog input buffer can be selected to provide very high input impedance or direct input.

The Programmable Gain Amplifier (PGA) provides selectable gains from 1 to 128 with 18 bits ENOB at the gain of 128. The A/D conversion is performed with a second-order Sigma-Delta modulator, and programmable FIR filter that provides a simultaneous 50Hz and 60Hz notch, which effectively improve the interference immunity.

The CS1242 provides SPI compatible serial interface bus.

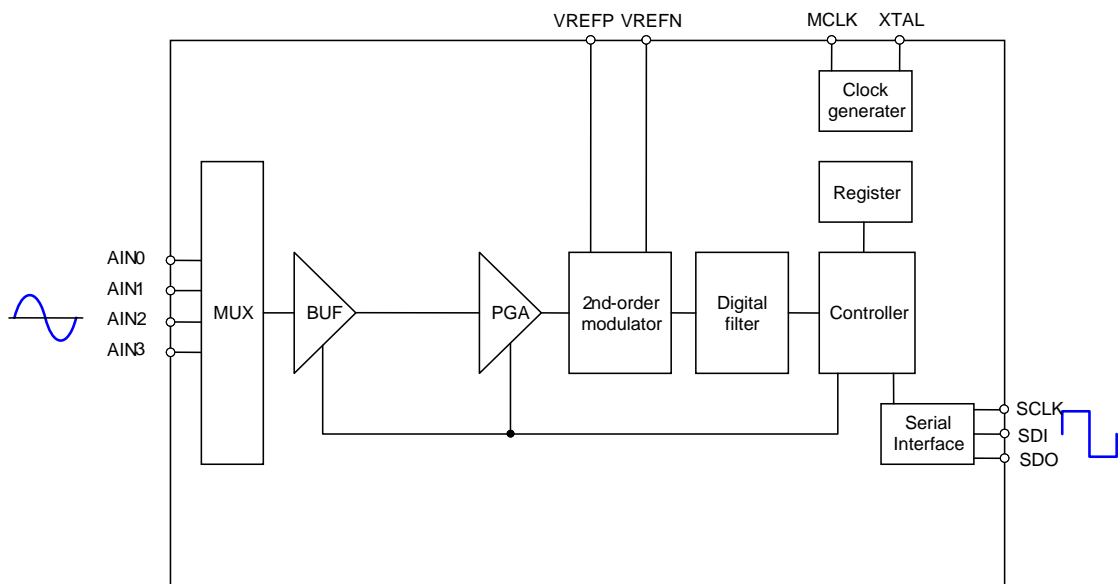


Figure 1 CS1242 Principle Block Diagram

2 CS1242 CHARACTERISTIC DESCRIPTION

2.1 ABSOLUTE MAXIMUM RATINGS

Table 1 shows the limit values of the CS1242

Table 1 Limit Value

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
AVDD to AGND	AVDD	-0.3	6	V
DVDD to DGND	DVDD	-0.3	6	V
DGND to AGND	DVGND	-0.3	0.3	V
Transient Input Current			100	mA
Continuous Input Current			10	mA
Digital Input Voltage to DGND		-0.3	DVDD+0.3	V
Digital Output Voltage to DGND		-0.3	DVDD+0.3	V
Max Junction Temperature			150	°C
Operating Temperature		-40	85	°C
Storage Temperature		-60	150	°C
Lead Temperature (Soldering, 10s)			240	°C

2.2 DIGITAL CHARACTERISTICS

Table 2 shows the digital characteristics of the CS1242.

Table 2 Digital Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
V _{IH}	0.8×DVDD		DVDD	V	
V _{IL}	DGND		0.2×DVDD	V	
V _{OH}	DVDD-0.4		DVDD+0.4	V	I _{oh} =1mA
V _{OL}	DGND		DGND+0.4	V	I _{oL} =1mA
I _{IH}			10	uA	V _I =DVDD
I _{IL}	-10			uA	V _I =DGND
f _{osc}	1		5	MHz	
t _{osc}	200		1000	ns	

NOTES: The digital interface is CMOS logic.

2.3 PINS and PACKAGING

The pins of the CS1242 are shown in Figure 2, and particular description refers to Table3.

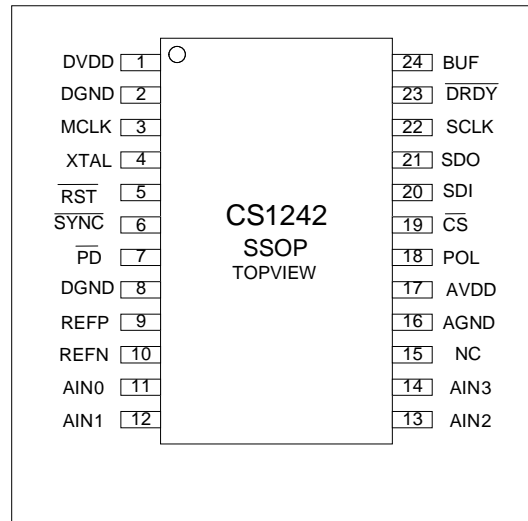


Figure 2 Pin Diagram

Table 3 Pin Description

PIN NUMBER	SYMBOL	DESCRIPTION	REMARK
1	DVDD	Digital power supply voltage, 2.7~5.25V	
2	DGND	Digital ground	
3	MCLK	Master clock input, 1~10MHz	
4	XTAL	Crystal oscillator drive pin 2	
5	RST	Active low, Chip reset pin	
6	SYNC	Active low, Sync control signal	
7	PD	Active low, Power down control	
8	DGND	Digital ground	
9	REFP	Analog reference voltage input (positive)	
10	REFN	Analog reference voltage input (negative)	
11	AIN0	Analog input 0	
12	AIN1	Analog input 1	
13	AIN2	Analog input 2	
14	AIN3	Analog input 3	
15	NC	No connection	
16	AGND	Analog ground	
17	AVDD	Analog power supply voltage, 2.7V~5.25V	
18	POL	Serial clock polarity	
19	CS	Active low, Chip select	
20	SDI	Serial data input	
21	SDO	Serial data output	
22	SCLK	Serial clock , Schmitt trigger	
23	DRDY	Active low ,Data ready	
24	BUF	Active high ,Analog input buffer enable	

The CS1242 uses SSOP-24 package, the temperature range of the CS1242 is from -40°C to +85°C, seeing the Table 4.

Table 4 Package

NAME	PACKAGE	TEMPERATURE RANGE
CS1242	SSOP-24	-40°C ~ 85°C

2.4 ELECTRICAL CHARACTERISTICS

Table 5 Electrical Characteristics (AVDD=5V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Analog input	Analog input range	Buffer OFF	AGND-0.1		AVDD+0.1	V
		Buffer ON	AGND+0.4		AVDD-1.5	V
	Full-scale input range (AIN+) - (AIN-)	RAN=0			±VREF/PGA	V
		RAN=1			±VREF/(2×PGA)	V
	Differential input impedance	Buffer OFF		5/PGA		MΩ
		Buffer ON		5		GΩ
	Bandwidth (-3dB)	f _{DATA} = 3.75Hz		1.65		Hz
		f _{DATA} = 7.50Hz		3.44		Hz
		f _{DATA} = 15.0Hz		3.7		Hz
	PGA	User-selectable gain ranges	1		128	
Input capacitance			9		pF	
Input leakage current	Modulator OFF, T = 25 °C		5		pA	
Burnout current sources			2		2uA	
System performance	Resolution	No missing codes		24		Bits
	Integral nonlinearity				±0.0015	% of FS
	Offset error			8		ppm of FS
	Offset error drift			0.02		ppm of FS/°C
	Gain error			0.005		%
	Gain error drift			0.5		ppm/°C
	Common-mode rejection	at DC	100			dB
		f _{CM} = 60Hz, f _{DATA} = 15Hz		130		dB
		f _{CM} = 50Hz, f _{DATA} = 15Hz		120		dB
	Notch rejection	f _{CM} = 60Hz, f _{DATA} = 15Hz		100		dB
f _{SIG} = 50Hz, f _{DATA} = 15Hz			100		dB	
Power-supply rejection	at DC	80	95		dB	
Voltage reference input	VREF≡REFP –REFN	RAN = 0	0.1	2.5	2.6	V
		RAN = 1	0	2.5	AVDD	V
	REFP, REFN Input range	RAN = 0	0		AVDD	V
		RAN = 1	0.1		AVDD	V
	Common-mode rejection	at DC		120		dB
		f _{VREFCM} = 60Hz		120		dB
Power-supply	Power-supply voltage	AVDD	4.75		5.25	V
	Current of analog part	PD = 0, or SLEEP		1		nA
		PGA = 1, Buffer OFF		120		uA
		PGA = 1, Buffer ON		160		uA
		PGA = 128, Buffer OFF		400		uA
		PGA = 128, Buffer ON		760		uA
	Current of digital part (DVDD = 5V)	Normal mode		2		mA
		SLEEP mode		200		uA
		Read data continuous mode		2.2		mA
		PD = 0		0.5		nA
Power dissipation	PGA = 1, Buffer OFF		11	15	mW	

Table 6 Electrical Characteristics (AVDD=3V)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog input	Analog input range	Buffer OFF	AGND-0.1		AVDD+0.1	V
		Buffer ON	AGND+0.3		AVDD-1.5	V
	Full-scale input range (AIN+) - (AIN-)	RAN=0			$\pm V_{REF}/PGA$	V
		RAN=1			$\pm V_{REF}/(2 \times PGA)$	V
	Differential input impedance	Buffer OFF		5/PGA		M Ω
		Buffer ON		5		G Ω
	Bandwidth (-3dB)	$f_{DATA} = 3.75\text{Hz}$		1.65		Hz
		$f_{DATA} = 7.50\text{Hz}$		3.44		Hz
		$f_{DATA} = 15.0\text{Hz}$		14.6		Hz
	PGA	User-selectable gain ranges	1		128	
Input capacitance			9		pF	
Input leakage current	Modulator OFF, T = 25 °C		5		pA	
Burnout current sources			2		2uA	
System performance	Resolution	No missing codes		24		Bits
	Integral nonlinearity				± 0.0015	% of FS
	Offset error			15		ppm of FS
	Offset error drift			0.04		ppm of FS/°C
	Gain error			0.01		%
	Gain error drift			1.0		ppm/°C
	Common-mode rejection	at DC	100			dB
		$f_{CM} = 60\text{Hz}, f_{DATA} = 15\text{Hz}$		130		dB
		$f_{CM} = 50\text{Hz}, f_{DATA} = 15\text{Hz}$		120		dB
	Notch rejection	$f_{CM} = 60\text{Hz}, f_{DATA} = 15\text{Hz}$		100		dB
$f_{SIG} = 50\text{Hz}, f_{DATA} = 15\text{Hz}$			100		dB	
Power-supply rejection	at DC	75	90		dB	
Voltage reference input	$V_{REF} \equiv REFP - REFN$	RAN = 0	0.1	1.25	1.30	V
		RAN = 1	0	2.5	2.6	V
	REFP, REFN input range	RAN = 0	0		AVDD	V
		RAN = 1	0.1		AVDD	V
	Common-mode rejection	at DC		120		dB
		$f_{VREFCM} = 60\text{Hz}$		120		dB
Bias current			0.65		uA	
Power-supply	Power-supply voltage	AVDD	2.7		3.3	V
	Current of analog part	$\overline{PD} = 0$, or SLEEP		1		nA
		PGA = 1, Buffer OFF		107		uA
		PGA = 1, Buffer ON		118		uA
		PGA = 128, Buffer OFF		360		uA
		PGA = 128, Buffer ON		500		uA
	Current of digital part (DVDD = 3V)	Normal mode		2		mA
		SLEEP mode		200		uA
		Read data continuous mode		2.2		mA
		$\overline{PD} = 0$		0.5		nA
Power dissipation	PGA = 1, Buffer OFF		6.6	9	mW	

2.5 TIMING CHARACTERISTICS

The timing diagram is shown in Figure 3, and particular description refers to Table7.

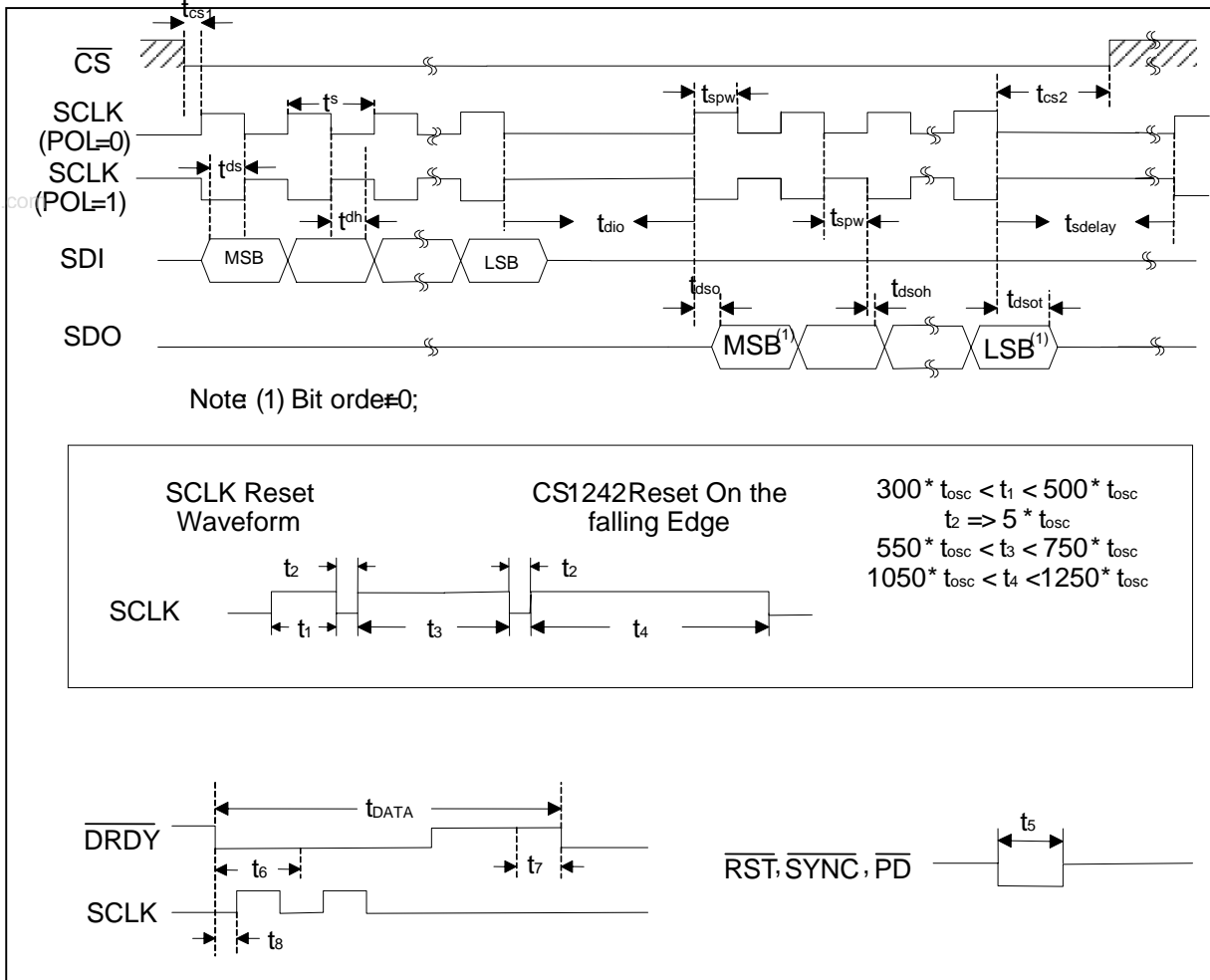


Figure 3 Timing Diagram

Table 7 Timing Table

SPEC	DESCRIPTION		MIN	MAX	UNITS
t_s	SCLK period		4		Tosc Periods
t_{spw}	SCLK Pulse Width, HIGH and LOW		200		ns
t_{cs1}	CS low to first SCLK edge, setup time		0		ns
t_{ds}	SDI data setup time (with SCLK delay)		50		ns
t_{dsh}	Valid SDI data hold time		50		ns
t_{dio}	Delay between last SCLK edge for SDI and first SCLK edge for SDO when sending the following commands: RDATA, RDATAAC, RREG, WREG		50		Tosc Periods
t_{dso}	SCLK edge to SDO new output data			50	ns
t_{dsoh}	SDO data hold time		0		
t_{dsot}	Last SCLK edge to SDO goes tri-state		6	10	Tosc Periods
t_{cs2}	CS low time after final SCLK edge		0		ns
t_{sdelay}	Final SCLK edge of one command until first edge SCLK of next command:	RREG, WREG, SYNC, SLEEP, RDATA, RDATAAC, STOPC	4		Tosc Periods
		GCALSELF, SELFOCA, OCALSYS, GCALSYS	8		DRDY periods
		CALSELF	15		DRDY Periods
		RESET (also SCLK reset or \overline{RST} pin gives off RESET command)	16		Tosc Periods
t_5	Pulse width		4		Tosc Periods
t_6	Allowed analog input change for next valid conversion			5000	Tosc Periods
t_7	DOR update, DOR data is invalid		4		Tosc Periods
t_8	First SCLK after DRDY goes low	RDATAAC mode	10		Tosc Periods
		Any other mode	0		Tosc Periods

3 CS1242 FUNCTION MODULE DESCRIPTION

3.1 INPUT MULTIPLEXER

The input multiplexer can provide for any combination of differential inputs, as shown in Figure 4.

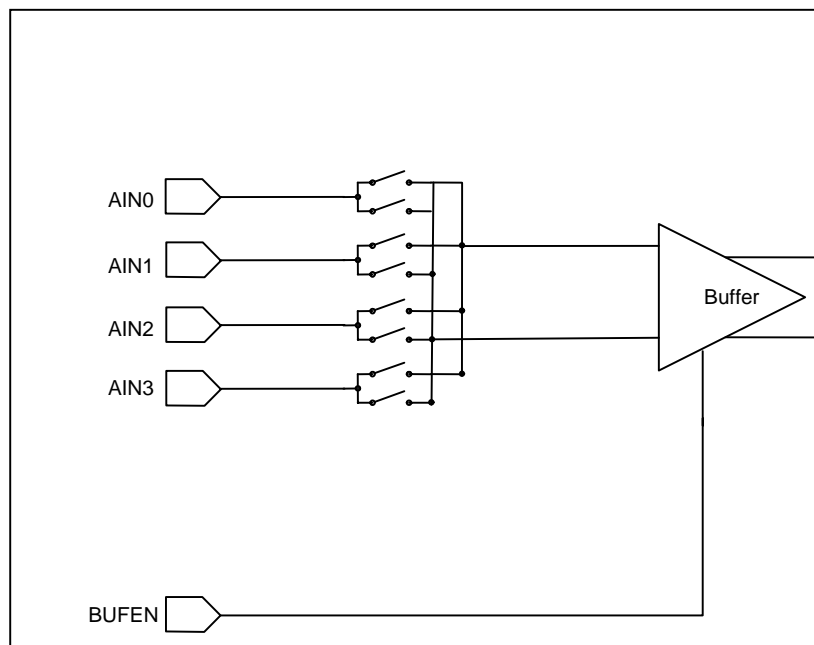


Figure 4 Schematic of Input Multiplexer

The CS1242 provides up to 2 independent differential input channels or 3 single-ended input channels. When using single-ended input, one of the four pins should be selected as the negative terminal. For example, if ADIN1 is selected as the positive (negative) differential input channel, any other channel can be selected as the negative (positive) terminal for the differential input channel.

The CS1242 can achieve stable output of the digital filter and switch the inputs in single-cycle. To minimize the switching error, MUX register should be set immediately on the falling edge of the DRDY signal.

3.2 ANALOG INPUT BUFFER

The input impedance of the CS1242 is about 5M Ω /PGA with the buffer off, but the input impedance is up to about 5G Ω with the buffer on.

The buffer can be controlled by the BUF pin and the register ACR. When the BUF bit in ACR register and BUF pin is high, the buffer is on.

The buffer will draw additional power dissipation when activated. The power depends on the PGA setting. When PGA=1, the buffer produces approximately 50uA additional current; When the PGA=128, the buffer produces approximately 150uA additional current.

The input range should be AGND+0.3V to AVDD-1.5V with the buffer on.

3.3 PROGRAMMABLE GAIN AMPLIFIER (PGA)

The Programmable Gain Amplifier (PGA) can be set to 1, 2, 4, 8, 16, 32, 64, or 128. Using PGA can improve the ENOB of the A/D converter. For example, when PGA=1, the full scale input is 5V, the converter can resolve down to 1 μ V; when PGA=128, the full scale input is 39mV, the converter can resolve down to 75nV.

3.4 MODULATOR

The Modulator of the CS1242 is a single loop, second order Sigma-Delta system. The sample frequency of the modulator is controlled by the SPEED bit in ACR register. The sample frequency is shown in Table8:

Table 8 The Sample Frequency of The Modulator

Frequency (MHz)	SPEED	ADC Sample Frequency (KHz)	Data Output Rate (Hz)			Rejection Frequency (Hz)
			DR = 00	DR = 01	DR = 10	
2.4576	0	19.200	15	7.5	3.75	50/60
	1	9.600	7.5	3.75	1.875	25/30
4.9152	0	38.400	30	15	7.5	100/120
	1	19.200	15	7.5	3.75	50/60

3.5 CALIBRATION

The CS1242 provides both self calibration and system calibration which include offset and gain calibration of the A/D converter. During calibration, the DRDY signal will be held at high, which indicates the result of the AD converter is invalid.

In order to ensure the accuracy of the A/D converter, the calibration should be performed after power-up, a change in temperature, or a change of the PGA.

At the completion of the calibration, the DRDY signal goes low, indicating the calibration is finished. The first output data of the converter after calibration is invalid because of the delay of the inside circuit, and the second output data is valid.

3.5.1 SELF CALIBRATION

Self calibration for the CS1242 is handled by the three commands: CALSELF, GCALSELF, and OCALSELF. The command CALSELF performs both offset and gain calibration. GCALSELF command performs a gain calibration, and OCALSELF performs an offset calibration, each calibration is completed in eight TDATA cycles. Performing SEFLCAL needs fifteen TDATA cycles. TDATA is the reciprocal of output speed.

During self calibration, A/D converter cuts off the external input automatically, and then connect to the inside voltage. During gain calibration, the PGA is set to 1 automatically. After the completion of the gain calibration, the PGA returns to the previous value set by the users. However, it is unnecessary to change the PGA during offset calibration.

Note: When performing calibration, if the external reference voltage is higher than AVDD-1.5V, the buffer must be closed during calibration.

3.5.2 SYSTEM CALIBRATION

System calibration corrects the offset and gain errors of the chip and the system. When performing system calibration, appropriate signal must be applied to the inputs. The commands of system calibration include OCALSYS and GCALSYS. The command OCALSYS corrects the offset error; the command GCALSYS corrects the gain error. Each calibration is finished in eight TDATA cycles.

The differential input voltage must be zero for offset calibration. The CS1242 computes the offset error for eliminating the system offset error.

The input voltage must be positive full-scale for gain calibration. The CS1242 computes the gain error for eliminating the system gain error.

3.6 EXTERNAL VOLTAGE REFERENCE

The CS1242 requires an external reference voltage which connects to REFP and REFN pins. ACR register decides the specific reference voltage value. The value can't exceed the supply voltage. The specific voltage value is shown in Table9:

Table 9 The Relation Between External Reference Voltage and RAN

RAN (ACR.2)	Power Voltage (V)	Reference Voltage (V)	Remark
0	5	≤ 2.5	
1	5	≤ 5	
0	3.0	≤ 1.25	
1	3.0	≤ 2.5	

3.7 CLOCK UNIT

The clock source for the CS1242 can be provided from external clock, a crystal, or oscillator. If the clock source is external clock, the clock is only connected to MCLK pin, and the XTAL pin is unused. If the source is a crystal, the clock circuit is shown in Figure5: (two capacitances of 10~20pF connect to the MCLK and XTAL pins)

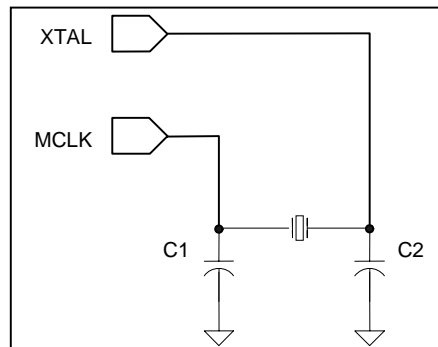


Figure 5 Schematic of Using External Crystal

3.8 DIGITAL FILTER (FIR)

The CS1242 has a programmable FIR filter which can be set to different data output rates. When the clock is 2.4576MHz, the data output rate can be set to 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the FIR filter rejects both 50Hz and 60Hz interference.

Using other clock frequency can get other data output rates, and the notch frequencies change simultaneously. For example, when the clock frequency is 3.6864MHZ, the register is under the default setting, and the data output rate is:

$$(3.6864\text{MHz}/2.4576\text{MHz}) \times 15\text{Hz} = 22.5\text{Hz}$$

Notch frequency:

$$(3.6864\text{MHz}/2.4576\text{MHz}) \times (50\text{Hz and } 60\text{Hz}) = (75\text{Hz and } 90\text{Hz})$$

3.9 SERIAL PERIPHERAL INTERFACE (SPI)

The CS1242 can communicate with external controller through the SPI bus. The CS1242 only operates in slave mode. The serial interface is a standard four-wire SPI interface, including CS, SCLK, SDI, SDO, and an additional clock polarity control pin POL. The bus supports both serial clock polarities controlled by POL pin.

3.9.1 CHIP SELECT (CS)

Before communicating with the CS1242, the external controller must send the chip select (CS) signal to the chip. During communication, the CS signal must be maintained at low. When the CS signal is high, the entire SPI is reset. CS can be hard-wired low, the SPI bus can work in the three-wire mode which fits for communicating with external controller.

3.9.2 SERIAL CLOCK (SCLK)

The serial clock features a Schmitt-triggered input, which is used for sampling the SDI and SDO signals. The SCLK must be very clean to prevent the sample error. If the SCLK doesn't appear in three DRDY cycles, the SPI bus is reset on next SCLK and starts a new communication cycle. A special waveform can reset the entire chip. See the RESET chapter for more information.

3.9.3 CLOCK POLARITY (POL)

The POL pin controls the polarity of serial clock (SCLK). When POL is low, the data is sampled on the falling edge of the SCLK. If there is no clock pulse, the SCLK should be kept at low. When the POL is high, the data is sampled on the rising edge of the SCLK. If there is no clock pulse, the SCLK should be kept at high.

3.9.4 DATA INPUT (SDI) and DATA OUTPUT (SDO)

The data input pin (SDI) and the data output pin (SDO) receive and send data. The SDO is high impedance when unused, allowing SDI and SDO to be connected together and driven by a bidirectional bus. Under this situation, the command RDATAAC should not be sent to the CS1242, because stopping the RDATAAC mode requires the command STOPC or RESET. Under RDATAAC mode, the bidirectional bus is busy sending data, so the command STOPC or RESET can not be sent to the CS1242 through the bus to stop the RDATAAC mode. However, if the data from SDO includes the command STOPC or RESET, SDI will detect the command, and the RDATAAC mode will be stopped.

3.10 DATA READY (DRDY)

The DRDY signal is used for indicating the status of data registers. When the new data in the data output register (DOR) is ready, the DRDY signal goes low. After a read operation, the DRDY signal goes high. When the DOR register is ready to update, the DRDY goes high, which indicates that the data in DOR can't be read.

The status of DRDY also can be got from the seventh bit of ACR register.

3.11 SYNCHRONIZATION (SYNC)

Synchronization can be achieved through SYNC pin or SYNC command. The digital circuit will be reset on the falling edge of the SYNC signal when using the SYNC pin. While the SYNC is low, the serial interface is inactivated. While the SYNC is high, the digital circuit releases from the reset status, synchronization occurs on the rising edge of next system clock.

When using the command SYNC to achieve synchronization, the digital filter is reset on the edge of the last SCLK pulse, the modulator will be held at RESET status until the next edge of SCLK is detected. Synchronization occurs on the rising edge of the system clock in the first SCLK after SYNC command.

3.12 POWER-UP RESET and CHIP RESET

The power-on reset circuit is designed to reset the CS1242 automatically after power-up.

The CS1242 can be reset through three methods when the CS1242 is working: pulling the RST pin down to low, sending RESET command, or sending specific waveform on the SCLK (the SCLK RESET waveform, as shown in the Timing Diagram of the CS1242).

4 CS1242 REGISTER DESCRIPTION

The CS1242 configures the working mode through a series of control registers, which are used for controlling data format, MUX setting, data rate, calibration, etc.

4.1 REGISTER LIST

Registers list is shown in Table 10:

Table 10 Registers List

Address	Register	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00H	SETUP	ID3	ID2	ID1	ID0	Reserved	PGA2	PGA1	PGA0
01H	MUX	PS3	PS2	PS1	PS0	NS3	NS2	NS1	NS0
02H	ACR	$\overline{\text{DRDY}}$	$\text{U}/\overline{\text{B}}$	SPEED	BUF	BITOR	RAN	DR1	DR0
03H	ODAC	Reserved	CHSEL	ISET1	ISET0	Reserved	Reserved	Reserved	Reserved
04H	Reserved								
05H	Reserved								
06H	Reserved								
07H	OCC0	OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
08H	OCC1	OCC15	OCC14	OCC13	OCC12	OCC11	OCC10	OCC09	OCC08
09H	OCC2	OCC23	OCC22	OCC21	OCC20	OCC19	OCC18	OCC17	OCC16
0AH	GCC0	GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
0BH	GCC1	GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
0CH	GCC2	GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
0DH	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
0EH	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0FH	DOR0	DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

4.2 DETAILED REGISTER DEFINITIONS

SETUP Register (Address = 00H, Reset Value = xxxx0000) PGA Control

MSB				LSB			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	ID2	ID1	ID0	Reserved	PGA2	PGA1	PGA0
SETUP. 7-4 : Code of the chip, factory programmed bits SETUP. 3 : Reserved SETUP. 2-0 : PGA2/PGA1/PGA0, Programmable Gain Amplifier Gain Selection 000 = 1 (Default) 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = 64 111 = 128							

Multiplexer Control Register (MUX) (Address = 01H, Reset Value = 01H) Input Channel Select

MSB							LSB	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
PS3	PS2	PS1	PS0	NS3	NS2	NS1	NS0	
SETUP. 7-4 : PS3~0, Positive Channel Selection 0000 = ADIN0 (Default) 0001 = ADIN1 0010 = ADIN2 0011 = ADIN3 Rest = Reserved								
SETUP. 3-0 : NS3~0, Negative Channel Selection 0000 = ADIN0 0001 = ADIN1 (Default) 0010 = ADIN2 0011 = ADIN3 Rest = Reserved								

Analog Control Register (ACR) (Address = 02H, Reset Value = x0H) Analog Control

MSB							LSB	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
$\overline{\text{DRDY}}$	U/ $\overline{\text{B}}$	SPEED	BUF	BITOR	RAN	DR1	DR0	
SETUP.7 : $\overline{\text{DRDY}}$ (Data Ready), Read Only, Bit 7 duplicates the state of the $\overline{\text{DRDY}}$ signal.								
SETUP.6 : U/ $\overline{\text{B}}$, Data Format 0 = Bipolar (Default); <i>+FSR Output 0x7FFFFFFH, ZERO = 0x00000H, -FSR = 0x800000H;</i> 1 = Unipolar; <i>+FSR Output 0xFFFFFFFFH, ZERO = 0x00000H, -FSR = 0x000000H;</i>								
SETUP.5 : SPEED, Modulator Clock Speed Control 0 = fosc/128 (Default) 1 = fosc/256;								
SETUP.4 : BUF (Buffer Enable) 0 = BUF Disabled (Default); 1 = BUF Enabled;								
SETUP.3 : BITOR, Set Bit Order For Output Data 0 = Most Significant Bit Transmitted First (Default); 1 = Least Significant Bit Transmitted First;								
SETUP.2 : RAN, Range Selection 0 = Full-Scale Input Range Equal to $\pm V_{\text{REF}}$ (default); 1 = Full-Scale Input Range Equal to $\pm V_{\text{REF}} / 2$;								
SETUP.1-0 : DR1/DR0, (Data Rate) 00 = 15Hz (Default); 01 = 7.5Hz; 10 = 3.75Hz; 11 = Reserved								

ODAC REGISTER (Address = 03H, Reset Value = 00H) Offset DAC Set

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Nullity	CHSEL	ISEL1	ISET1	Nullity	Nullity	Nullity	Nullity
ISET11-0 : Analog Bias Current Select, 00 = The Bias Current is 10uA (Default), 01 or 10 = Bias Current Increase by 25%, 11 = Bias Current Increase by 50%, When using a higher clock frequency, increasing the analog bias current will help improve the performance of the CS1242.							
CHSEL : Chopper-modulation Select 0 = Chopper frequency is half the sample frequency of modulator, when PGA=1 to 128 is enabled (Default); 1 = Chopper frequency is equal to the sample frequency of modulator, when PGA = 2 to 128 is enabled; CHSEL is set to 0 in normal state. However, in certain state (the state relates to the application circuit), high frequency noise will couple to the low frequency signal, CHSEL can be set to 1, and this will cause offset and noise increase.							

Offset Calibration Coefficient Register 0 (OCC0) (Address = 07H, Reset Value = 00H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
Offset calibration coefficient is composed of OCC0, OCC1 and OCC2. OCC23-00(totally 24 bits, OCC23 is MSB, OCC00 is LSB) is used for calibrating the offset error.							

Offset Calibration Coefficient Register 1 (OCC1) (Address = 08H, Reset Value = 00H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC15	OCC14	OCC13	OCC12	OCC11	OCC10	OCC09	OCC08
Offset calibration coefficient is composed of OCC0, OCC1 and OCC2. OCC23-00(totally 24 bits, OCC23 is MSB, OCC00 is LSB) is used for calibrating the offset error.							

Offset Calibration Coefficient Register 2 (OCC2) (Address = 09H, Reset Value = 00H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC23	OCC22	OCC21	OCC20	OCC19	OCC18	OCC17	OCC16
Offset calibration coefficient is composed of OCC0, OCC1 and OCC2. OCC23-00(totally 24 bits, OCC23 is MSB, OCC00 is LSB) is used for calibrating the offset error.							

Gain Calibration Coefficient Register 0 (GCC0) (Address = 0AH, Reset Value = 59H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
Gain calibration coefficient is composed of GCC0, GCC1 and GCC2. GCC23-00(totally 24 bits, GCC23 is MSB, GCC00 is LSB) is used for calibrating the gain error.							

Gain Calibration Coefficient Register 1 (GCC1) (Address = 0BH, Reset Value = 55H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
Gain calibration coefficient is composed of GCC0, GCC1 and GCC2. GCC23-00(totally 24 bits, GCC23 is MSB, GCC00 is LSB) is used for calibrating the gain error.							

Gain Calibration Coefficient Register 2 (GCC2) (Address = 0CH, Reset Value = 55H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
Gain calibration coefficient is composed of GCC0, GCC1 and GCC2. GCC23-00(totally 24 bits, GCC23 is MSB, GCC00 is LSB) is used for calibrating the gain error.							

Data Output Register 2 (DOR2) (Address = 0DH, Reset Value = 00H) ADC Data

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR 23	DOR22	DOR 21	DOR 20	F DOR 19	DOR 18	DOR 17	DOR 16
ADC data is composed of DOR0, DOR1 and DOR2. DOR23-00(totally 24 bits, DOR23 is MSB, DOR00 is LSB)							

Data Output Register 1 (DOR1) (Address = 0EH, Reset Value = 00H) ADC Data

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
ADC data is composed of DOR0, DOR1 and DOR2. DOR23-00(totally 24 bits, DOR23 is MSB, DOR00 is LSB)							

Data Output Register 0 (DOR0) (Address = 0FH, Reset Value = 00H) ADC Data

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00
ADC data is composed of DOR0, DOR1 and DOR2. DOR23-00(totally 24 bits, DOR23 is MSB, DOR00 is LSB)							

5 CS1242 COMMAND DESCRIPTION

The CS1242 has a series of commands, which control the working mode, working speed, calibration, etc. Some of the commands are single (such as RESET); some need operands (such as WREG, etc).

Operands:

n = Amount (0-127)

r = Register (0-15)

x = Arbitrary value

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5.1 CS1242 COMMAND LIST

Commands aggregate of the CS1242 is shown in Table 11.

Table 11 Commands Table

COMMANDS	DESCRIPTION	OPERATE CODE	OPERANDS
RDATA	Read data from DOR register	0000 0001 (01 _H)	--
RDATA C	Read data from DOR register continuously	0000 0011 (03 _H)	--
STOPC	Stop read data from DOR register continuously	0000 1111 (0F _H)	--
RREG	Read value from "rrrr" register	0001 r r r r (1X _H)	xxxx_nnnn
WREG	Write value to "rrrr" register	0101 r r r r (5X _H)	xxxx_nnnn
CALSELF	Self offset and gain calibration	1111 0000 (F0 _H)	
OCALSELF	Self offset calibration	1111 0001 (F1 _H)	
GCALSELF	Self gain calibration	1111 0010 (F2 _H)	
OCALSYS	System offset calibration	1111 0011 (F3 _H)	
GCALSYS	System gain calibration	1111 0100 (F4 _H)	
WAKEUP	Wake up system from sleep mode	1111 1011 (FB _H)	
SYNC	Sync DRDY	1111 1100 (FC _H)	
SLEEP	Put in sleep mode	1111 1101 (FD _H)	
RESET	Reset to power-up value	1111 1110 (FE _H)	
NOTE: The received data format is always MSB first; the BITOR bit in ACR register sets the data out format.			

5.2 DETAILED COMMANDS DESCRIPTION

RDATA—Read Data from Data Output Register (DOR)

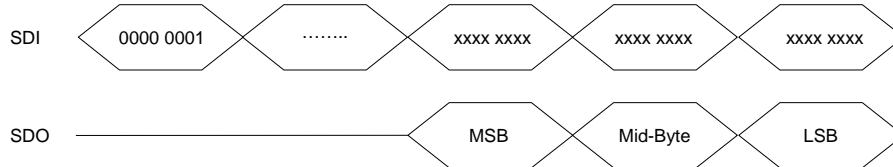
Description: Read the most recent conversion single data from the data output register (DOR). This is a 24-bit value.

Operands: none

Byte: 1

Encoding: 0000 0001

Data transmit sequence:



RDATA C—Read Data Continuous from Data Output Register (DOR)

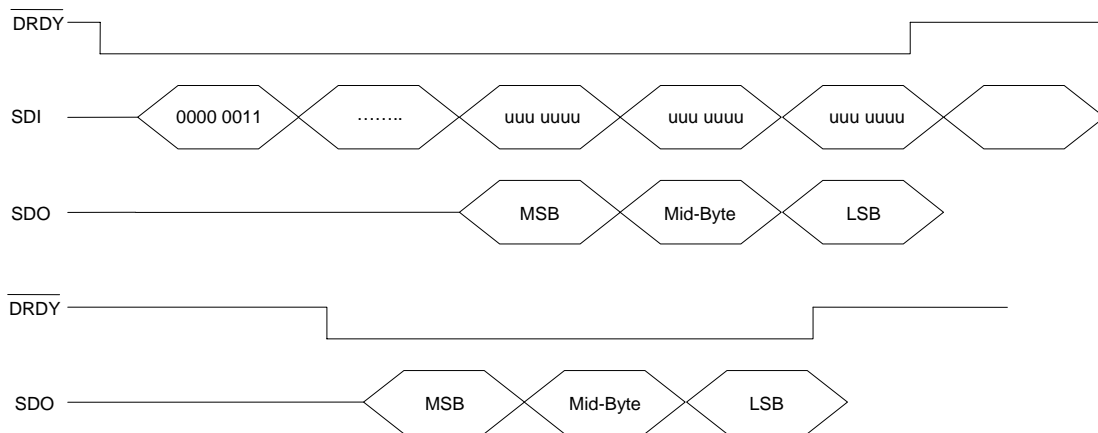
Description: Read data continuous mode enables the continuous output of new data on each DRDY signal period, and don't need to send the command RDATA when DRDY goes low. This mode can be terminated by either the STOPC command or the RESET command. After the DRDY goes low, it needs more than 10 t_{OSC} to execute this command.

Operands: none

Byte: 1

Encoding: 0000 0011

Data transmit sequence:



STOPC—Stop Continuous Data Output Mode

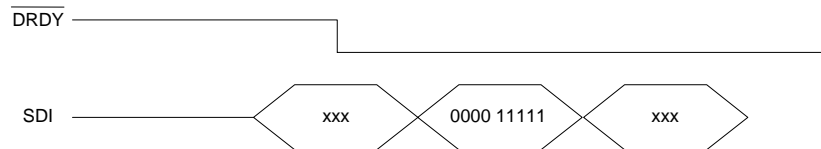
Description: Stop the continuous data output mode. The command is sent after $\overline{\text{DRDY}}$ goes low.

Operands: none

Byte: 1

Encoding: 0000 1111

Data transmit sequence:



RREG—Read from Register

Description: Output the data from up to 16 registers, the starting register address is decided by operand in command. The number of registers read will be one plus the second byte. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

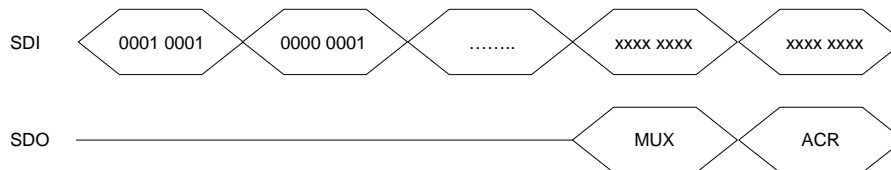
Operands: r, n

Byte: 2

Encoding: 0001 rrrr xxxx nnnn

Data transmit sequence:

Read 2 registers, starting with the register 01H (MUX)



WREG—Write to Register

Description: Write multi-data to registers. The starting register address is decided by operand in command. The number of registers that will be written is one plus the value of the second byte.

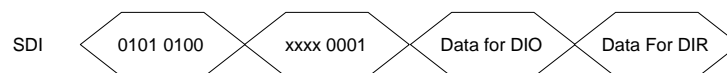
Operands: r, n

Byte: 2

Encoding: 0101 rrrr xxxx nnnn

Data transmit sequence:

Write data to two registers, starting with the register 04H (DIO)



CALSELF—Offset and Gain Self Calibration

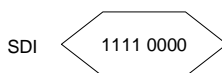
Description: Perform offset and gain self calibration. The OCC register and the GCC register are updated after the operation.

Operands: none

Byte: 1

Encoding: 1111 0000

Data transmit sequence:



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OCALSELF—Offset Self Calibration

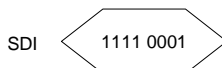
Description: Perform offset self calibration. The OCC register is updated after this operation.

Operands: none

Byte: 1

Encoding: 1111 0011

Data transmit sequence:

**SLFGCAL—Gain Self Calibration**

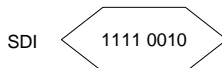
Description: Perform gain self calibration. The GCC register is updated after this operation.

Operands: none

Byte: 1

Encoding: 1111 0010

Data transmit sequence:

**OCALSYS—System Offset Calibration**

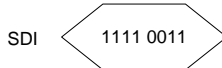
Description: Perform system offset calibration. For a system offset calibration, the input should be set to 0V, and the CS1242 computes the OCC value that will compensate for offset errors. The OCC value is updated after this operation. 0V signal must be applied to the analog inputs, and the OCC register is updated automatically.

Operands: none

Byte: 1

Encoding: 1111 0011

Data transmit sequence:



GCALSYS—System Gain Calibration

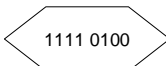
Description: Perform system gain calibration. For a system gain calibration, the input should be set to the full-scale voltage and the CS1242 computes the GCC value that will compensate for gain errors. GCC register value is updated after this operation. Full-scale voltage must be applied to the analog inputs, and the GCC register is updated automatically.

Operands: none

Byte: 1

Encoding: 1111 0100

Data transmit sequence:

SDI 

WAKEUP—Wake Up from The Sleep Mode

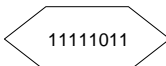
Description: Wake up the CS1242 from the sleep mode

Operands: none

Byte: 1

Encoding: 1111 1011

Data transmit sequence:

SDI 

SYNC—Synchronize DRDY

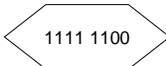
Description: Synchronize the data of the CS1242

Operands: none

Byte: 1

Encoding: 1111 1100

Data transmit sequence:

SDI 

SLEEP—Sleep Mode

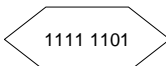
Description: Put the CS1242 into sleep mode. Use WAKEUP command to wake up from sleep mode.

Operands: none

Byte: 1

Encoding: 1111 1101

Data transmit sequence:

SDI 

RESET—Reset to Power-up Value

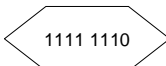
Description: Restore the registers to their power-up values. This command will also stop the RDATAAC command.

Operands: none

Byte: 1

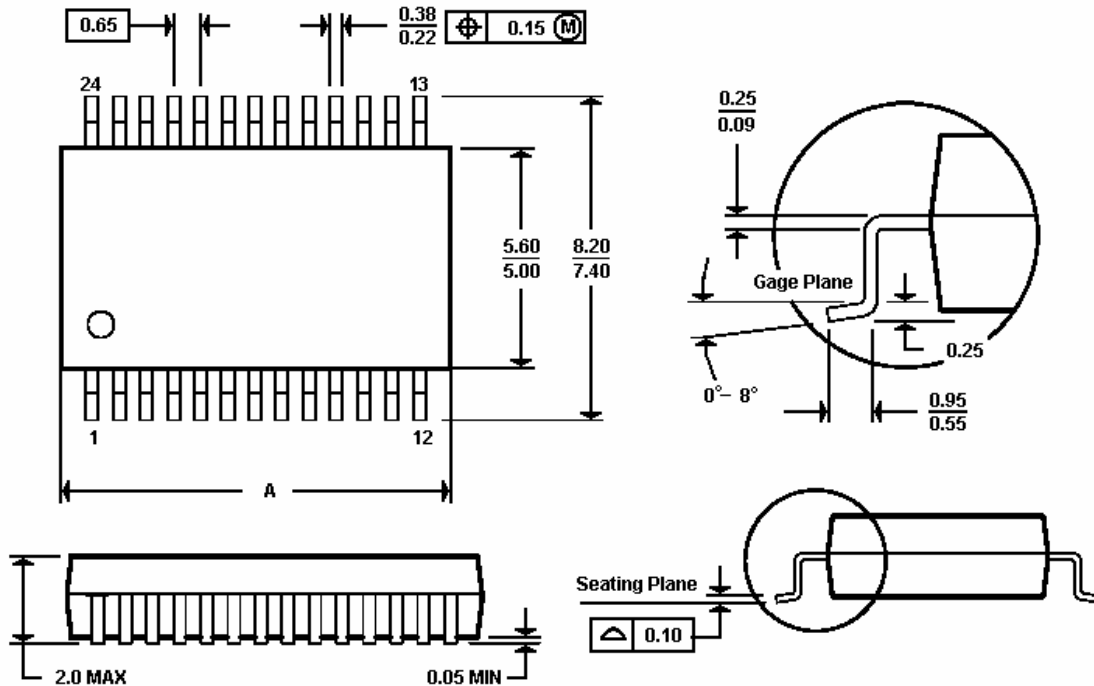
Encoding: 1111 1110

Data transmit sequence:

SDI 

6 CS1242 PACKAGE

The CS1242 uses SSOP24 packaging, shown in the following figure.



NOTES :

- A. All linear dimensions are in millimeters
- B. This drawing is subject to change without notice
- C. Body dimensions do not include mold flash or protrusion nont to exceed 0.15
- D. Falls within JEDEC MO-150

DIM	PINS	
	24	28
A MAX	9.50	10.50
A MIN	7.90	9.90