AUTOMOTIVE GRADE

CS8140/1

5V, 500mA Linear Regulator with ENABLE, $\overline{\text{RESET}}$, and Watchdog

Description

The CS8140 is a 5V Watchdog Regulator with protection circuitry and three logic control functions that allow a microprocessor to control its own power supply. The CS8140 is designed for use in automotive, switch mode power supply post regulator, and battery powered systems.

Basic regulator performance characteristics include a low noise, low drift, 5V ± 4% precision output voltage with low dropout voltage (1.25V @ I_{OUT} = 500mA) and low quiescent current (7mA @ I_{OUT} = 500mA). On board short circuit, thermal, and overvoltage protection make it possible to use this regulator in particularly harsh operating environments.

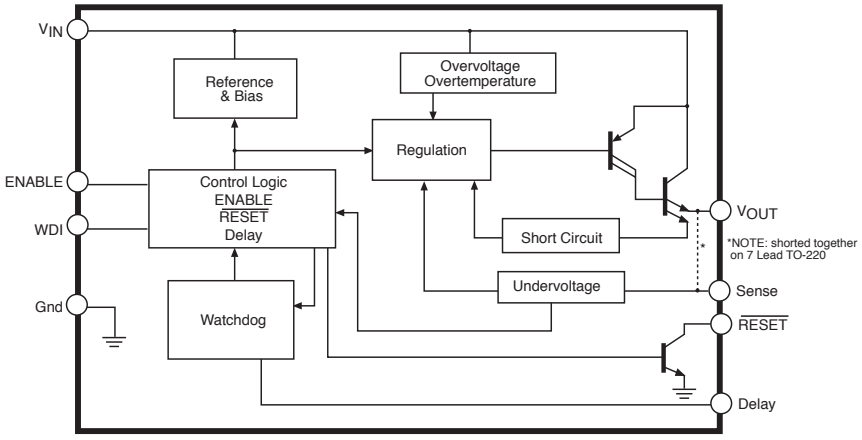
The Watchdog logic function monitors an input signal (WDI) from the microprocessor or other signal source. When the signal frequency moves outside externally programmable window limits, a $\overline{\text{RESET}}$ signal is generated ($\overline{\text{RESET}}$). An external capacitor (C_{DELAY}) programs the watchdog window frequency limits as well as the power on reset (POR) and $\overline{\text{RESET}}$ delay.

The $\overline{\text{RESET}}$ function is activated by any of three conditions: the watchdog signal moves outside of its preset limits; the output voltage drops out of regulation by more than 4.5%; or the IC is in its power up sequence. The $\overline{\text{RESET}}$ signal is independent of V_{IN} and reliable down to V_{OUT} = 1V.

In conjunction with the Watchdog, the ENABLE function controls the regulator's power consumption. The CS8140's output stage and its attendant circuitry are enabled by setting the ENABLE lead high. The regulator goes into sleep mode (I_{OUT} = 250µA) when the ENABLE lead goes low and the watchdog signal moves outside its preset window limits. This unique combination of control functions in the CS8140 gives the microprocessor control over its own power down sequence: i.e. it gives the microprocessor the flexibility to perform housekeeping functions before it powers down.

The CS8141 has the same features as the CS8140, except that the CS8141 only responds to input signals (WDI) which are below the preset watchdog frequency threshold.

Block Diagram

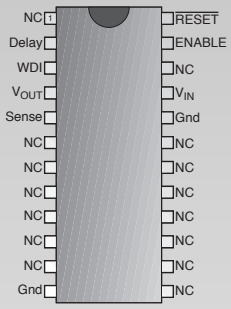


Features

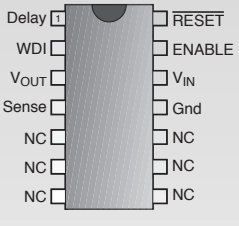
- 5V ± 4%, 500mA Output Voltage
- µP Compatible Control Functions
  - Watchdog
  - $\overline{\text{RESET}}$
  - ENABLE
- Low Dropout Voltage (1.25V @ 500mA)
- Low Quiescent Current (7mA @ 500mA)
- Low Noise, Low Drift
- Low Current SLEEP Mode (I_Q = 250µA)
- Fault Protection
  - Thermal Shutdown
  - Short Circuit
  - 60V Peak Transient Voltage

Package Options

24 Lead SOIC Wide

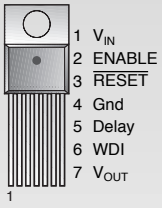


14 Lead PDIP



7 Lead TO-220

Tab (Gnd)



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Absolute Maximum Ratings

Input Voltage
- Operating Range ..... -0.5 to +26V
- Peak Transient Voltage (46V Load Dump @ 14V V_{BAT}) 60V
- Electrostatic Discharge (Human Body Model) 4kV

WDI Input Signal Range ..... -0.3 to +7V
Internal Power Dissipation ..... Internally limited
Junction Temperature Range (TJ) ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Soldering
- Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
- Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

ENABLE ..... -0.3V to V_{IN}

Electrical Characteristics: $7V \le V_{IN} \le 26V$, $5mA \le I_{OUT} \le 500mA$, $-40^{\circ}C \le T_J \le +150^{\circ}C$, $-40^{\circ}C \le T_A \le 125^{\circ}C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage (V_{OUT})					
Output Voltage, V_{OUT}	$7V \le V_{IN} \le 26V$ $5mA < I_{OUT} < 500mA$	4.8	5.0	5.2	V
Dropout Voltage (V_{IN} - V_{OUT})	$I_{OUT} = 500mA$		1.25	1.50	V
Line Regulation	$I_{OUT} = 50mA$, $7V \le V_{IN} \le 26V$		5	25	mV
Load Regulation	$V_{IN} = 14V$, $50mA \le I_{OUT} \le 500mA$		5	80	mV
Output Impedance, R_{OUT}	500mA DC and 10mA AC, $100Hz \le f \le 10kHz$		200		mΩ
Quiescent Current, (I_Q)					
Active Mode	$0 \le I_{OUT} \le 500mA$, $7V \le V_{IN} \le 26V$		7.00	15.00	mA
Sleep Mode	$I_{OUT} = 0mA$, $V_{IN} = 13V$, ENABLE = 0V		0.25	0.50	mA
Ripple Rejection	$7 \le V_{IN} \le 17V$, $I_{OUT} = 250mA$, $f = 120Hz$	60	75		dB
Current Limit		700	1200	2000	mA
Thermal Shutdown		150	180		°C
Overvoltage Shutdown	$V_{OUT} < 1V$	30	34	38	V
■ ENABLE					
Threshold					
HIGH	$V_{OUT} \ge 0.5V$, ($V_{OUT(ON)}$)		4.05	4.50	V
LOW	$V_{OUT} < 0.5V$, ($V_{OUT(OFF)}$)	3.50	3.95		V
Threshold Hysteresis	(HIGH - LOW)		100		mV

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ $\overline{\text{RESET}}$					
Threshold					
HIGH $V_{R(HI)}$	V_{OUT} increasing	4.65	4.90	V_{OUT} - 0.05	V
LOW $V_{R(LOW)}$	V_{OUT} decreasing	4.50	4.70	4.90	V
Threshold Hysteresis(V_{RH})	(HIGH - LOW)	150	200	250	mV
Reset Output Leakage	$V_{OUT} \geq V_{R(HI)}$			25	µA
$\overline{\text{RESET}}$ = HIGH					
Output Voltage					
Low($V_{L(LOW)}$)	$1V \leq V_{OUT} \leq V_{R(LOW)}$ Rp = 2.7kΩ*		0.1	0.4	V
Low (V_{Rpeak})	V_{OUT}, Power up, Power down		0.6	1.0	V
Delay Times	C_{DELAY} = 0.1µF				
t_{POR}		30.0	47.5	65.0	ms
$t_{WDI(\overline{\text{RESET}})}$		0.5	1.0	1.5	ms
■ Watchdog					
Input Voltage					
HIGH		2.0			V
LOW				0.8	V
Input Current	WDI ≤ V_{OUT}		0	10	µA
Threshold Frequency	C_{DELAY} = 0.1µF				
$f_{WDI_{LOWER}}$		64	77	96	Hz
$f_{WDI(UPPER)}$**		218	262	326	Hz

* R_P is connected to $\overline{\text{RESET}}$ and V_{OUT}.

** CS8140 only

To observe safe operating junction temperature, low duty cycle pulse testing is used on tests where applicable.

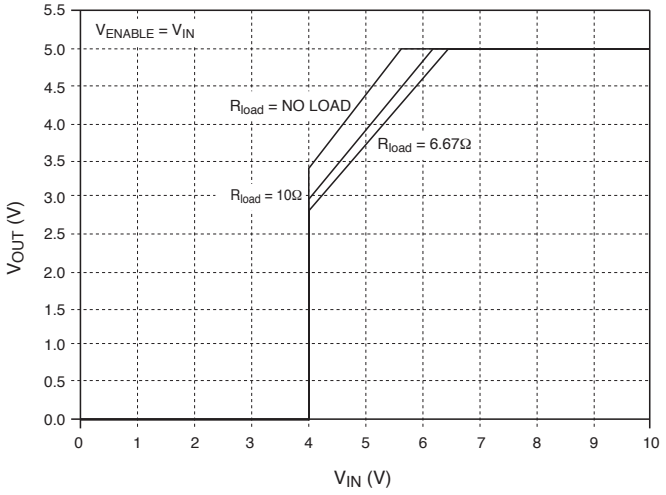
Package Lead Description

Package Lead #			Lead Symbol	Function
7 Lead TO-220	24 Lead * SOIC Wide	14 Lead PDIP		
1	21	12	V_{IN}	Supply voltage to IC, usually direct from the battery.
2	23	13	ENABLE	CMOS compatible logical input. V_{OUT} is disabled when ENABLE is LOW and WDI is beyond its preset limits.
3	24	14	$\overline{\text{RESET}}$	CMOS compatible output lead. $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops below 4.5% of its typical value for more than 2µs or WDI signal falls outside it's window limits.
4	12, 20	11	Gnd	Ground connection.
5	2	1	Delay	Timing capacitor for Watchdog and $\overline{\text{RESET}}$ functions.
6	3	2	WDI	CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming digital pulse train. The signal is usually generated by the system microprocessor.
7	4	3	V_{OUT}	Regulated output voltage, 5V (typ).
N/A	5	4	Sense	Kelvin connection which allows remote sensing of output voltage for improved regulation.
	1,6-11,13-19,22	5-10	NC	No connection.

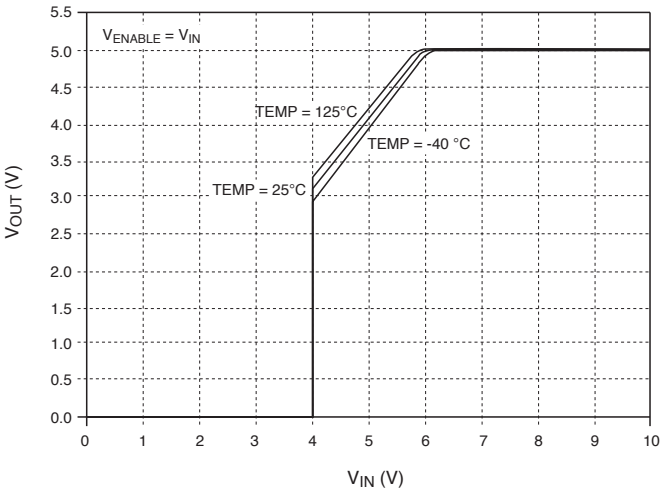
* The CS8141 uses a fused lead package. Leads 6-8 and 17-19 are fused together through the lead frame. These leads are electrically connected to IC ground and should be connected to system ground for a good thermal connection.

Typical Performance Characteristics

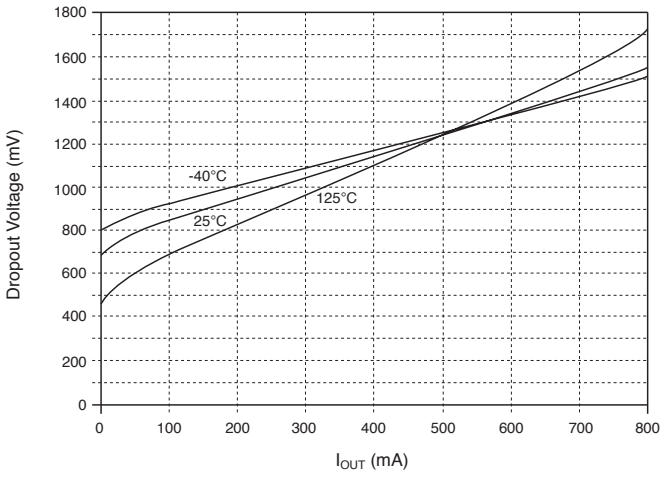
V_{OUT} vs. V_{IN} over R_{LOAD}; T = 25°C



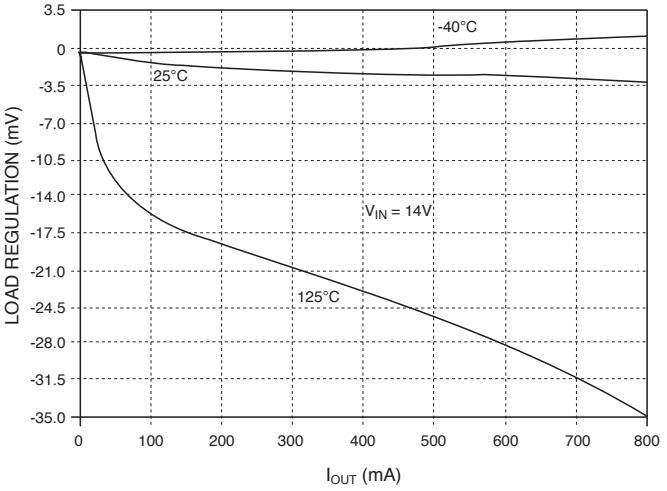
V_{OUT} vs. V_{IN} over Temperature; R_{LOAD} = 25Ω



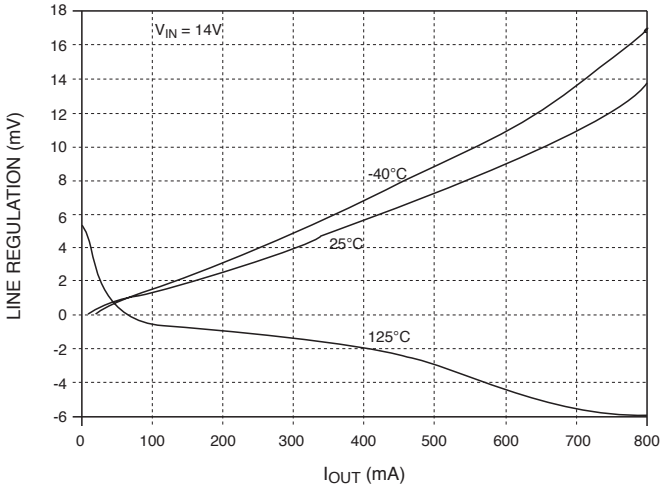
Dropout Voltage vs. Output Current over Temperature



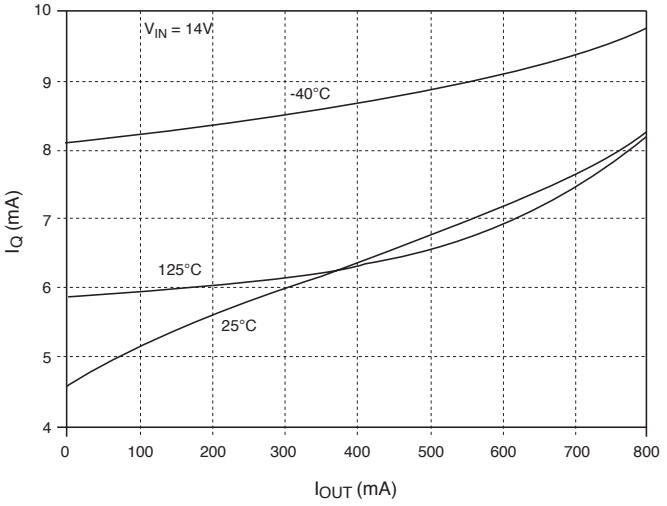
Load Regulation vs. Output Current over Temperature



Line Regulation vs. Output Current over Temperature

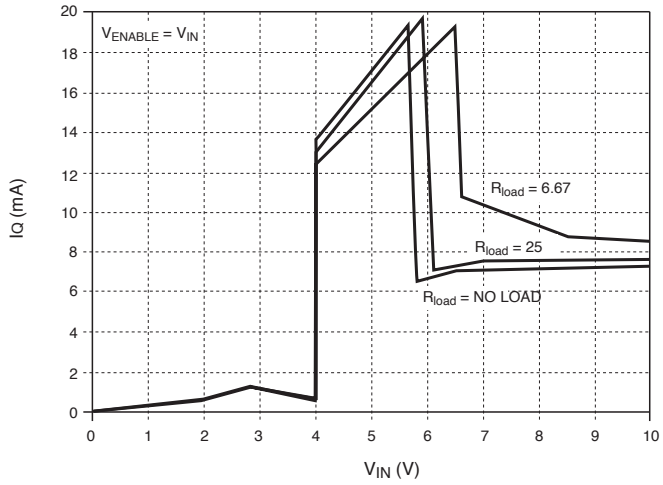


Quiescent Current vs. Output Current over Temperature

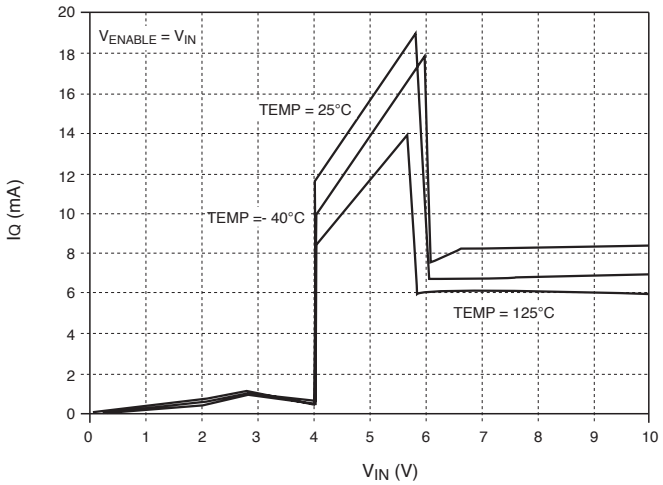


Typical Performance Characteristics: continued

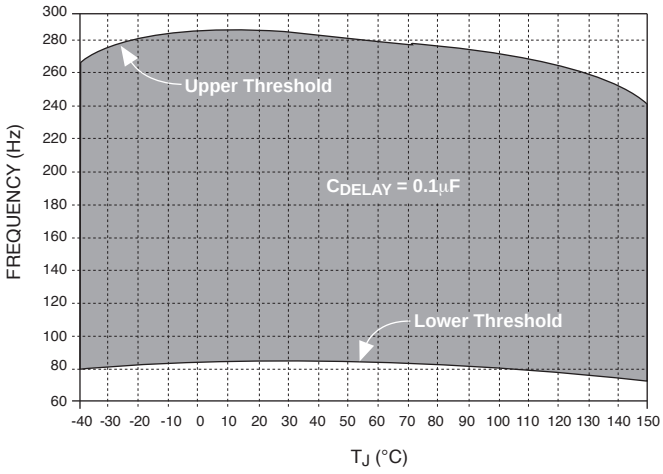
Quiescent Current vs. V_{IN} over R_{LOAD}; T = 25°C



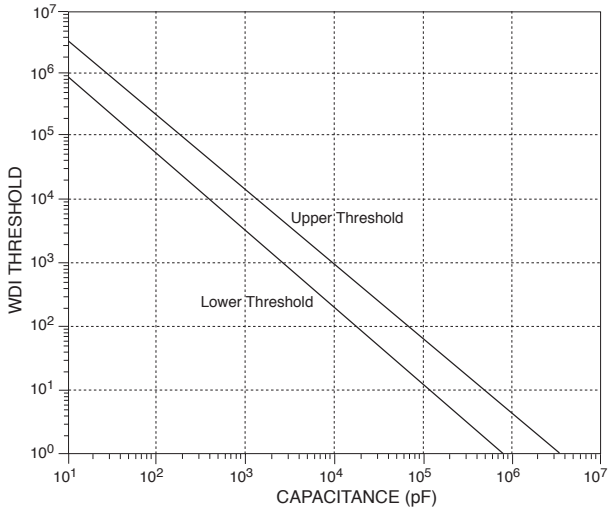
Quiescent Current vs. V_{IN} over Temperature; R_{LOAD} = 25Ω



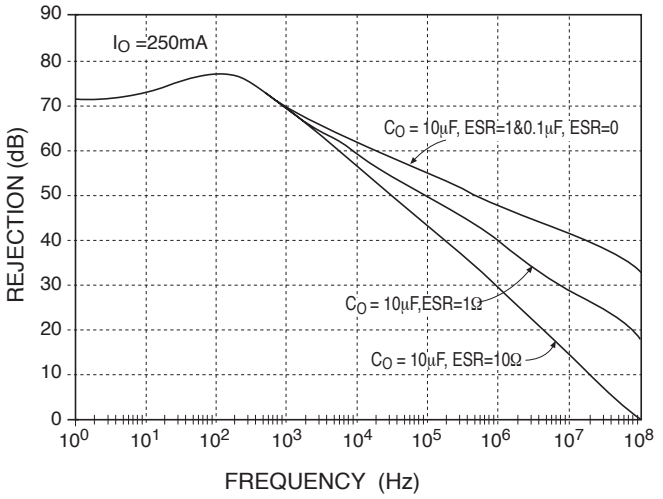
Watchdog Frequency Thresholds vs. Temperature



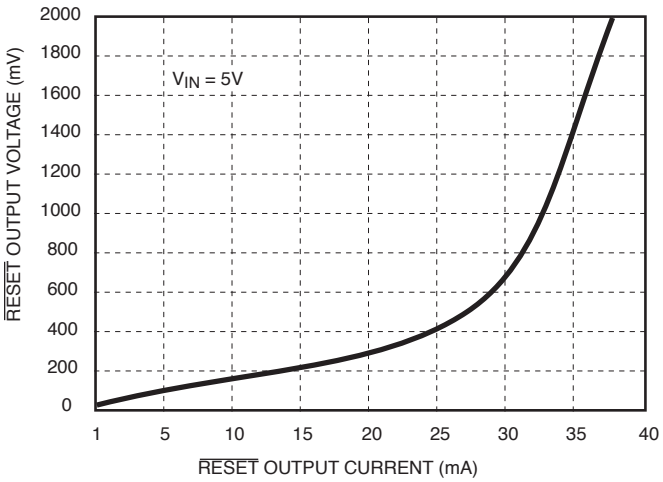
Watchdog Frequency Threshold vs C_{DELAY}



Ripple Rejection vs Frequency



$\overline{\text{RESET}}$ Output Voltage vs Output Current



Definition of Terms

Dropout Voltage
The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage
The DC voltage applied to the input terminals with respect to ground.

Line Regulation
The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation
The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current
The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection
The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Current Limit
Peak current that can be delivered to the output.

Circuit Description

Voltage Reference and Output Circuitry

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop , the output voltage is maintained within ±4% over temperature and supply variation.

Output Stage

The composite PNP-NPN output structure (Figure1) provides 500mA (min) of output current while maintaining a low drop out voltage (1.25V) and drawing little quiescent current (7mA).

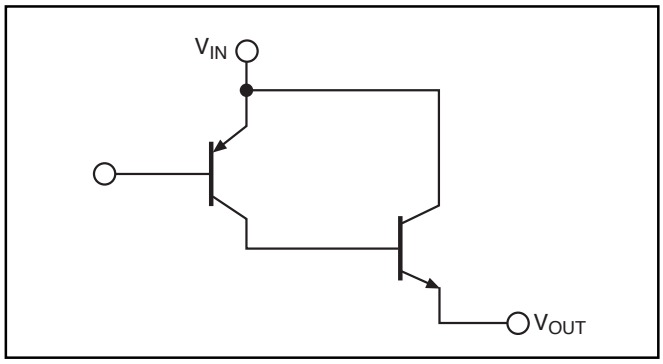


Figure 1: Composite Output Stage of the CS8140/1

The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).

If the input voltage rises above 30V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

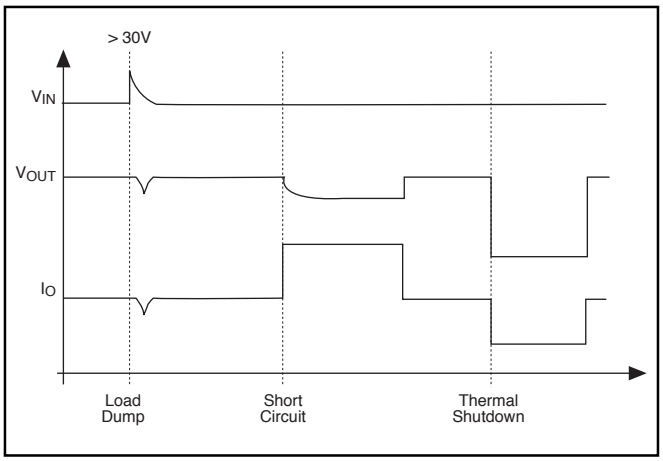


Figure 2: Typical Circuit Waveforms for Output Stage Protection.

Should the junction temperature of the power device exceed 180˚C (typ), the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

Regulator Control Functions

The CS8140 differs from all other linear regulators in its unique combination of control features.

Watchdog and ENABLE Functions

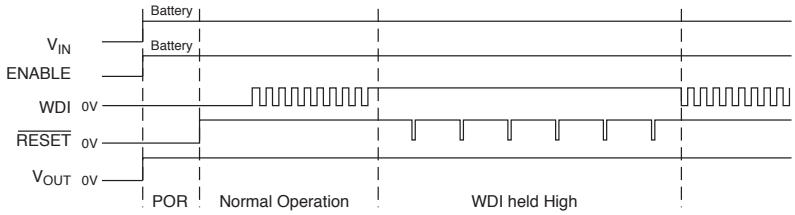
V_{OUT} is controlled by the logic functions ENABLE and Watchdog (Table 1).

V_{OUT} (V)					
	WDI				
ENABLE	Slow	Normal	Fast	High	Low
H	5	5	5	5	5
L	0	5	0	0	0

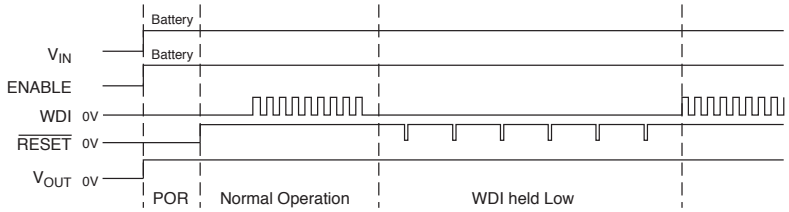
Table 1: V_{OUT} as a Function of ENABLE and Watchdog

Figure 3: Timing Diagrams for Watchdog and ENABLE Functions

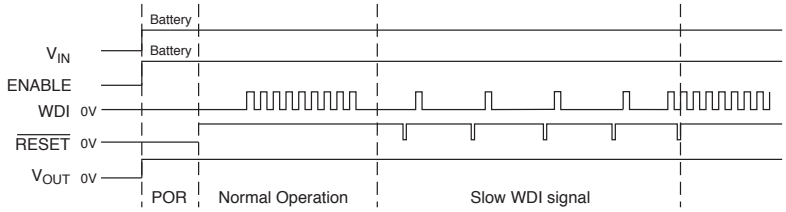
3a: V_{OUT} when Watchdog is held high and ENABLE = HIGH.



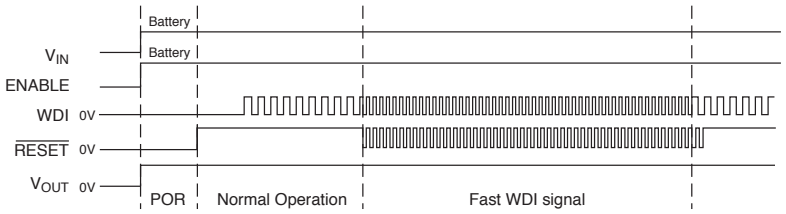
3b: V_{OUT} when Watchdog is held low and ENABLE = HIGH.



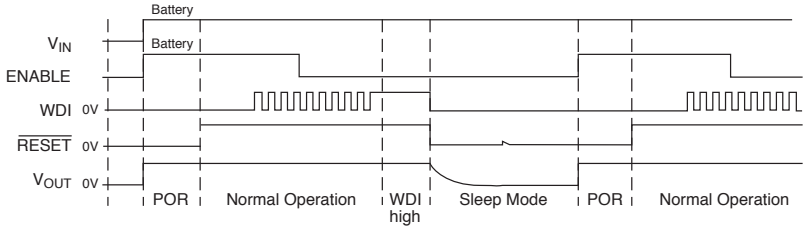
3c: V_{OUT} when Watchdog is too slow and ENABLE = HIGH.



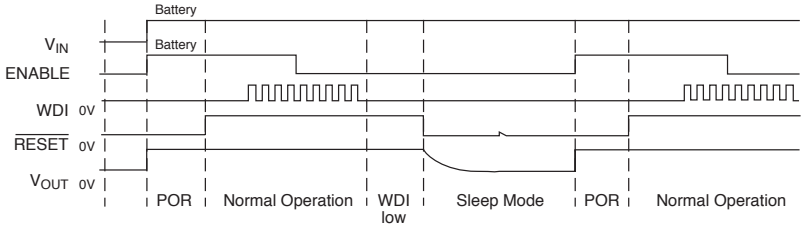
3d: V_{OUT} when Watchdog is too fast and ENABLE = HIGH.



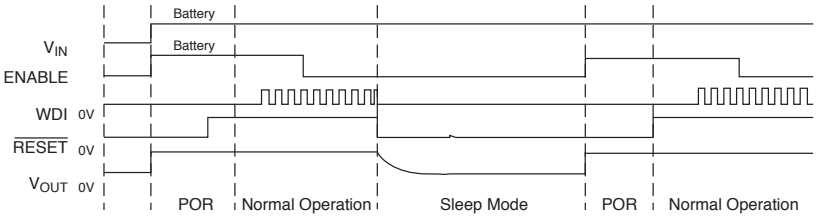
3e: WDI held high after a normal period of operation; ENABLE = LOW.



3f: WDI held low or is too slow after a normal period of operation; ENABLE = LOW.



3g: WDI frequency rises above the upper frequency threshold after a normal period of operation; ENABLE = LOW (for the CS8140 only).



Circuit Description: continued

As long as ENABLE is high or ENABLE is low and the Watchdog signal is normal, V_{OUT} will be at 5V (typ). If ENABLE is low and the Watchdog signal moves outside programmable limits, the output transistor turns off and the IC goes into SLEEP mode. Only the ENABLE circuitry in the IC remains powered up, drawing a quiescent current of 250μA.

The Watchdog monitors the frequency of an incoming WDI signal. If the signal falls outside of the WDI window, a frequency programmable pulse train is generated at the $\overline{\text{RESET}}$ lead (Figure 3) until the correct Watchdog input signal reappears at the lead (ENABLE = HIGH).

The lower and upper window threshold limits of the watchdog function are set by the value of C_{DELAY}. The limits are determined according to the following equations for the CS8140:

(a) $t_{WDILOWER} = (1.3 \times 10^{5})C_{DELAY}$ or

$f_{WDI(LOWER)} = (7.69 \times 10^{-6})C_{DELAY}^{-1}$

(b) $t_{WDI(UPPER)} = (3.82 \times 10^{-4})C_{DELAY}$ or

$f_{WDI(UPPER)} = (2.62 \times 10^{-5})C_{DELAY}^{-1}$

For the CS8141 the lower limit is determined by the equations in (a) above.

The capacitor C_{DELAY} also determines the frequency of the $\overline{\text{RESET}}$ signal and the POWER-ON- $\overline{\text{RESET}}$ (POR) delay period.

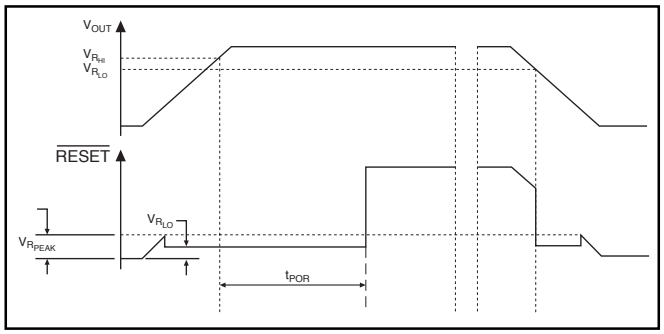
$\overline{\text{RESET}}$ Function

The $\overline{\text{RESET}}$ function is activated when the Watchdog signal is outside of its preset window (Figure 3), when the regulator is in its power up state (Figure 4a) or when V_{OUT} drops below V_{OUT} -4.5% for more than 2μs (Figure 4b.)

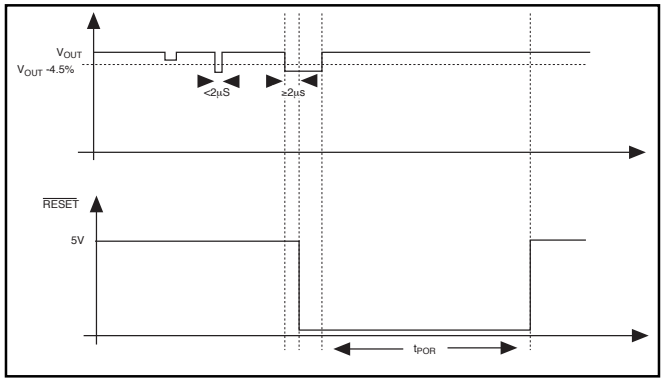
If the Watchdog signal falls outside of the preset voltage and frequency window, a frequency programmable pulse train is generated at the $\overline{\text{RESET}}$ lead (Figure 3) until the correct Watchdog input signal reappears at the lead. The duration of the $\overline{\text{RESET}}$ pulse is determined by C_{DELAY} according to the following equation:

$$t_{WDI(\overline{RESET})} = (1 \times 10^{4})C_{DELAY}$$

$\overline{\text{RESET}}$ Circuit Waveforms with Delays Indicated



4a: Power $\overline{\text{RESET}}$ and Power Down



4b: Undervoltage Triggered $\overline{\text{RESET}}$

If an undervoltage condition exists, the voltage on the $\overline{\text{RESET}}$ lead goes low and the delay capacitor, C_{DELAY}, is discharged. $\overline{\text{RESET}}$ remains low until output is in regulation, the voltage on C_{DELAY} exceeds the upper switching threshold and the Watchdog input signal is within its set window limits (Figure 4). The delay after the output is in regulation is:

$$t_{POR(typ)} = (4.75 \times 10^{5})\ C_{DELAY}$$

The $\overline{\text{RESET}}$ delay circuit is also programmed with the external cap C_{DELAY}.

The output of the reset circuit is an open collector NPN. $\overline{\text{RESET}}$ is operational down to V_{OUT} = 1V. Both $\overline{\text{RESET}}$ and its delay are governed by comparators with hysteresis to avoid undesirable oscillations.

Application Notes

CS8140 Design Example

The CS8140 with its unique integration of linear regulator and control features: $\overline{\text{RESET}}$, ENABLE and WATCHDOG, provides a single IC solution for a microprocessor power supply. The reset delay, reset duration and watchdog frequency limits are all determined by a single capacitor. For a particular microprocessor the overriding requirement is usually the reset delay (also known as power on reset). The capacitor is chosen to meet this requirement and the reset duration and watchdog frequency follow.

The reset delay is given by:

$$t_{POR(typ)} = (4.75 \times 10^{5})C_{DELAY}$$

Assume that the reset delay must be 200ms minimum.

From the CS8140 data sheet the reset delay has a ±37% tolerance due to the regulator.

Assume the capacitor tolerance is ±10%.

$$t_{POR}\ (min) = (4.75 \times 10^{5} \times 0.63) \times C_{DELAY} \times 0.9$$

$$C_{DELAY}\ (min) = \frac{t_{POR}\ (min)}{2.69 \times 10^{5}}$$

$$C_{DELAY} = (min) = 0.743\ \mu F$$

Closest standard value is 0.82μF.

Minimum and maximum delays using 0.82μF are 220ms and 586ms.

The duration of the reset pulse is given by:

$$T_{WDI(\overline{RESET})}(typ) = (1 \times 10^4) \times C_{DELAY}$$

This has a tolerance of ±50% due to the IC, and ±10% due to the capacitor.

The duration of the reset pulse ranges from 3.69ms to 13.5ms.

The watchdog signal can be expressed as a frequency or time. From a programmers point of view, time is more useful since they must ensure that a watchdog signal is issued consistently several times per second.

The maximum and minimum watchdog times are given by:

$$t_{WDI(LOWER)} = (1.3 \times 10^5)C_{DELAY}$$
$$t_{WDI(UPPER)} = (3.82 \times 10^4)C_{DELAY}$$

There is a tolerance of ±20% due to the CS8140.

With a capacitor tolerance of ±10%:

$$t_{WDI(LOWER)} = (1.3 \times 10^5) \times 1.20 \times 1.1 \times C_{DELAY}$$
$$t_{WDI(UPPER)} = (3.82 \times 10^4) \times 0.8 \times 0.9 \times C_{DELAY}$$

$$t_{WDI(LOWER)} = 141ms(max)$$
$$t_{WDI(UPPER)} = 22.5ms\ (max)$$

$$t_{WDI(LOWER)} = (1.3 \times 10^5) \times 0.8 \times 0.9 \times C_{DELAY}$$
$$t_{WDI(UPPER)} = (3.82 \times 10^4) \times 1.2 \times 1.1 \times C_{DELAY}$$

$$t_{WDI(LOWER)} = 76ms(min)$$
$$t_{WDI(UPPER)} = 41ms\ (min)$$

The software must be written so that a watchdog signal arrives at least every 76ms but not faster than every 41ms (Figure 5).

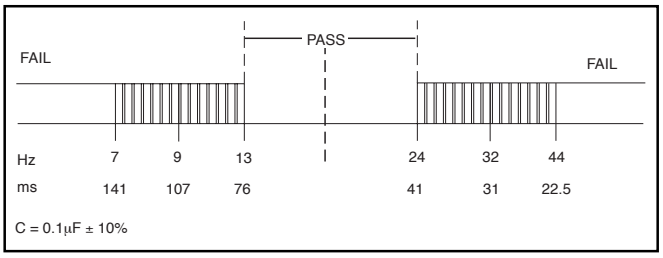


Figure 5: WDI signal for CDelay = 0.82µF using CS8140.

The CS8141 is identical to the CS8140 except that the CS8141 only has a lower watchdog frequency threshold. The designer using this part need only be concerned with $t_{WDI(LOWER)}$ as shown in Figure 6.

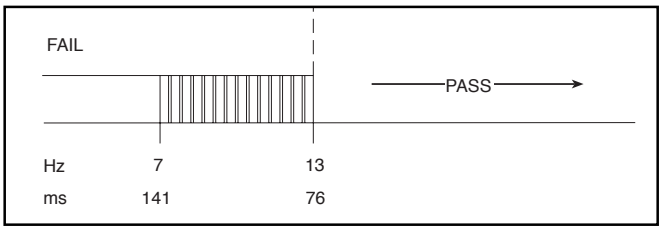


Figure 6: WDI signal for CDelay = 0.82µF using CS8141.

Energy Conservation and Smart Features

Energy conservation is another benefit of using a regulator with integrated microprocessor control features. Using the CS8140 or CS8141 as indicated in Figure 8, the microprocessor can control its own power down sequence. The momentary contact switch quickly charges C1 through R1.

When the voltage across C1 reaches 3.95V (the enable threshold), the output switches on and V_{OUT} rises to 5V. After a delay period determined by C_{Delay}, a frequency programmable reset pulse train is generated at the reset output. The pulse train continues until the correct watchdog signal appears at the WDI lead. C1 is now left to discharge through the input impedance of the enable lead (approximately 150kΩ) and the enable signal disappears. The output voltage remains at 5V as long as the CS8140 continues to receive the correct watchdog signal.

The microprocessor can power itself down by terminating its watchdog signal. When the microprocessor finishes its housekeeping or power down software routine, it stops sending a watchdog signal. In response, the regulator generates a reset signal and goes into a sleep mode where V_{OUT} drops to 0V, shutting down the microprocessor.

Stability Considerations

The output or compensation capacitor C_2 in Figure 7 helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

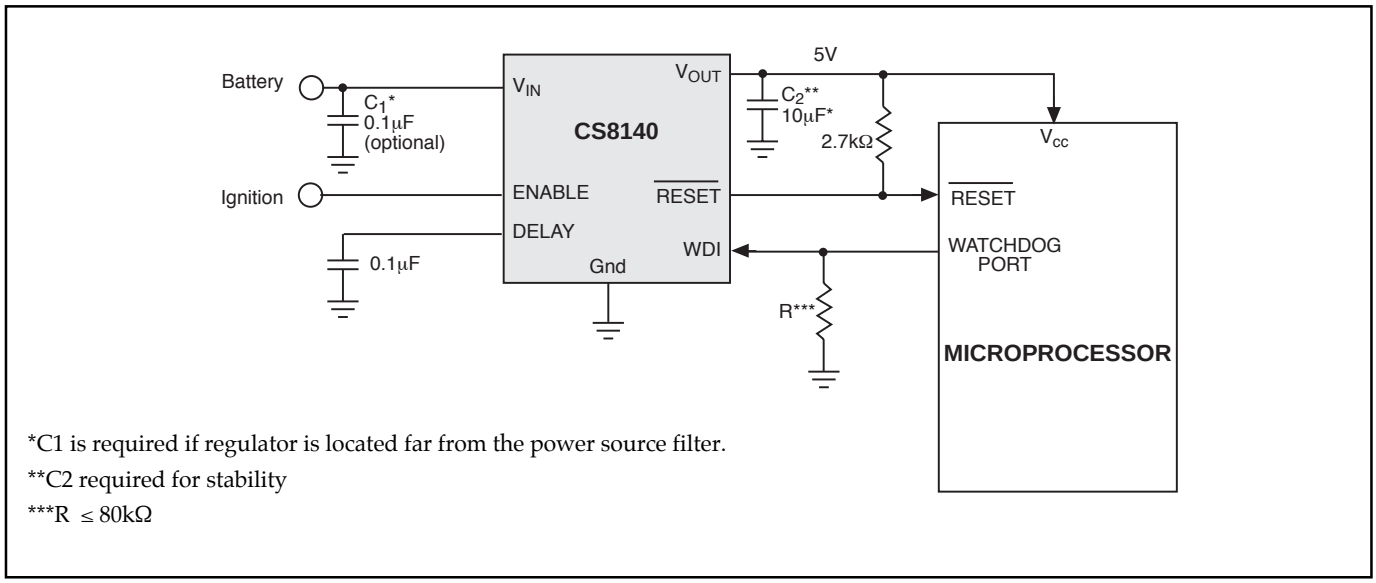
The value for the output capacitor C_2 in Figure 7 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Application Diagrams



*C1 is required if regulator is located far from the power source filter.
**C2 required for stability
***R ≤ 80kΩ

Figure 7. Application Diagram

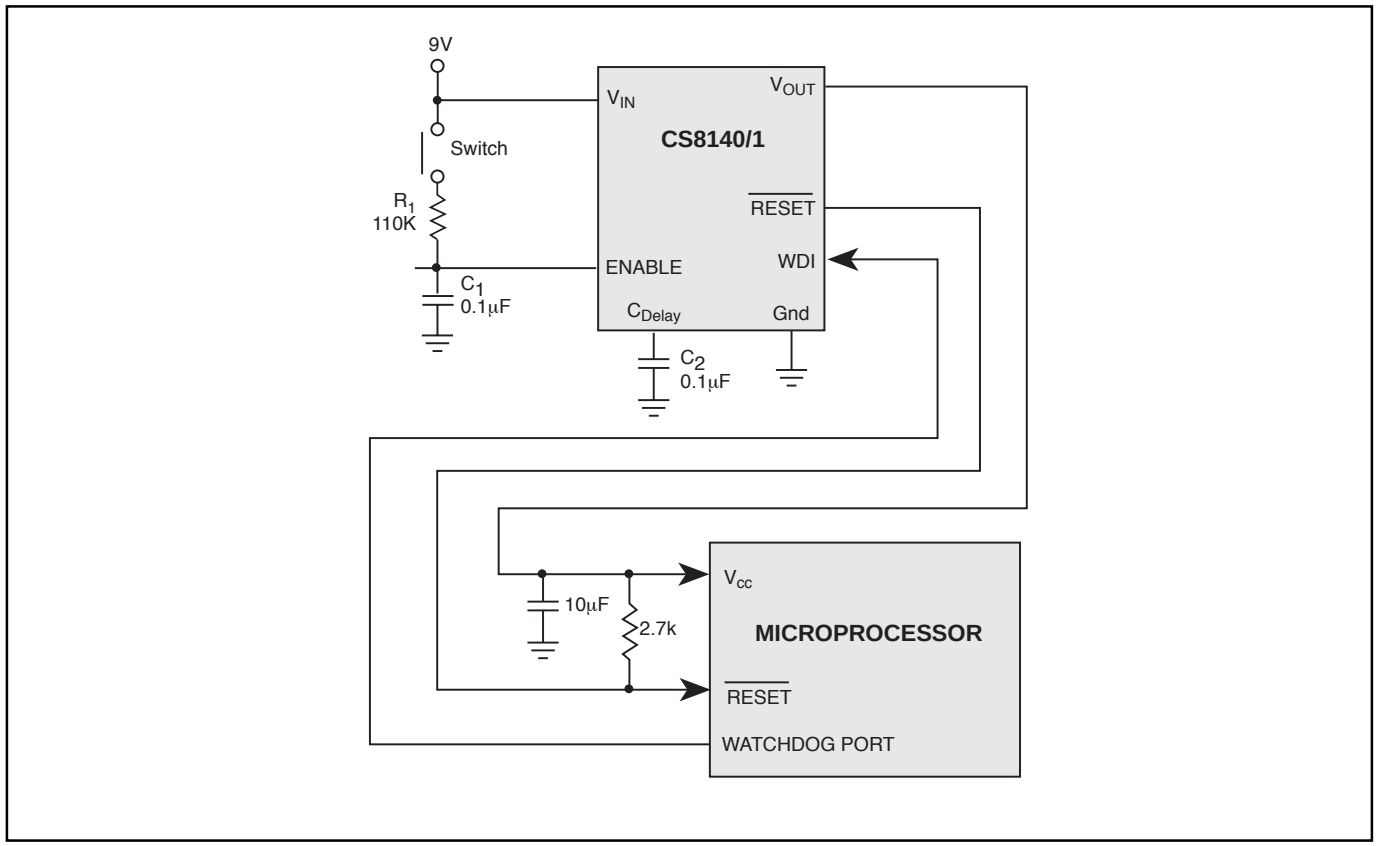


Figure 8. Applications diagram for CS8140. The CS8140 provides a 5V tightly regulated supply and control function to the microprocessor. In this application, the microprocessor controls its own power down sequence (*see text*).

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of +/- 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 9) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\}I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

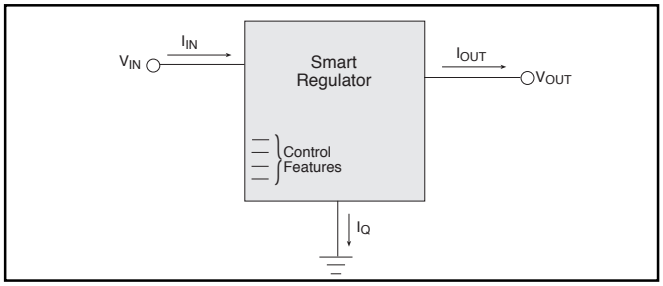


Figure 9: Single output regulator with key performance parameters labeled.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

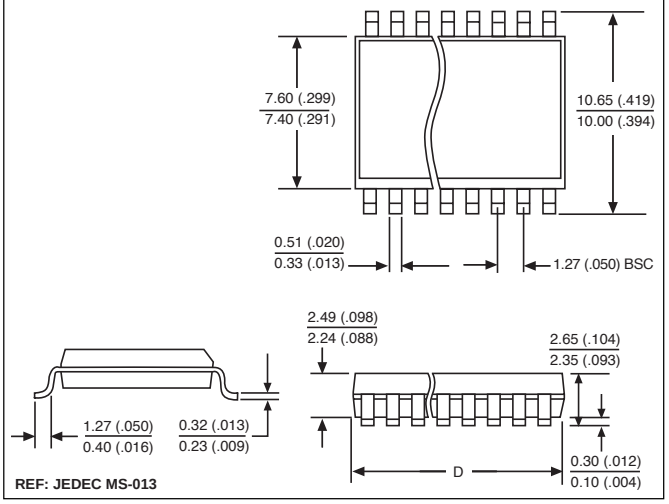
$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Package Specification

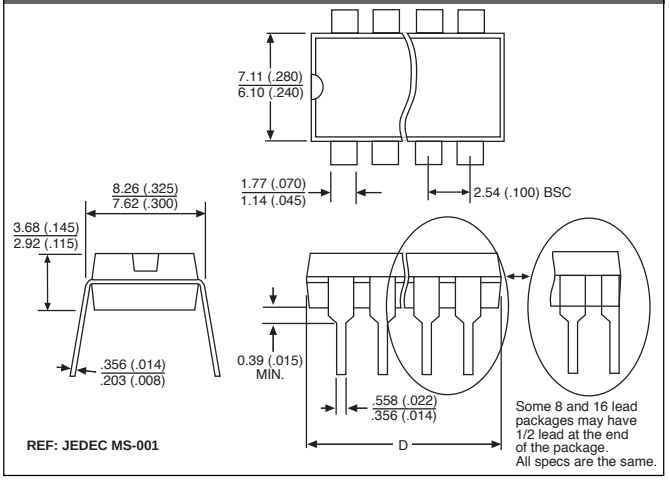
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D Metric Max	D Metric Min	D English Max	D English Min
24 Lead SOIC Wide	15.60	15.20	.614	.598
14 Lead PDIP	19.69	18.67	.775	.735

Surface Mount Wide Body (DW); 300 mil wide



Plastic DIP (N); 300 mil wide



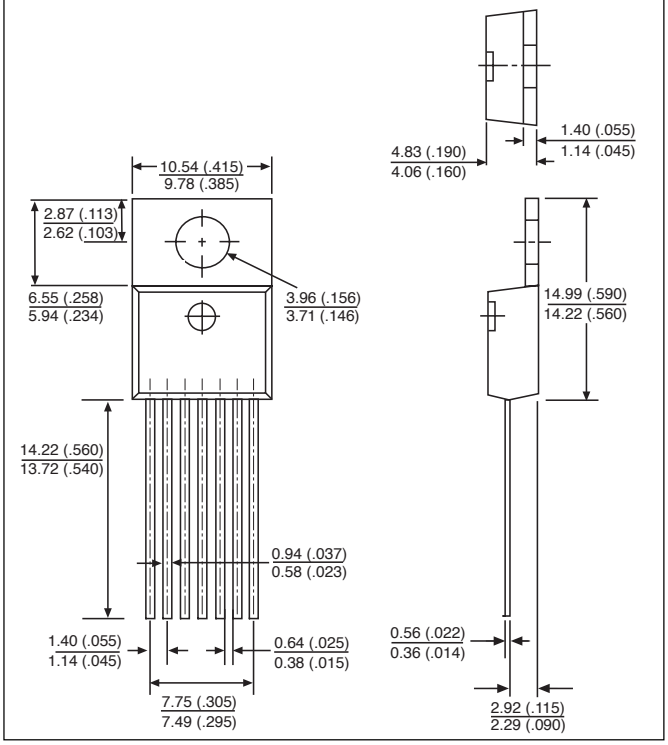
Ordering Information

Part Number	Description
CS8140YT7	7L TO-220 Straight
CS8140YTVA7	7L TO-220 Vertical
CS8140YTHA7	7L TO-220 Horizontal
CS8140YDW24	24L SO
CS8140YDWR24	24L SO *(tape & reel)*
CS8140YN14	14L PDIP
CS8141YT7	7L TO-220 Straight
CS8141YTVA7	7L TO-220 Vertical
CS8141YTHA7	7L TO-220 Horizontal
CS8141YDWF24	24L SO *(internally fused leads)*
CS8141YDWFR24	24L SO *(internally fused leads)* *(tape & reel)*
CS8141YN14	14L PDIP

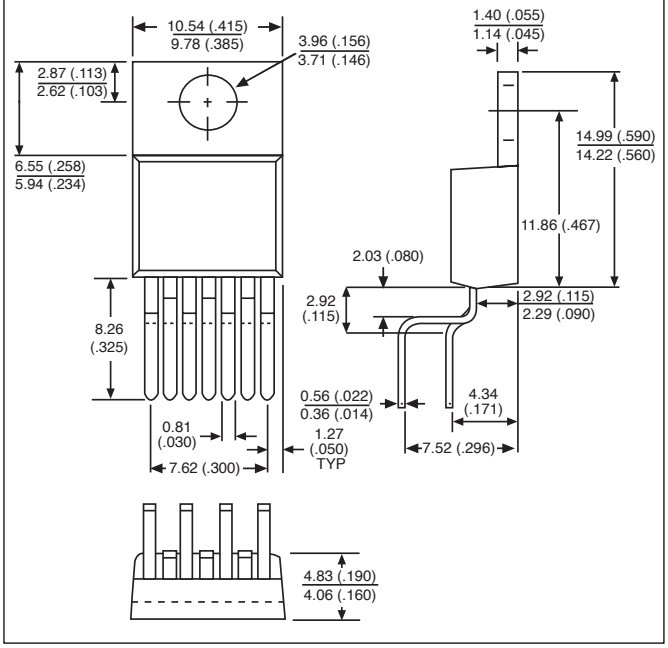
PACKAGE THERMAL DATA

Thermal Data		7 L TO-220	24L CS8140	24L (Fused) CS8141	14 L PDIP	
$R_{\Theta JC}$	typ	1.6	16	9	48	°C/W
$R_{\Theta JA}$	typ	50	80	55	85	°C/W

7 Lead TO-220 (T) Straight



7 Lead TO-220 (TVA) Vertical



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