AUTOMOTIVE GRADE

CS8122

2% 5V, 750mA Low Dropout Linear Regulator with Delayed $\overline{\text{RESET}}$

Description

The CS8122 is a precision 5V linear regulator capable of sourcing in excess of 750mA. The $\overline{\text{RESET}}$'s delay time is externally programmed using a discrete RC network. During power up, or when the output goes out of regulation, the $\overline{\text{RESET}}$ lead remains in the low state for the duration of the delay. This function is independent of the input voltage and will function correctly as long as the output voltage remains at or above 1V. Hysteresis is included in the Delay and the $\overline{\text{RESET}}$ comparators to improve noise immunity. A latching discharge circuit is used to discharge the delay capacitor when it is triggered by a brief fault condition.

The regulator is protected against a variety of fault conditions: i.e. reverse battery, overvoltage, short circuit and thermal runaway conditions. The regulator is protected against voltage transients ranging from -50V to +40V. Short circuit current is limited to 1.2A (typ).

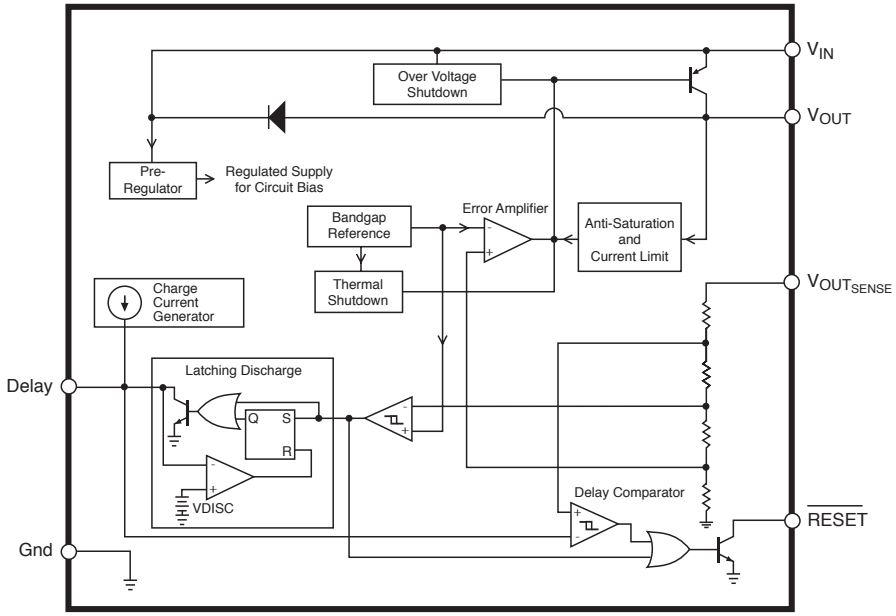
The CS8122 is an improved replacement for the CS8126 and features a tighter tolerance on its output voltage (2% vs 4%).

The CS8122 is packaged in a 5 lead TO–220 with copper tab. The copper tab can be connected to a heat sink if necessary.

Features

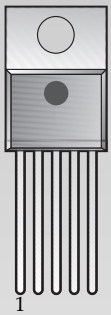
- 5V +/- 2% Regulated Output
- Low Dropout Voltage (0.6V @ 0.5A)
- 750mA Output Current Capability
- Externally Programmed $\overline{\text{RESET}}$ Delay
- Fault Protection
  - Reverse Battery
  - 60V Load Dump
  - -50V Reverse Transient
  - Short Circuit
  - Thermal Shutdown

Block Diagram



Package Options

5 Lead TO-220



1 V_{IN}
2 V_{OUT}
3 Gnd
4 Delay
5 $\overline{\text{RESET}}$

Cherry Semiconductor

Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

Absolute Maximum Ratings

Input Operating Range ..... -0.5 to 26V
Power Dissipation ..... Internally Limited
Transient Input Voltage ..... -50V, 60V
Output Current ..... Internally Limited
ESD Susceptibility (Human Body Model) 4kV
Junction Temperature ..... -55°C to 150°C
Storage Temperature ..... -55°C to 150°C
Lead Temperature Soldering
Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak

Electrical Characteristics: $-40^{\circ}C \le T_A \le +125^{\circ}C$, $-40^{\circ}C \le T_J \le +150^{\circ}C$, $6V \le V_{IN} \le 26V$, $5mA \le I_{OUT} \le 500mA$, $R_{\overline{RESET}} = 4.7k\Omega$ to V_{CC} unless otherwise noted*

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage (V_{OUT})					
Output Voltage		4.9	5.0	5.1	V
Dropout Voltage	I_{OUT} = 500mA		0.35	0.60	V
Supply Current	$I_{OUT} \le 10mA$ $I_{OUT} \le 100mA$ $I_{OUT} \le 500mA$		2 6 55	7 12 100	mA
Line Regulation	$6V \le V_{IN} \le 26V$, I_{OUT} = 50mA		5	50	mV
Load Regulation	$50mA \le I_{OUT} \le 500mA$, V_{IN} = 14V		10	50	mV
Ripple Rejection	f = 120Hz, V_{IN} = 7 to 17V, I_{OUT} = 250mA	54	75		dB
Current Limit		0.75	1.20		A
Overvoltage Shutdown		32		40	V
Maximum Line Transient	$V_{OUT} \le 5.5V$	60	95		V
Reverse Polarity Input Voltage DC	$V_{OUT} \ge -0.6V$, 10Ω Load	-15	-30		V
Reverse Polarity Input Voltage Transient	1% Duty Cycle, T < 100ms, 10Ω Load	-50	-80		V
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
■ $\overline{RESET}$ and Delay Functions					
Delay Charge Current	V_{DELAY} = 2V	5	10	15	µA
$\overline{RESET}$ Threshold	V_{OUT} Increasing, $V_{RT(ON)}$ V_{OUT} Decreasing, $V_{RT(OFF)}$	4.65 4.50	4.90 4.70	V_{OUT}-0.01 V_{OUT}-0.16	V V
$\overline{RESET}$ Hysteresis	$V_{RH} = V_{RT(ON)} - V_{RT(OFF)}$	150	200	250	mV
Delay Threshold	Charge, $V_{DC(HI)}$ Discharge, $V_{DC(L)}$	3.25 2.85	3.50 3.10	3.75 3.35	V V
Delay Hysteresis		200	400	800	mV
$\overline{RESET}$ Output Voltage Low	$1V < V_{OUT} < V_{RT(L)}$, 3kΩ to V_{OUT}		0.1	0.4	V
$\overline{RESET}$ Output Leakage	$V_{OUT} > V_{RT(H)}$ Current	0		10	µA
Delay Capacitor Discharge Voltage	Discharge Latched "ON", $V_{OUT} > V_{RT}$		0.2	0.5	V
Delay Time	C_{DELAY} = 0.1µF	16	32	48	ms

* To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

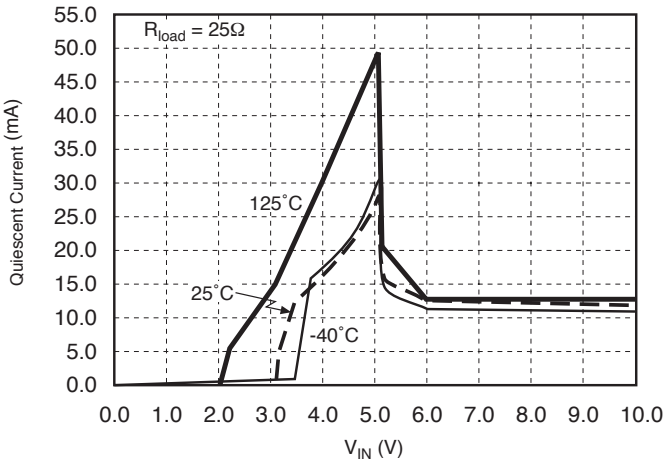
$$\text{Delay Time} = \frac{C_{Delay} \times V_{Delay\ Threshold\ Charge}}{I_{Charge}} = C_{Delay} \times 3.5 \times 10^5\ (\text{typ})$$

Package Lead Description

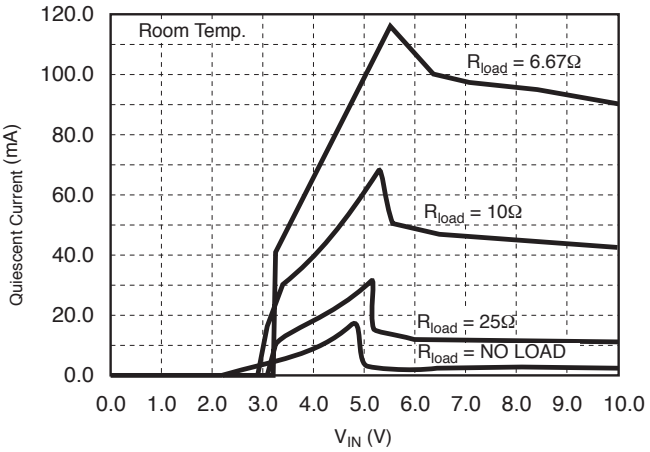
PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
5Lead TO-220		
1	V_{IN}	Unregulated supply voltage to IC.
2	V_{OUT}	Regulated 5V output.
3	Gnd	Ground connection.
4	Delay	Timing capacitor for $\overline{\text{RESET}}$ function.
5	$\overline{\text{RESET}}$	CMOS/TTL compatible output lead. $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops below 6% of it's regulated value.

Typical Performance Characteristics

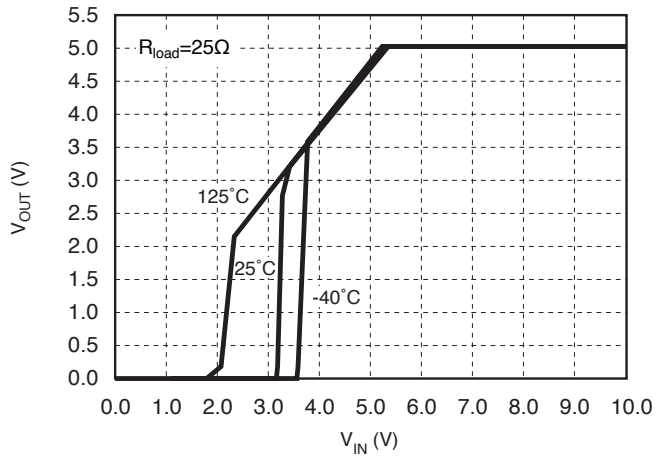
Quiescent Current vs Input Voltage over Temperature



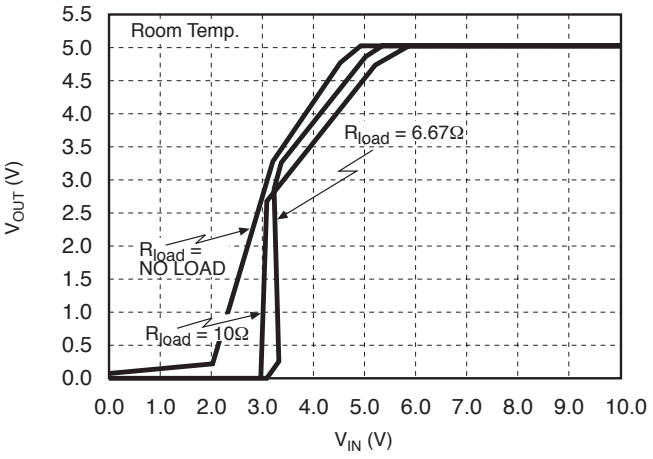
Quiescent Current vs Input Voltage over Load Resistance



Output Voltage vs Input Voltage over Temperature

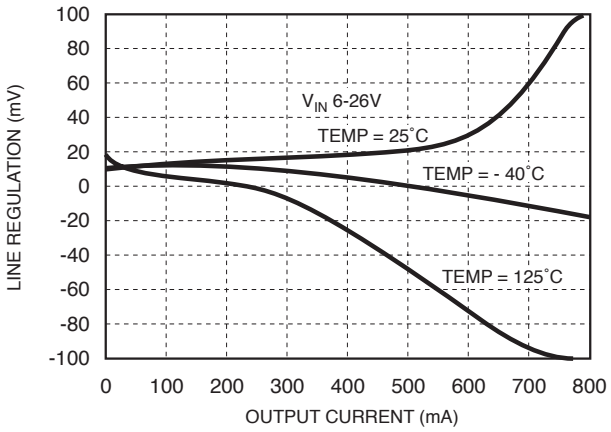


V_{OUT} vs. V_{IN} over R_{LOAD}

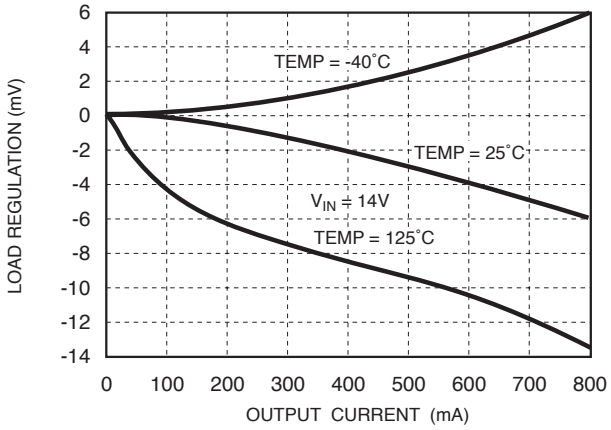


Typical Performance Characteristics: continued

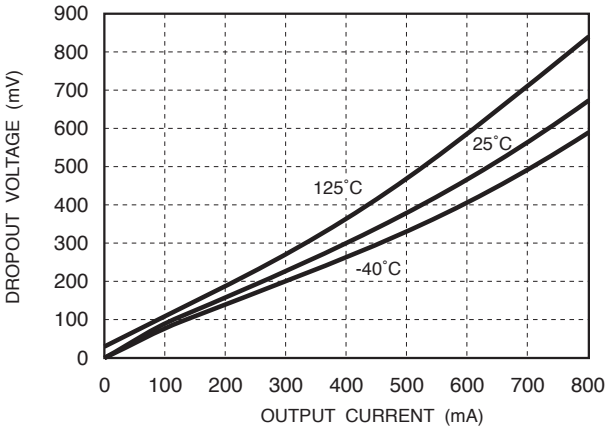
Line Regulation vs. Output Current



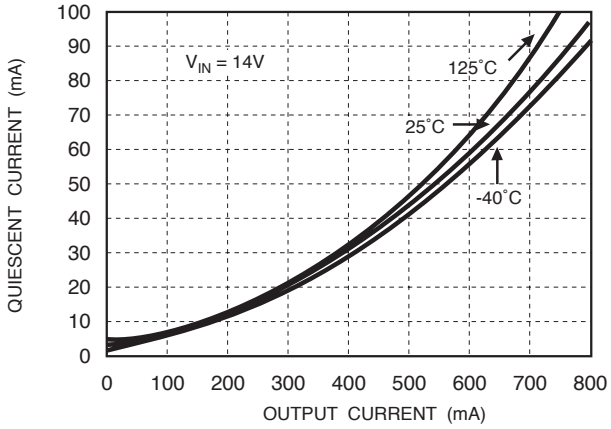
Load Regulation vs. Output Current



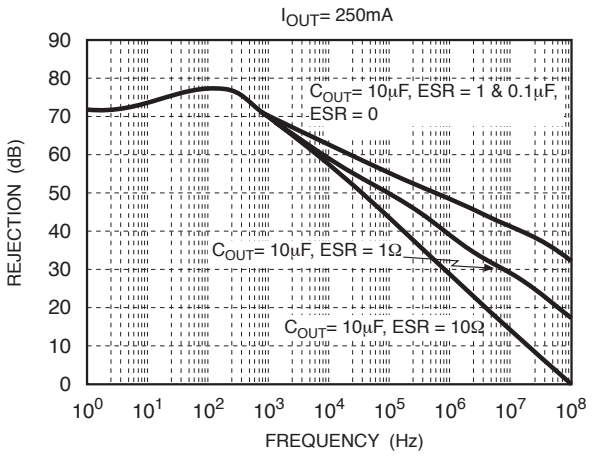
Dropout Voltage vs. Output Current



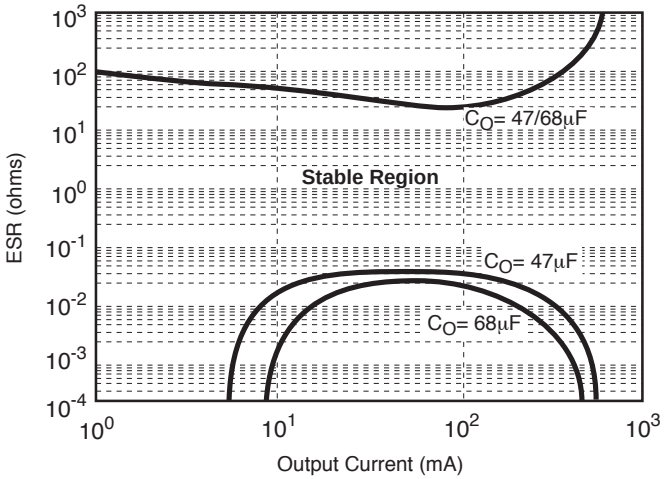
Quiescent Current vs. Output Current



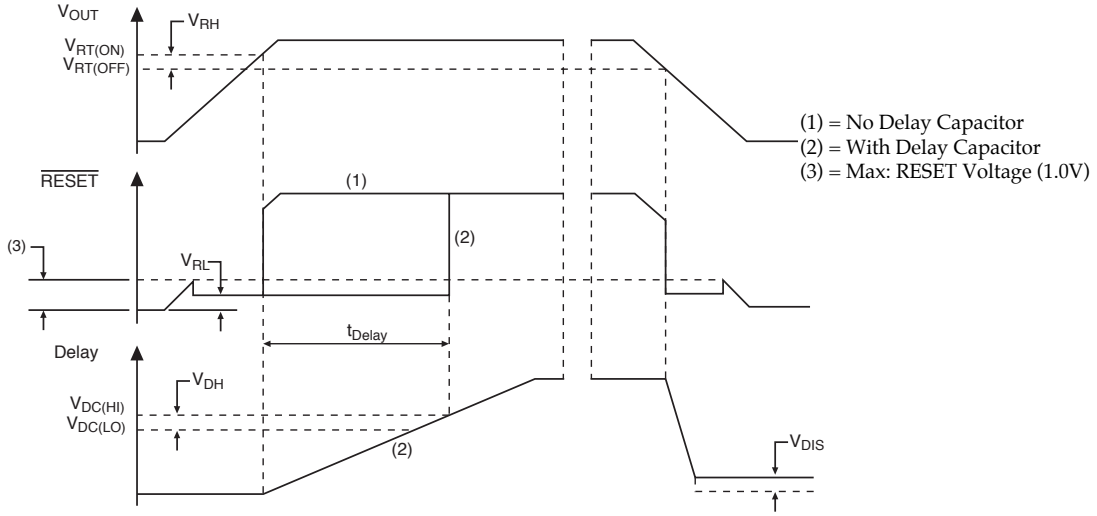
Ripple Rejection



Output Capacitor ESR



$\overline{\text{RESET}}$ Circuit Waveform



Circuit Description

The CS8122 $\overline{\text{RESET}}$ function, has hysteresis on both the reset and delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1V.

The $\overline{\text{RESET}}$ circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text{RESET}}$ output NPN transistor is controlled by the two circuits described (see Block Diagram).

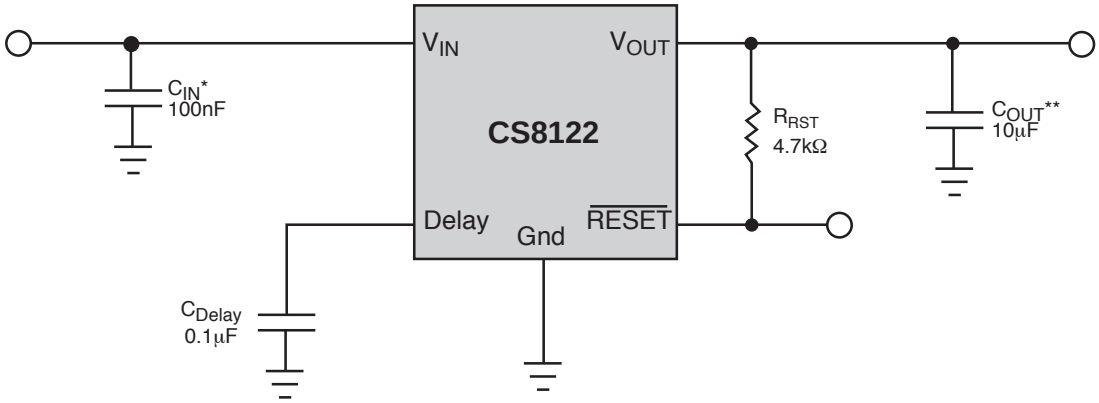
Low Voltage Inhibit Circuit

The Low Voltage Inhibit Circuit monitors output voltage, and when output voltage is below the specified minimum, causes the $\overline{\text{RESET}}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the $\overline{\text{RESET}}$ output transistor to go into the OFF state if allowed by the $\overline{\text{RESET}}$ Delay circuit.

Reset Delay Circuit

The Reset Delay Circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead. The Delay lead provides source current to the external delay capacitor only when the Low Voltage Inhibit circuit indicates that output voltage is above $V_{RT(ON)}$. Otherwise, the Delay lead sinks current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage is below $V_{RT(OFF)}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures that a controlled $\overline{\text{RESET}}$ pulse is generated following detection of an error condition. The circuit allows the $\overline{\text{RESET}}$ output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $V_{DC(HI)}$.

Test Circuit



*C_{IN} required if regulator is far from power source filter.

**C_{OUT} required for stability.

Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 1) is:

$$P_{D(max)}=|V_{IN(max)}-V_{OUT(min)}|I_{OUT(max)}+V_{IN(max)}I_Q \quad (1)$$

where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

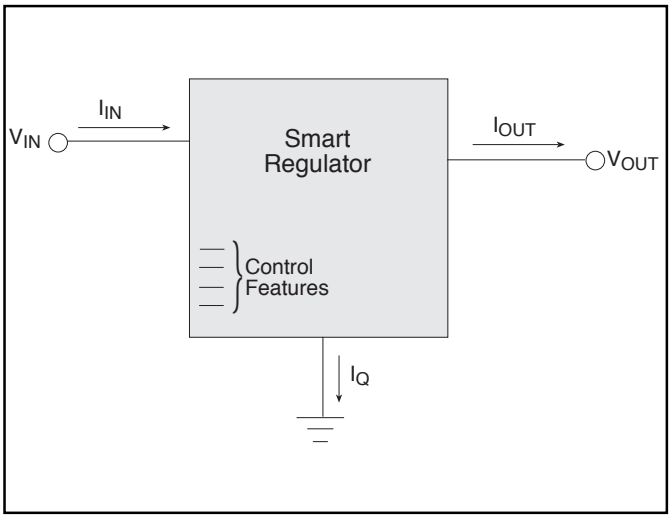


Figure 1: Single output regulator with key performance parameters labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

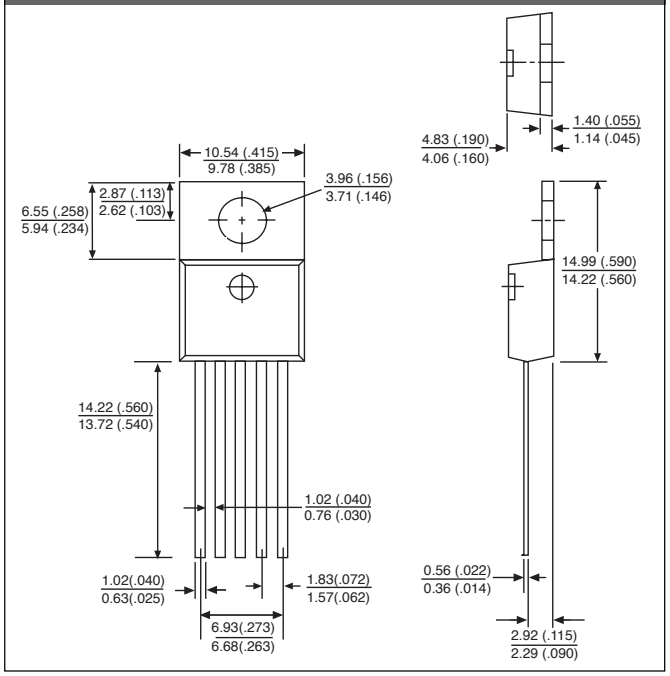
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

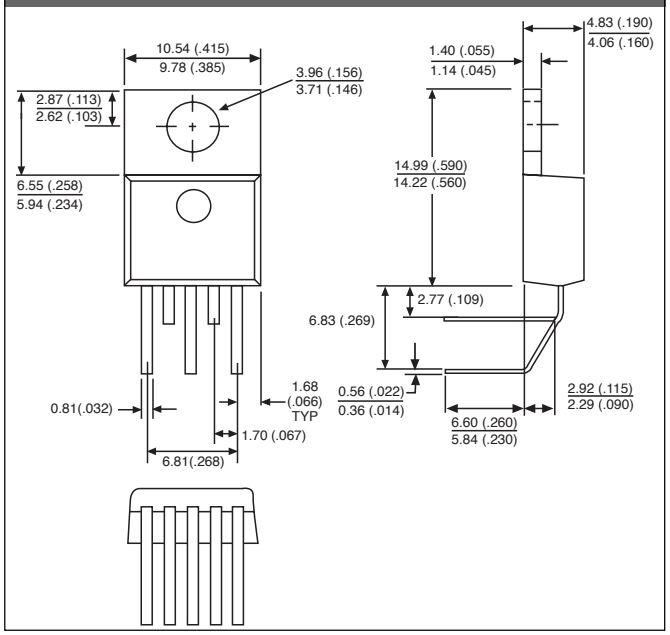
Package Specification

PACKAGE DIMENSIONS IN mm(INCHES)

5 Lead TO-220 (T) Straight



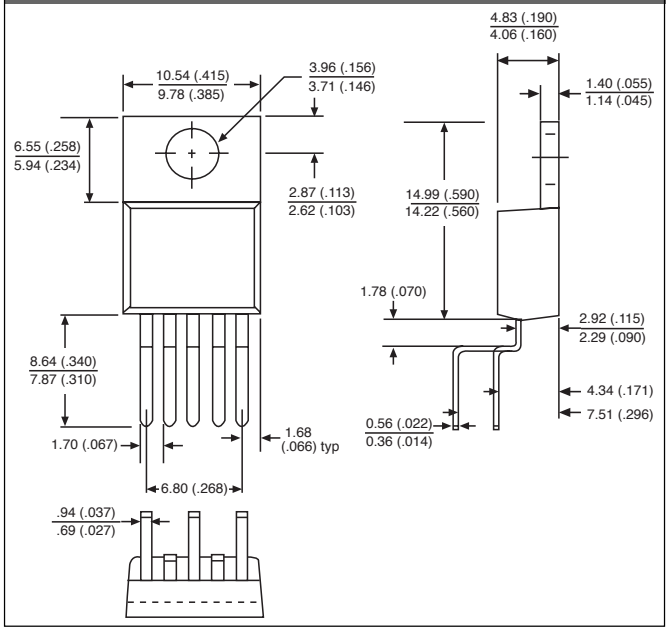
5 Lead TO-220 (THA) Horizontal



PACKAGE THERMAL DATA

Thermal Data		5 Lead TO-220	
$R_{\Theta JC}$	typ	2.1	°C/W
$R_{\Theta JA}$	typ	50	°C/W

5 Lead TO-220 (TVA) Vertical



Ordering Information

Part Number	Description
CS8122YT5	5 Lead TO-220 Straight
CS8122YTHA5	5 Lead TO-220 Horizontal
CS8122YTVA5	5 Lead TO-220 Vertical

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.