CS4373

Low-power, High-performance ΔΣ Test DAC

Features

- Digital ΔΣ Input, Differential Analog Output
- Selectable Differential Outputs (OUT±, BUF±)
- Selectable Output Attenuation
  - 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64
- User-programmable Test Modes
  - Differential
  - Common mode
- Output Voltage: 5 V_{P-P} Differential
- Outstanding Noise Performance
  - 114 dB SNR @ 430 Hz bandwidth
- Low Total Harmonic Distortion
  - OUT±: -118 dB THD typical, -112 dB THD max
  - BUF±: -100 dB THD typical, -95 dB THD max
- Low Power Consumption
  - Normal mode: 7.8 mA
  - Low power mode: 5.0 mA
  - Power down: 400 µA
  - Sleep mode: 2 µA
- Power Supply Options
  - VA+ = +5 V; VA- = 0 V; VD = +3.3 V to +5 V
  - VA+ = +2.5 V; VA- = -2.5 V; VD = +3.3 V

Description

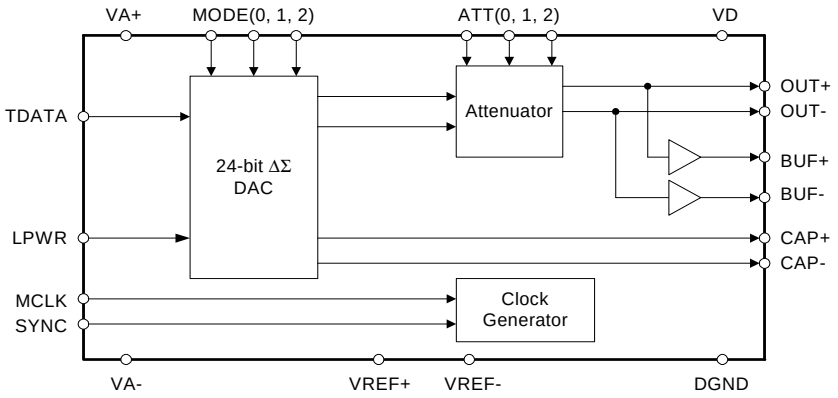
The CS4373 is a differential output digital-to-analog converter intended for high-resolution, low-frequency measurement systems. It is designed to work with the CS5376A and CS5378 digital filters, the CS3301 and CS3302 high-precision amplifiers, and the CS5371 or CS5372 high-performance ΔΣ modulators.

The CS4373 includes a set of multiplexed outputs which provide a precision output (OUT±) for testing the electronics channel and a buffered output (BUF±) for in-circuit sensor tests. It is driven by a ΔΣ bitstream and the maximum analog output is differential 5 volts peak-to-peak. Distortion performance of the DAC is typically -118 dB THD from the precision output, and -100 dB THD from the buffered output. Noise performance is 114 dB SNR over a 430 Hz bandwidth.

The CS4373 has very low power consumption. In normal mode (LPWR=0; MCLK=2.048 MHz), power consumption is 40 mW; while in Low Power mode (LPWR=1; MCLK=1.024 MHz), power consumption is 25 mW.

ORDERING INFORMATION

See page 19.



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Contacting Cirrus Logic Support

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To find the one nearest to you, go to **www.cirrus.com**

1. CHARACTERISTICS & SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- DGND = 0 V. All voltages with respect to 0 V.
- Devices are connected as shown in Figure 4 on page 8 unless otherwise noted.
- Tests performed using the TBS bitstream at TBSGAIN = 0x4B8F2, unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply		VD	3.135	3.3	5.25	V
Positive Analog Power Supply	Single Supply Dual Supplies	VA+	4.75 2.375	5 2.5	5.25 2.625	V V
Negative Analog Power Supply	Single Supply Dual Supplies	VA-	-0.25 -2.625	0 -2.5	0.25 -2.375	V V
Voltage Reference	Single Supply Dual Supply	VREF	- -	2.5 2.5	- -	V V
Specified Temperature Range		T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Performance						
Dynamic Range (OUT±)	Unloaded	SNR_{OUT}	110	114	-	dB
Dynamic Range (BUF±)	Unloaded 1 kΩ load	SNR_{BUF}	100 100	106 106	- -	dB dB
Total Harmonic Distortion (OUT±)	Unloaded	THD_{OUT}	-	-118	-112	dB
Total Harmonic Distortion (BUF±)	Unloaded 1 kΩ load	THD_{BUF}	- -	-100 -90	-95 -85	dB dB
Input Characteristics						
Bit Rate (TDATA)		f_{TDATA}	-	MCLK/8	-	bits/sec
Full Scale Bandwidth		BW_{FS}	-	200	-	Hz
Wideband Max Amplitude	(Note 1)	A_{WB}	-	-20	-	dBFS
One's Density Input Range	(Note 2)	IR_{OD}	25	-	75	%

Notes: 1. Max amplitude for operation above 200 Hz is TBSGAIN = 0x0078E5.

2. Specification guaranteed by design. These are the negative and positive full scale limits for the TDATA bitstream.

ANALOG CHARACTERISTICS (CONTINUED)

Parameter		Symbol	Min	Typ	Max	Unit
Analog Outputs						
Differential Output Level		V_{DIF}	-	-	5	V_{P-P}
Absolute Accuracy		ABS	-	±1	±2	%FS
Relative Accuracy		REL	-	±0.2	±1.8	%FS
Offset Error		VOS	-	-	1	%FS
Full Scale Drift	(Note 3)	FSD	-	5	-	ppm/°C
Offset Drift	(Note 3)	VOD	-	1	-	µV/°C
Analog Output Load at BUF±	Load Resistance Load Capacitance	R_L C_L	1 -	- -	- 100	kΩ pF
Voltage Reference Input						
VREF	(Note 4, 5)	$VREF_V$	-	2.5	-	V
VREF Current		$VREF_I$	-	-	120	µA
Power Supplies						
Power Supply Rejection	(Note 6)	PSRR	90	-	-	dB
DC Power Supply Currents	(Note 7 and 8)					
Normal Power Mode LPWR = 0; MCLK = 2.048 MHz	Analog Digital	VA VD	- -	7.8 100	- -	mA µA
Low Power Mode LPWR = 1; MCLK = 1.024 MHz	Analog Digital	VA VD	- -	5.0 100	- -	mA µA
Power Down Mode	Analog Digital	VA VD	- -	400 100	- -	µA µA
Sleep Mode	Analog Digital	VA VD	- -	2 2	- -	µA µA

3. Specification is for the parameter over the specified temperature range and is for the CS4373 only and does not include the effects of external components.
4. A 2.5 V voltage reference results in the highest dynamic range and best signal-to-noise performance, though smaller reference voltages may be used.
5. VREF is defined as {(VREF+) - (VREF-)} and Inputs must satisfy: VA- ≤ VREF- < VREF+ ≤ VA+
6. Power Supply Rejection is tested by applying a 100 mV_{P-P} 50 Hz signal to each supply.
7. All outputs unloaded. All digital inputs forced to VD or GND respectively. VA+ = 5 V; VA- = 0; VD+ = 3.3 V.
8. In Low Power Mode LPWR = 1, the Master Clock MCLK is reduced to 1.024 MHz. This reduces the signal bandwidth by a factor of 2.

DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	0.6 * VD	-	VD	V
Low-Level Input Voltage	V_{IL}	0.0	-	0.8	V
Input Leakage Current	I_{in}	-	±1	±10	µA

ABSOLUTE MAXIMUM RATINGS

CAUTION: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Max	Unit
DC Power Supplies (Note 9, 10)	Positive Digital Positive Analog Negative Analog	VD VA+ VA-	-0.3 -0.3 -3.3	+6.8 +6.8 +0.3	V V V
Input Current, Any Pin Except Supplies	(Note 11, 12)	I_{IN}	-	±10	mA
Input Current, Supplies	(Note 12)	I_{IN}	-	±50	mA
Output Current		I_{OUT}	-	±25	mA
Power Dissipation	(Note 13)	PDS	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	(VA-) - 0.5	(VA+) + 0.5	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.5	(VD) + 0.5	V
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

9. VA+ and VA- must satisfy {(VA+) - (VA-)} < +6.8 V.
10. VD and VA- must satisfy {(VD) - (VA-)} < +7.6 V.
11. Includes continuous over-voltage conditions at the analog input (AIN) pins.
12. Transient current of up to 100 mA can be safely tolerated without SCR latch-up.
13. Total power dissipation, including all input and output currents.

SWITCHING CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
MCLK Frequency (Note 14)	Normal Power Mode Low Power Mode	f_c	- -	2.048 1.024	- -	MHz MHz
MCLK Duty Cycle		DC_{CLK}	40	-	60	%
MCLK Jitter (In-band or aliased in-band)		CKJ_{IB}	-	-	300	ps
MCLK Jitter (Out-of-band)		CKJ_{OB}	-	-	1	ns
Rise Times:	Any Digital Input	t_{rise}	-	-	50	ns
Fall Times:	Any Digital Input	t_{fall}	-	-	50	ns
SYNC Setup Time to MCLK falling	(Note 15)	t_{mss}	20	-	-	ns
SYNC Hold Time after MCLK falling		t_{msh}	20	-	-	ns

Notes: 14. If MCLK is removed, the CS4373 enters a sleep mode state.

15. SYNC latched on MCLK falling edge, data output on next MCLK rising edge.

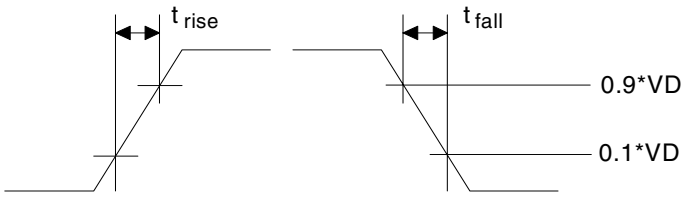


Figure 1. Rise and Fall Times

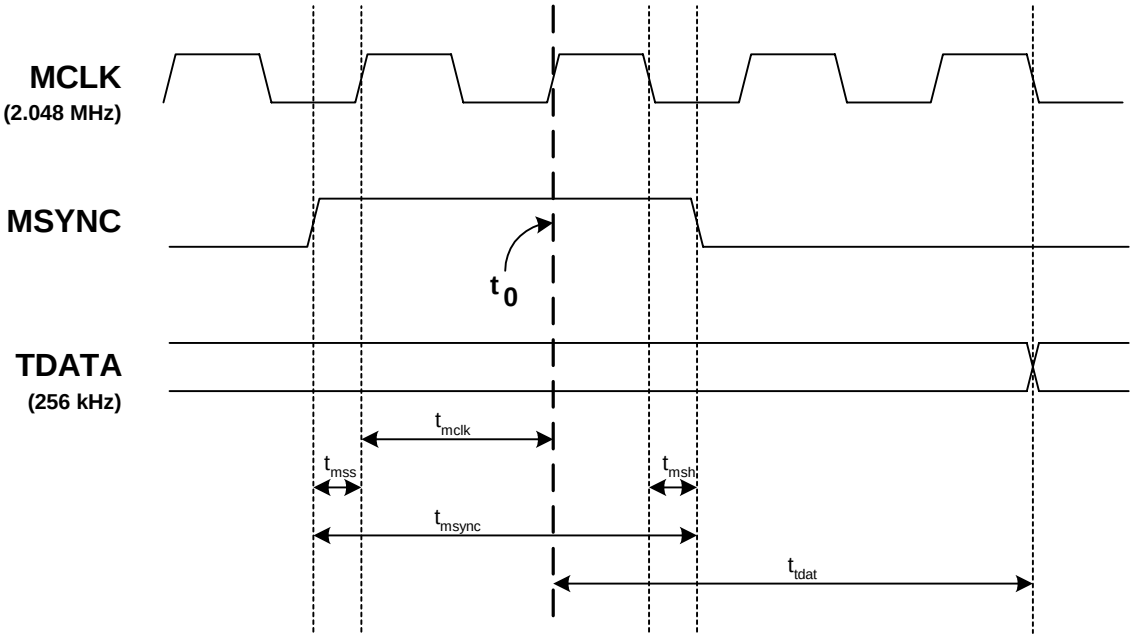


Figure 2. Timing

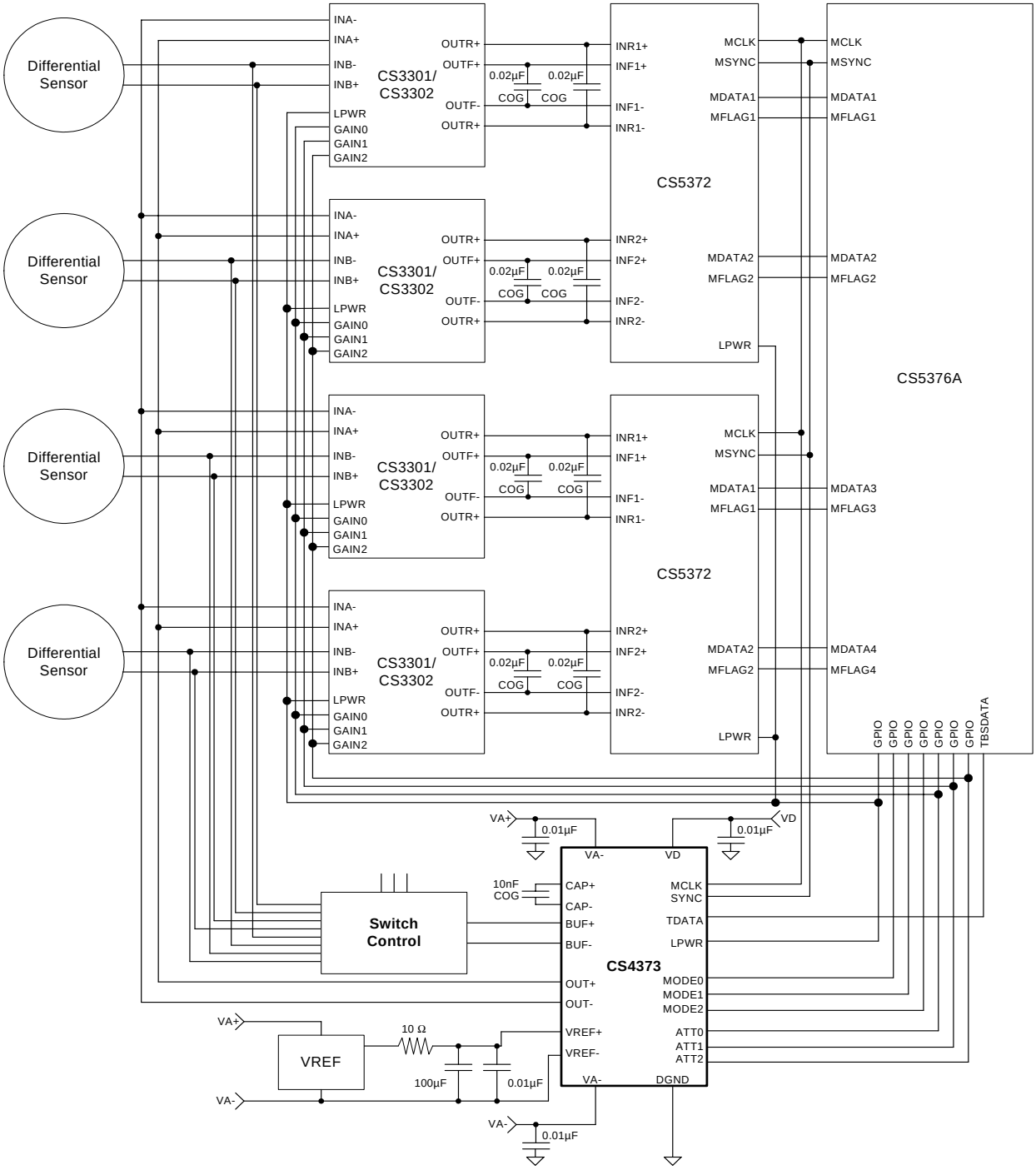


Figure 4. CS4373 System Connections

2. TERMINOLOGY

- *Dynamic Range (Signal-to-Noise Ratio)* - Ratio of the rms magnitude of the theoretical full scale signal to the integrated rms noise from DC to 400 Hz. The following formula is used to calculate this value:

$$SNR = 20\log\left(\frac{\text{rms magnitude of full scale signal}}{\text{rms magnitude of noise floor}}\right)$$

- *Total Harmonic Distortion* - Ratio of the power of the fundamental frequency to the sum of the powers of all harmonic frequencies from DC to 400 Hz. The following formula is used to calculate this value:

$$THD = 10\log\left(\frac{\text{sum of the powers of the harmonic frequencies}}{\text{power of the fundamental frequency}}\right)$$

- *Full Scale Bandwidth* - The bandwidth in which the converter can generate a full scale signal while maintaining all performance specifications.
- *Wideband Max Amplitude* - The maximum amplitude of the output signal beyond the full scale band-width.
- *Differential Output Level* - The peak-to-peak voltage between the analog output pins of the converter.
- *Absolute Accuracy* - Variation in the measured output voltage from the theoretical output voltage at each of the attenuation ranges. The following formula is used to calculate this value:

$$\text{absolute accuracy} = \left|\left(\frac{\text{measured attenuated voltage - theoretical attenuated voltage}}{\text{theoretical attenuated voltage}}\right)\cdot 100\%\right|$$

- *Relative Accuracy* - Variation in the measured output voltage from the theoretical output voltage (relative to measured full scale signal with no attenuation) at each of the attenuation ranges. The following formula is used to calculate this value:

$$\text{relative accuracy} = \left|\left(\frac{\text{measured attenuated voltage - theoretical attenuated voltage}}{\text{theoretical attenuated voltage (relative to the measured full scale voltage)}}\right)\cdot 100\%\right|$$

- *Offset Error* - Variation from the theoretical common mode voltage generated by the converter. The following formula is used to calculate this value:

$$\text{offset error} = \left|\left(\frac{\text{measured offset}}{\text{theoretical full scale voltage}}\right)\cdot 100\%\right|$$

- *Full Scale Drift* - The variation of the measured full scale voltage across the specified temperature range.
- *Offset Drift* - The variation in the measured offset voltage across the specified temperature range.

3. GENERAL DESCRIPTION

The CS4373 DAC is designed to fully verify the performance of the acquisition channel. Also, the input switching arrangements allows for verification of sensor source impedance and, in the case a moving-coil geophone, basic parameters of the electro-mechanical transfer function.

Test signals are typically generated by the CS5376A or CS5378 digital filter. The CS5376A/78 supplies TDATA with a ΔΣ bitstream at a rate of MCLK/8. The DAC reconstructs the digital bitstream to analog.

The full scale output voltage of the DAC matches the maximum input signal rating of the CS3301 and the CS3302 amplifier. A passive, programmable attenuator provides output levels that matches all gain settings of CS3301 and CS3302 while preserving the S/N of the DAC.

The DAC can be operated at full scale for signal frequencies up to 200 Hz. For frequencies above 200 Hz the amplitude must be reduced to -20 dB with respect to full scale.

4. ANALOG OUTPUTS

4.1 CAP+ / CAP-

The CS4373 DAC needs an anti-alias filter to function properly. The filter is constructed with resistors internal to the CS4373 and a capacitor connected the CAP+ and CAP- pins. This filter will eliminate out of band signals from the OUT± and BUF± outputs.

A 10 nF COG capacitor is required across CAP±; other types of capacitors, such as X7R, do not have the stability required. Using the 10 nF COG sets the -3 dB corner of the output anti-alias filter to 40 kHz.

4.2 OUT+ / OUT-

The OUT± pins are high precision, high output impedance differential outputs designed to test external electronics within the chip set. These outputs directly interface to the CS3301 and CS3302 for multiple test modes (See Figure 4 on page 8 for typical connection). These outputs can be attenuated to match the gain ranges of the CS3301/3302 using ATT0, ATT1, and ATT2.

4.3 BUF+ / BUF-

BUF± are buffered differential outputs used to test external sensors such as hydrophones or geophones. These outputs are also attenuated internally with the ATT0, ATT1 and ATT2 pins to match the gain ranges of the CS3301 and CS3302 (See Figure 4 on page 8 for typical connection).

5. DIGITAL FILTER INTERFACE

The CS4373 is designed to operate with the CS5376A or CS5378 digital filter. The CS5376A/78 generates the master clock (MCLK), the ΔΣ test bitstream (TDATA) and the synchronization signal input (SYNC). Each of these can be configured within the digital filter to fit the application requirements.

5.1 Signal Bitstream Input - TDATA

TDATA is the test bitstream input for the CS4373. It is a ΔΣ one's density bitstream input at a rate of MCLK/8. The digital filter has a bitstream available on its TBSDATA pin. When used with the CS5376A/78, TDATA can be connected directly to TBSDATA for it's bitstream generation.

5.2 Master Clock - MCLK

For proper operation, the CS4373 must be provided with a CMOS compatible clock on the MCLK pin. MCLK must have less than 300 ps of in-band jitter to maintain full performance specifications.

When used with the CS5376A/78 digital filters, MCLK is automatically generated and is typically 2.048 MHz or 1.024 MHz.

5.3 Clock Sync Input - SYNC

To synchronize the timing of the digital input bitstream, the CS4373 uses a SYNC signal. When using the CS5376A/78 digital filters, SYNC is automatically generated from a SYNC signal input from the external system.

The CS4373 SYNC input is rising edge triggered and resets the internal MCLK counter-divider.

6. VOLTAGE REFERENCE

6.1 Voltage Reference Inputs

The CS4373 is designed to operate with a 2.5 V voltage reference applied across the VREF+ and VREF- pins.

In a single supply power configuration the VREF+ pin should be connected to the voltage reference output, and the VREF- pin connected to ground. In a dual supply power configuration the voltage reference should be powered from the VA+ and VA- supplies, with the VREF+ pin connected to the voltage reference output and the VREF- pin connected to VA-. Because most 2.5 V voltage references require a power supply voltage greater than 3 V to operate, when powering the voltage reference from dual ±2.5 V supplies the reference voltage into the VREF+ pin should be defined relative to the VA- supply (see Figure 5).

The selected voltage reference should produce less than 1 µVrms of noise in the measurement bandwidth on the VREF+ pin. The digital filter output word rate selection determines the bandwidth over which voltage reference noise affects the CS4373 dynamic range.

6.2 Voltage Reference Configurations

For a 2.5 V reference, the Linear Technology LT1019-2.5 voltage reference yields low enough noise if the output is filtered with a low pass RC filter as shown in Figure 5.

6.3 VREF Input Impedance

The switched-capacitor input architecture of the VREF+ pin causes the input current required from the voltage reference to change any time MCLK is changed. The input impedance of the voltage reference input is calculated similar to the analog signal input impedance as [1 / (f * C)] where f is the master clock frequency, MCLK, and C is the internal sampling capacitor. A 2.048 MHz MCLK yields a voltage reference input impedance of approximately [1 / (2.048 MHz)*(20 pF)], or about 24 kΩ.

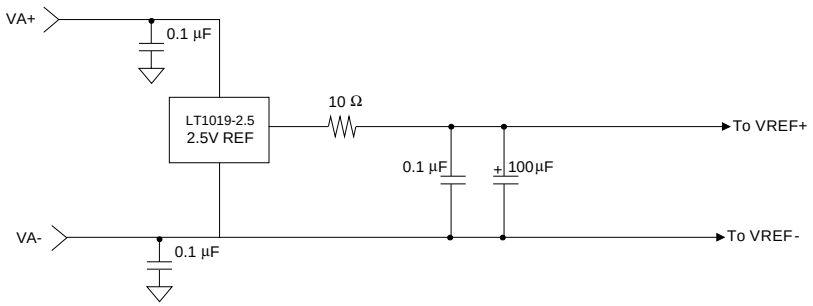


Figure 5. 2.5 Voltage Reference Circuit

6.4 Gain Accuracy

Gain accuracy of the CS4373 is affected by variations of the voltage reference input. A change in the voltage reference input impedance due to a change in MCLK could affect gain accuracy when using the higher source impedance configuration of Figure 5. The VREF+ pin input impedance and the external low-pass filter resistor create a voltage divider for the output reference voltage, reducing the effective voltage reference input. If gain error is to be minimized, especially when MCLK is to be changed, the voltage reference should be buffered to have a low output impedance to minimize the effect of the resistive voltage divider.

6.5 Gain Drift

Gain drift of the CS4373 due to temperature does not include the temperature drift characteristics of the external voltage reference. Gain drift is not affected by the sample rate or by power supply variations.

7. TEST MODES

The CS4373 has 7 test modes. The MODE0, MODE1, and MODE2 pins define which mode the part will operate. Table 1 lists the test mode options and corresponding MODE pin settings.

The following subsections explain the CS4373 Test Mode Options:

7.1 Test Mode 0: Reserved

7.2 Test Mode 1: Sensor Test Mode

This mode is used to test an external sensor such as a hydrophone or geophone. Both the BUF± and OUT± are active outputs; and impulse response, linearity, and sensor impedance can be measured in the Sensor Test Mode. See Figure 6 for a typical connection diagram.

	MODE2	MODE1	MODE0	
Test Mode 0	0	0	0	Reserved
Test Mode 1	0	0	1	Sensor Test Mode (OUT± AND BUF±)
Test Mode 2	0	1	0	Electronics Test (OUT± ONLY)
Test Mode 3	0	1	1	Sensor Test (BUF± ONLY)
Test Mode 4	1	0	0	Common Mode
Test Mode 5	1	0	1	High Voltage/High Current Mode
Test Mode 6	1	1	0	Reserved
Test Mode 7	1	1	1	Sleep Mode

Table 1. Test Modes

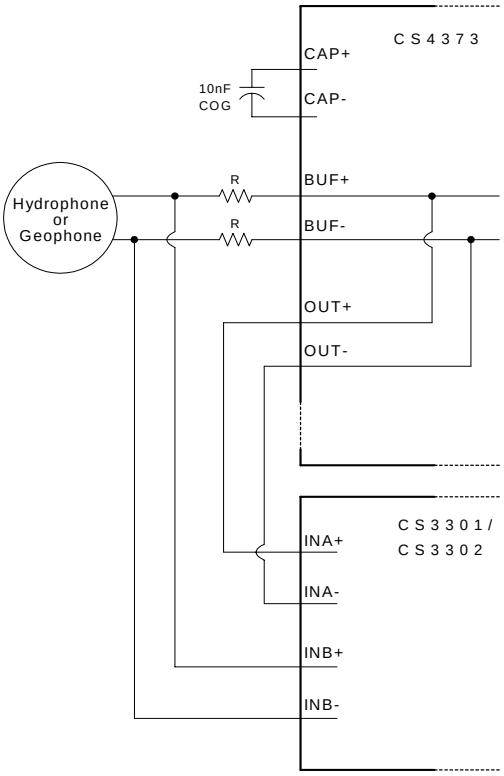


Figure 6. Test Mode 1

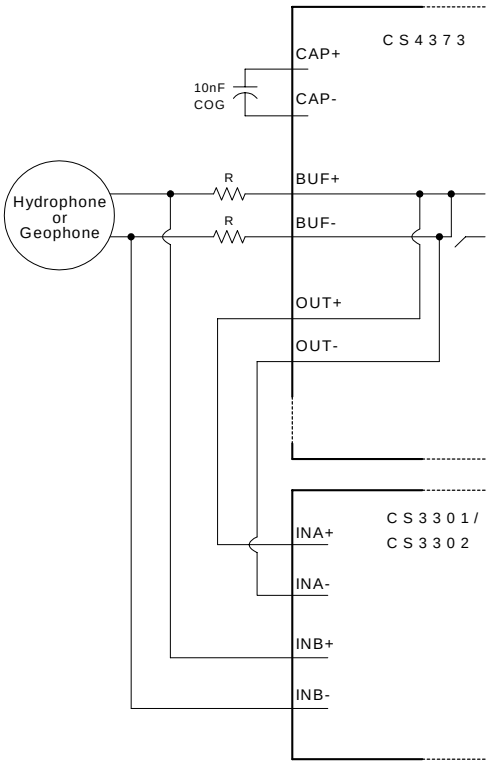


Figure 7. Test Mode 4

By placing known resistances on both BUF+ and BUF- (each side of the sensor) the voltage at the buffered outputs (BUF+ and BUF-) can be measured through the CS3301 or CS3302 and compared to the voltage on the precision outputs (OUT+ and OUT-). From these measurements the leakage current of the sensor can be determined

Linearity can also be measured from the output of OUT±. And when connected to the digital filter, a digital impulse bitstream can be fed directly to the CS4373 to test the impulse response of the system.

7.3 Test Mode 2: Electronics Test Mode

In this test mode, outputs BUF± are high-Z and only OUT± is available. BUF± become high impedance to protect any external sensors still connected. This mode can be used to test other system electronics on the board. It should be noted that since only OUT± can be used in this mode, and OUT± are unbuffered outputs, OUT± can only be connected to a high impedance load, such as the CS3301 and CS3302 amplifiers.

7.4 Test Mode 3: Sensor Test Mode

As opposed to Test Mode 1, in this mode BUF± are the only available outputs. This mode offers another option to test external circuitry. While operating in Test Mode 3, OUT± are high impedance to ensure no interference.

7.5 Test Mode 4: Common Mode

In this mode the system can be tested using a common mode output from both BUF± and OUT±. Figure 7 shows BUF± and OUT± connections internal to the CS4373. Again, since the OUT± pins are unbuffered, they must only be connected to a high impedance load, such as the CS3301 and CS3302.

7.6 Test Mode 5: High Voltage/High Current Mode

This mode allows connection of the OUT± pins to high voltage or high current electronics. Figure 8 shows a typical connection diagram for this operational mode. The CS3301 and CS3302 amplifiers can be used in the configuration as the precision buffers. When using the circuit in Figure 8, the gain of the circuit is defined as:

$$A_V = \frac{V_2}{V_1} = \left(1 + \frac{2R_1}{R_2}\right)$$

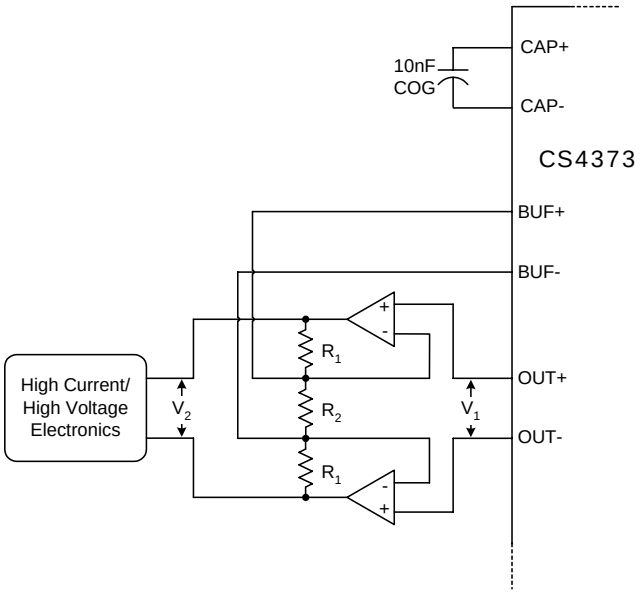


Figure 8. Test Mode 5

7.7 Test Mode 6: Reserved

7.8 Test Mode 7: Sleep Mode

In this mode the chip is put into a low power sleep mode (See Section 9, "Power Modes" on page 15 for more).

8. ATTENUATION SETTINGS

The DAC outputs can be attenuated to match the gain ranges of the CS3301 and CS3302 amplifiers. Using pins ATT0, ATT1 and ATT2, the outputs of the DAC can be set to one of 7 attenuation options. Table 2 shows each attenuation option.

Attenuation Selection	ATT2	ATT1	ATT0
1	0	0	0
1/2	0	0	1
1/4	0	1	0
1/8	0	1	1
1/16	1	0	0
1/32	1	0	1
1/64	1	1	0
Reserved	1	1	1

Table 2. Attenuator Selection

9. POWER MODES

Five power modes are available when using the CS4373. Normal, low power modes are operational modes; power down and sleep mode are non-operational standby modes.

9.1 Normal Power Mode

The normal operational mode for the CS4373, LPWR=0 and MCLK=2.048 MHz, provides the best performance with low power consumption. This power mode is recommended when maximum performance is required.

9.2 Low Power Mode

The CS4373 has a low-power operational mode, LPWR = 1 and MCLK = 1.024 MHz, that reduces power consumption at the expense of 3 dB SNR. This operational mode is recommended when minimizing power is more important than maximizing SNR.

9.3 Sleep Mode

When selecting Test Mode 7, the CS4373 will be put in a sleep mode in which the DAC is inactive. Each analog output is placed into a high impedance state.

9.4 Power Down

The CS4373 is automatically placed into power down if MCLK is disabled. It is equipped with loss of clock detection circuitry to force power down if MCLK is removed. In power down the DAC is inactive and the analog outputs are placed in a high impedance state. When used with the CS5376A or CS5378 the CS4373 will be in this state upon power-up since MCLK is disabled by default.

10. POWER SUPPLY

The CS4373 has one positive analog power supply pin, VA+, one negative analog power supply pin, VA-, one digital power supply pin, VD, and one digital ground pin, DGND. The analog and digital circuitry are separated internally to enhance performance, therefore power must be supplied to all three supply pins. The digital ground pin must be connected to system ground.

When used with the CS5376A or CS5378 digital filter the maximum voltage differential between the CS4373 digital supply, VD, and the I/O supplies, (VDD1, VDD2, VDDPAD) must be 0.3 V or less.

10.1 Power Supply Bypassing

The analog supply pins, VA+, VA-, should be decoupled to system ground with a 0.1 µF capacitor; while the digital supply pin, VD, should be decoupled to system ground with a 0.01 µF capacitor. Bypass capacitors can be X7R, tantalum, or any other dielectric types.

10.2 SCR Latch-up Considerations

The VA- pin is tied to the CS4373 CMOS substrate and should always be connected to the most negative supply voltage to ensure SCR latch-up does not occur. In general, latch-up may occur when any pin voltage (including the analog inputs) is 0.7 V or more below VA-, or 7.6 V or more above VA-.

When using dual analog power supplies, it is recommended to connect the VA- power supply pin to system ground (DGND) using a reversed biased Schottky diode. This configuration clamps the VA- voltage a maximum of 0.3 V above ground to ensure SCR latch-up does not occur during power up. If the VA+ power supply ramps before the VA- supply, the VA- voltage could be pulled above ground through the CS4373. If the VA- supply is unintentionally pulled 0.7 V above the DGND pin, SCR latch-up can occur.

10.3 DC-DC Converter Considerations

Many low-frequency measurement systems are battery powered and utilize DC-DC converters to efficiently generate power supply voltages. To minimize interference effects, operate the DC-DC converter at a frequency which is rejected by the digital filter, or operate it synchronous to the MCLK rate.

A synchronous DC-DC converter whose operating frequency is derived from MCLK will theoretically minimize the potential for “beat frequencies” to appear in the measurement bandwidth. However this requires the source clock to remain jitter-free within the DC-DC converter circuitry. If clock jitter can occur within the DC-DC converter (as in a PLL-based architecture), it’s better to use a non-synchronous DC-DC converter whose switching frequency is rejected by the digital filter.

During PCB layout, do not place high-current DC-DC converters near sensitive analog components. Carefully routing a separate DC-DC “star” ground will help isolate noisy switching currents away from the sensitive analog components.

10.4 Power Supply Rejection

Power supply rejection of the CS4373 is frequency dependent. The digital filter rejects power supply noise for frequencies above the filter corner frequency at 130 dB or greater. For frequencies between DC and the digital filter corner frequency, power supply rejection is nearly constant at 90 dB.

11.PIN DESCRIPTION

Positive Capacitor Output	**CAP+**	1	28	**LPWR**	Low Power Mode Enable
Negative Capacitor Output	**CAP-**	2	27	**MODE0**	Mode Select
Positive Buffered Output	**BUF+**	3	26	**MODE1**	Mode Select
Negative Buffered Output	**BUF-**	4	25	**MODE2**	Mode Select
Positive High Precision Output	**OUT+**	5	24	**ATT0**	Attenuation Range Select
Negative High Precision Output	**OUT-**	6	23	**ATT1**	Attenuation Range Select
Positive Analog Power Supply	**VA+**	7	22	**ATT2**	Attenuation Range Select
Negative Analog Power Supply	**VA-**	8	21	**TDATA**	Signal Bitstream Input
Negative Voltage Reference	**VREF-**	9	20	**VD**	Positive Digital Power Supply
Positive Voltage Reference	**VREF+**	10	19	**DGND**	Digital Ground
No Connect	**NC**	11	18	**MCLK**	Master Clock Input
No Connect	**NC**	12	17	**SYNC**	Clock Sync Input
No Connect	**NC**	13	16	**DNC**	Do Not Connect
No Connect	**NC**	14	15	**DNC**	Do Not Connect

Pin Name	Pin #	I/O	Pin Description
CAP+, CAP-	1, 2	**O**	External Capacitor Connection for Test DAC anti-alias filter
BUF+, BUF-	3, 4	**O**	Buffered Output from the Test DAC
OUT+, OUT-	5, 6	**O**	High precision output from the Test DAC
VA+, VA-	7, 8	**I**	Power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VREF-, VREF+	9, 10	**I**	Voltage reference for the internal sampling circuits. Refer to the Recommended Operating Conditions for appropriate voltages.
SYNC	17	**I**	Clock Sync Input - A low to high transition resets the internal clock phasing of the DAC.
MCLK	18	**I**	Master Clock Input - a CMOS compatible clock input for the DAC internal master clock.
DGND	19	**I**	Digital Ground - Ground reference for the digital section.
VD	20	**I**	Power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
LPWR	28	**I**	Low Power Mode Select - When set high the CS4373 enters into a Low Power Mode. (See Section Section 9, "Power Modes" on page 15 for more on Power Modes)
TDATA	24	**I**	Test DAC Signal Bitstream Input.

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>I/O</th><th>Pin Description</th></tr>
<tr><td>ATT2, ATT1, ATT0</td><td>21, 22, 23</td><td>I</td><td>Attenuation Range Select - Selects the internal attenuation range as detailed in Table 3.
<table>
<tr><th>Attenuation Selection</th><th>ATT2</th><th>ATT1</th><th>ATT0</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1/2</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1/4</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1/8</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1/16</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1/32</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1/64</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>reserved</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Table 3. Attenuator Selection</td></tr>
<tr><td>MODE2, MODE1, MODE0</td><td>25, 26, 27</td><td>I</td><td>Mode Selection - Determines the operational mode (0 - 7) of the device as detailed in Table 4.
<table>
<tr><th>Mode Selection</th><th>Mode</th><th>MODE2</th><th>MODE1</th><th>MODE0</th></tr>
<tr><td>Test Mode 0</td><td>Reserved</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Test Mode 1</td><td>Sensor Test</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Test Mode 2</td><td>OUT±</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Test Mode 3</td><td>BUF±</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Test Mode 4</td><td>Common Mode</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Test Mode 5</td><td>High Voltage</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Reserved</td><td>Reserved</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Test Mode 7</td><td>Chip Power Down</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Table 4. Mode Selection</td></tr>
</table>

12.ORDERING INFORMATION

Model	Temperature	Package
CS4373-IS	-40 to +85 °C	28-pin SSOP

13.ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS4373-IS	240 °C	2	365 Days

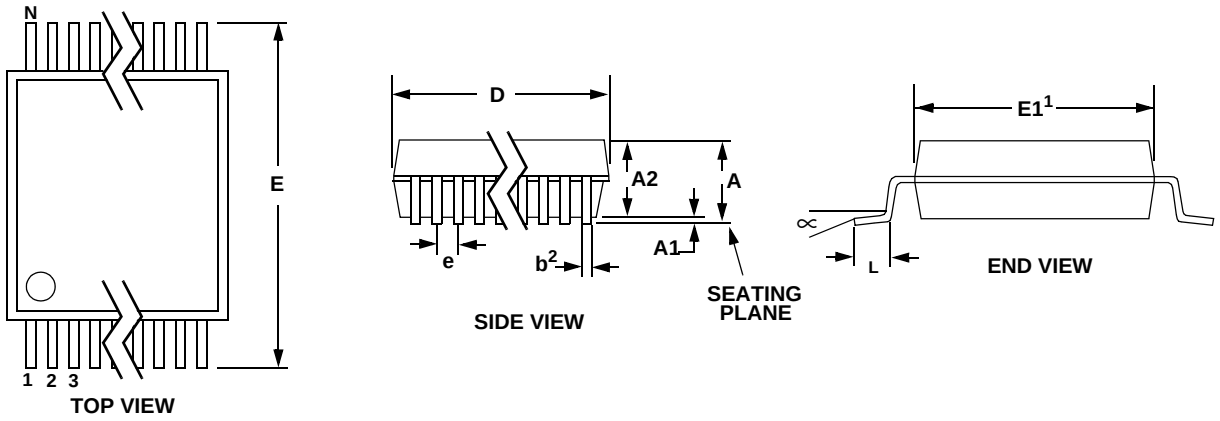
* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

14.REVISION HISTORY

Revision	Date	Changes
PP1	MAR 2003	Initial preliminary release.
F1	SEP 2005	Final version. MSL data added.

15.PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.