



Glass-passivated silicon thyristors in metal envelopes, intended for use in power control circuits (e.g. light and motor control) and power switching systems.

The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTW38–600R to 1000R.

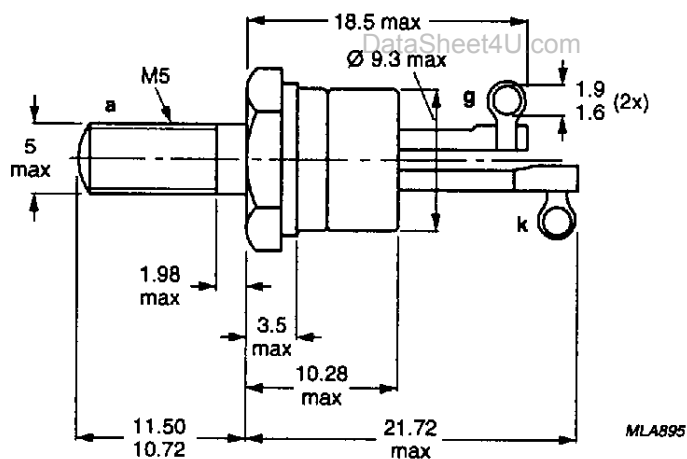
### QUICK REFERENCE DATA

		BTW38–600R	800R	1000R	
Repetitive peak voltages	$V_{DRM}/V_{RRM}$ max.	600	800	1000	V
Average on-state current	$I_{T(AV)}$ max.	10			A
R.M.S. on-state current	$I_{T(RMS)}$ max.	16			A
Non-repetitive peak on-state current	$I_{TSM}$ max.	150			A

### MECHANICAL DATA

Dimensions in mm

Fig.1 TO-64: with metric M5 stud ( $\phi 5$  mm); e.g. BTW38–600R.



Net mass: 7 g

Diameter of clearance hole: max. 5.2 mm

Accessories supplied on request:

see ACCESSORIES section

Supplied with device: 1 nut, 1 lock washer

Torque on nut: min. 0.9 Nm (9 kg cm)

max. 1.7 Nm (17 kg cm)

Nut dimensions across the flats: 8.0 mm.



Qualification approved to CECC 50 011-006.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		BTW38—600R			800R	1000R
<b>Anode to cathode</b>						
Non-repetitive peak voltages ( $t \leq 10$ ms)	$V_{DSM}/V_{RSM}$	max.	600	800	1000	V
Repetitive peak voltages	$V_{DRM}/V_{RRM}$	max.	600	800	1000	V
Crest working voltages	$V_{DWM}/V_{RWM}$	max.	400	600	700	V*
<b>Average on-state current (averaged over any 20 ms period) up to <math>T_{mb} = 85</math> °C</b>						
	$I_T(AV)$			max.	10	A
R.M.S. on-state current	$I_T(RMS)$			max.	16	A
Repetitive peak on-state current	$I_{TRM}$			max.	75	A
<b>Non-repetitive peak on-state current; <math>t = 10</math> ms; half sine-wave; <math>T_j = 125</math> °C prior to surge; with reapplied <math>V_{RWMmax}</math></b>						
	$I_{TSM}$			max.	150	A
$I^2 t$ for fusing ( $t = 10$ ms)	$I^2 t$			max.	112	A <sup>2</sup> s
<b>Rate of rise of on-state current after triggering with <math>I_G = 250</math> mA to <math>I_T = 25</math> A; <math>dI_G/dt = 0.25</math> A/<math>\mu</math>s</b>						
	$dI_T/dt$			max.	50	A/ $\mu$ s
<b>Gate to cathode</b>						
<b>Average power dissipation (averaged over any 20 ms period)</b>						
	$P_G(AV)$			max.	0.5	W
Peak power dissipation	$P_{GM}$			max.	5	W
<b>Temperatures</b>						
Storage temperature	$T_{stg}$				-55 to +125	°C
Junction temperature	$T_j$			max.	125	°C
<b>THERMAL RESISTANCE</b>						
From junction to mounting base	$R_{th j-mb}$	=			1.8	K/W
From mounting base to heatsink with heatsink compound	$R_{th mb-h}$	=			0.5	K/W
From junction to ambient in free air	$R_{th j-a}$	=			45	K/W
Transient thermal impedance ( $t = 1$ ms)	$Z_{th j-mb}$	=			0.1	K/W

**OPERATING NOTE**

The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.

During soldering the heat conduction to the junction should be kept to a minimum.

\*To ensure thermal stability:  $R_{th j-a} < 4$  K/W (d.c. blocking) or  $< 8$  K/W (a.c.). For smaller heat-sinks  $T_j$  max should be derated. For a.c. see Fig.3.

# CHARACTERISTICS

## Anode to cathode

On-state voltage (measured under pulse conditions)

$$I_T = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$$

$$V_T < 2 \text{ V}$$

Rate of rise of off-state voltage that will not trigger any device; exponential method;

$$V_D = 2/3 V_{DRMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$dV_D/dt < 200 \text{ V}/\mu\text{s}$$

Reverse current

$$V_R = V_{RWMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$I_R < 3 \text{ mA}$$

Off-state current

$$V_D = V_{DWMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$I_D < 3 \text{ mA}$$

Latching current;  $T_j = 25 \text{ }^\circ\text{C}$

$$I_L < 150 \text{ mA}$$

Holding current;  $T_j = 25 \text{ }^\circ\text{C}$

$$I_H < 75 \text{ mA}$$

## Gate to cathode

Voltage that will trigger all devices

$$V_D = 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{GT} > 1.5 \text{ V}$$

Voltage that will not trigger any device

$$V_D = V_{DRMmax}; T_j = 125 \text{ }^\circ\text{C}$$

$$V_{GD} < 200 \text{ mV}$$

Current that will trigger all devices

$$V_D = 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$$

$$I_{GT} > 50 \text{ mA}$$

## Switching characteristics

Gate-controlled turn-on time ( $t_{gt} = t_d + t_r$ ) when

switched from  $V_D = V_{DRMmax}$  to  $I_T = 40 \text{ A}$ ;

$$I_{GT} = 100 \text{ mA}; dI_G/dt = 5 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$$

$$t_{gt} \text{ typ. } 2 \mu\text{s}$$

Circuit-commutated turn-off time when switched

from  $I_T = 40 \text{ A}$  to  $V_R > 50 \text{ V}$  with

$$-dI_T/dt = 10 \text{ A}/\mu\text{s}; dV_D/dt = 50 \text{ V}/\mu\text{s}; T_j = 115 \text{ }^\circ\text{C}$$

$$t_q \text{ typ. } 35 \mu\text{s}$$

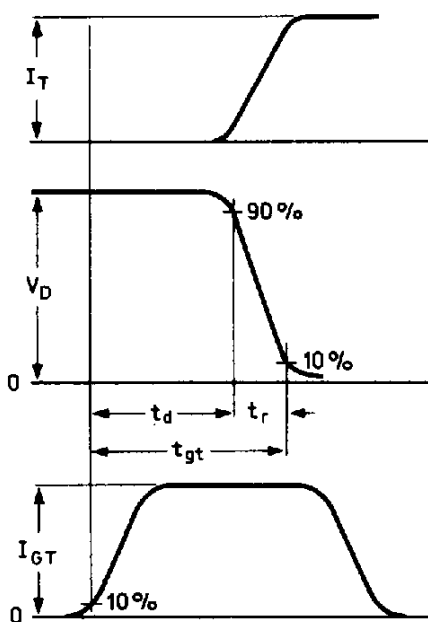


Fig.2a Gate-controlled turn-on time definition.

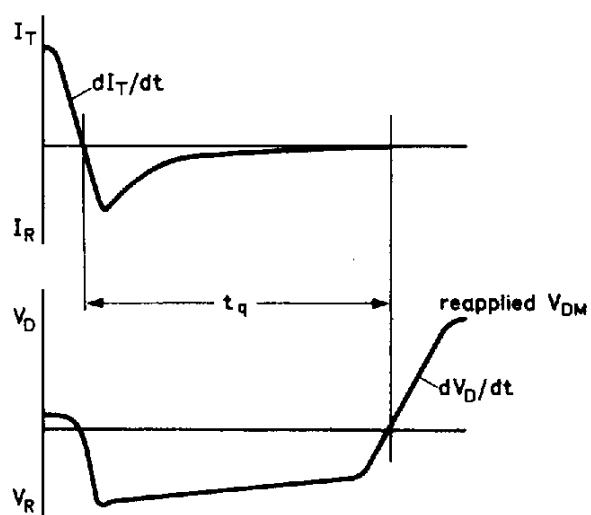


Fig.2b Circuit-commutated turn-off time definition.

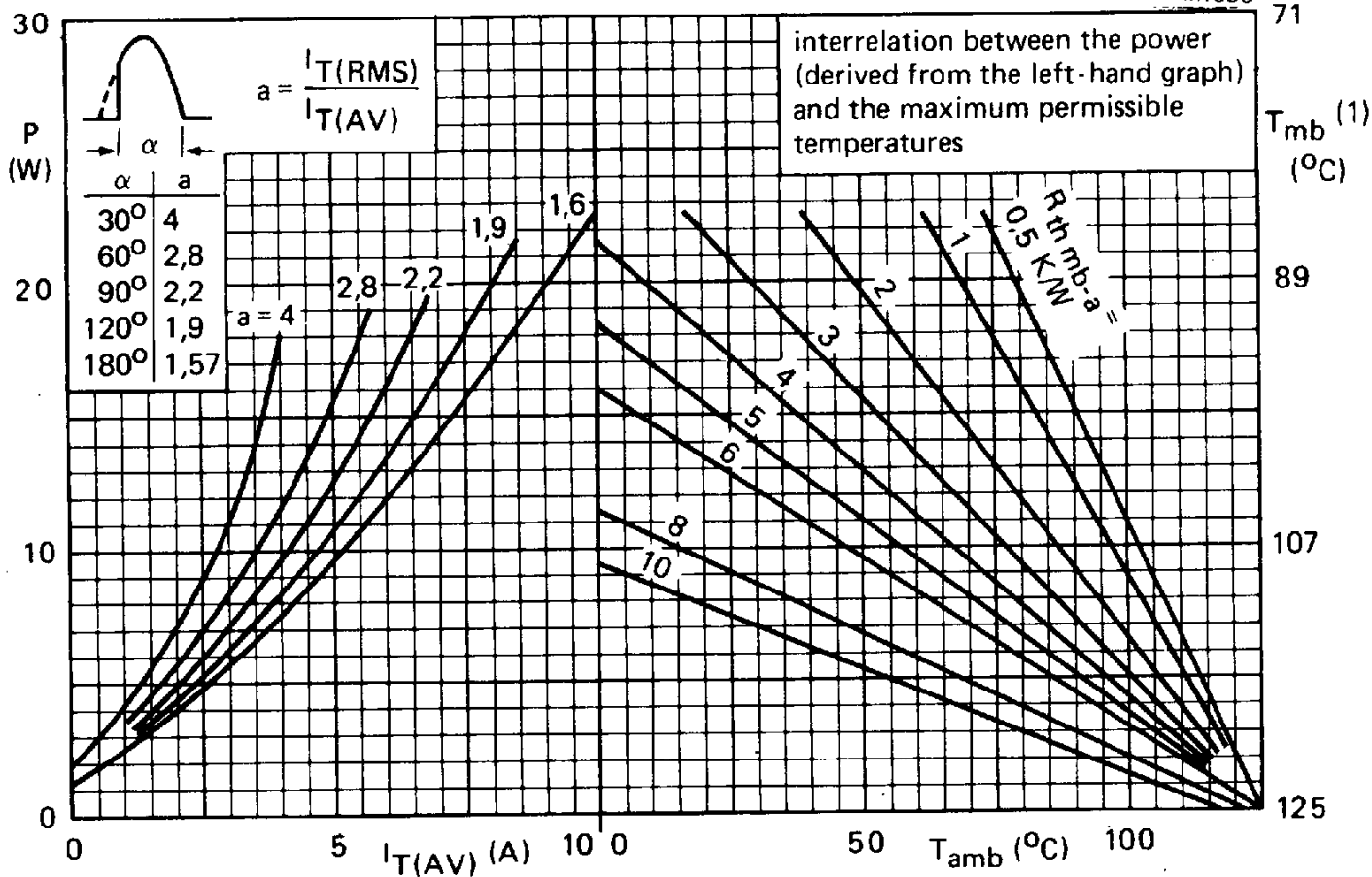


Fig. 3 (1)  $T_{mb}$ -scale is for comparison purposes only and is correct only for  $R_{th\ mb-a} \leq 6\ K/W$

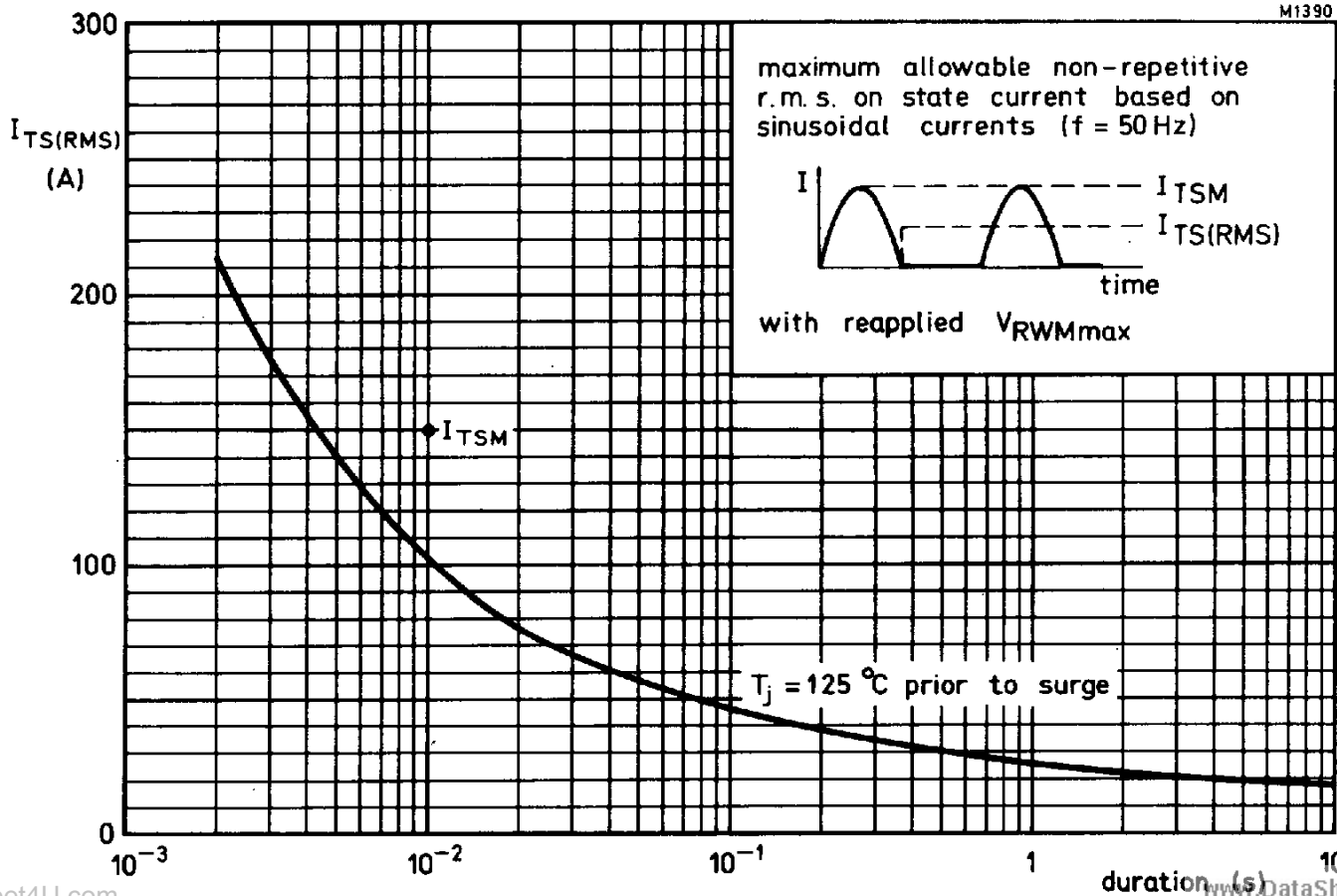


Fig. 4.

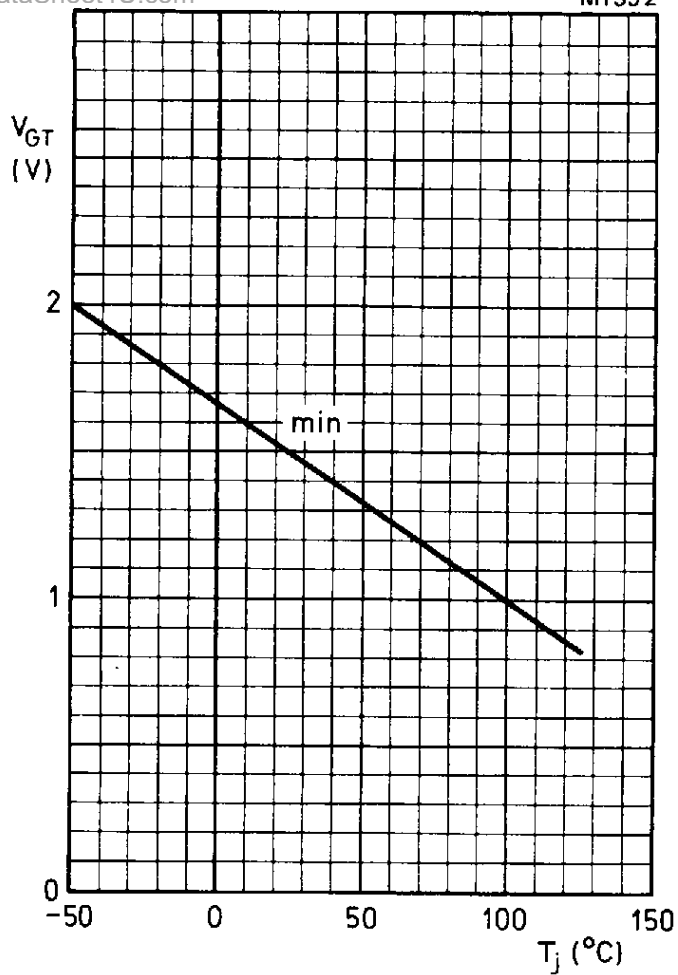


Fig. 5 Minimum gate voltage that will trigger all devices as a function of  $T_j$ .

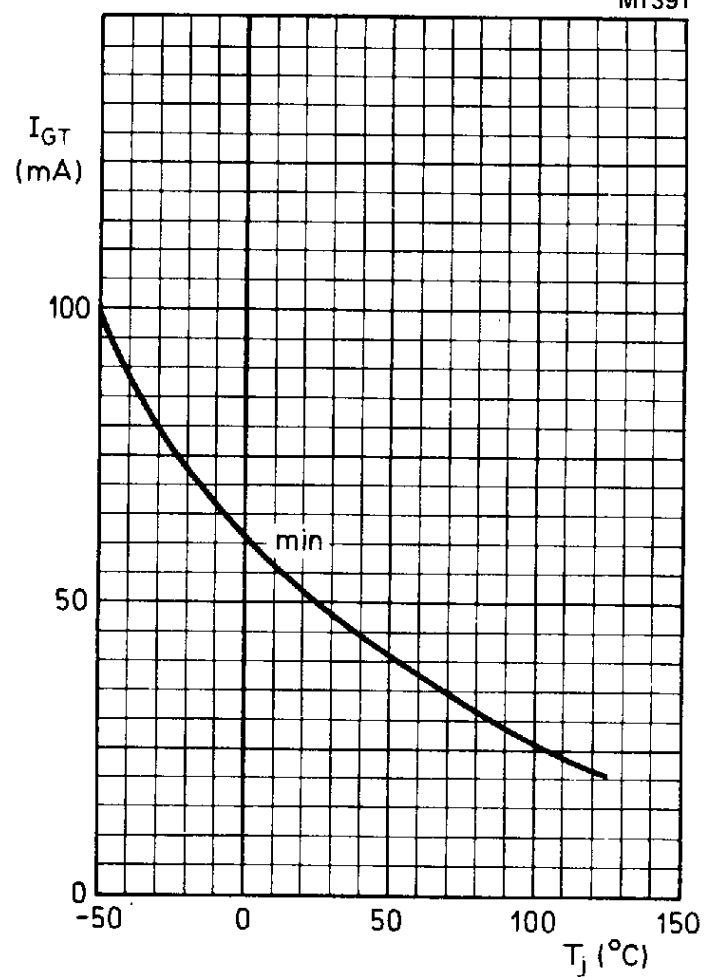


Fig. 6 Minimum gate current that will trigger all devices as a function of  $T_j$ .

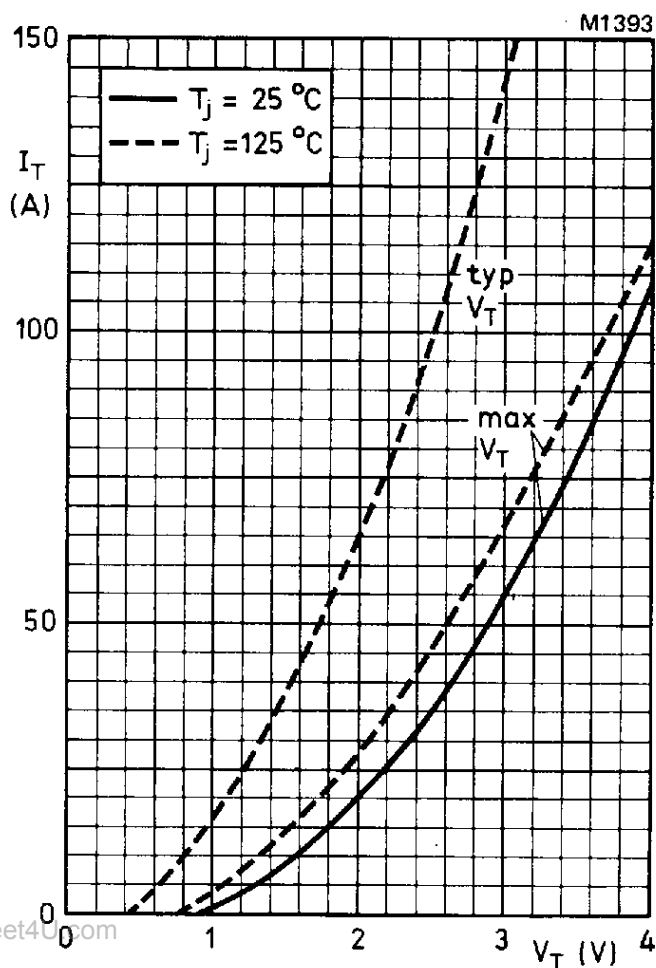


Fig. 7.

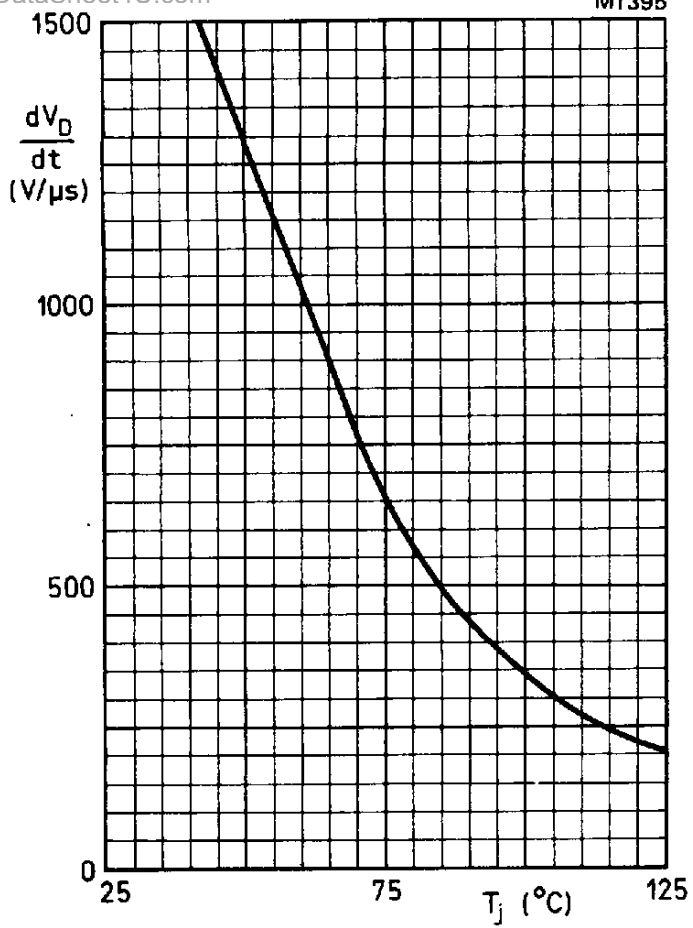


Fig. 8 Maximum rate of rise of off-state voltage that will not trigger any device (exponential method) as a function of  $T_j$ .

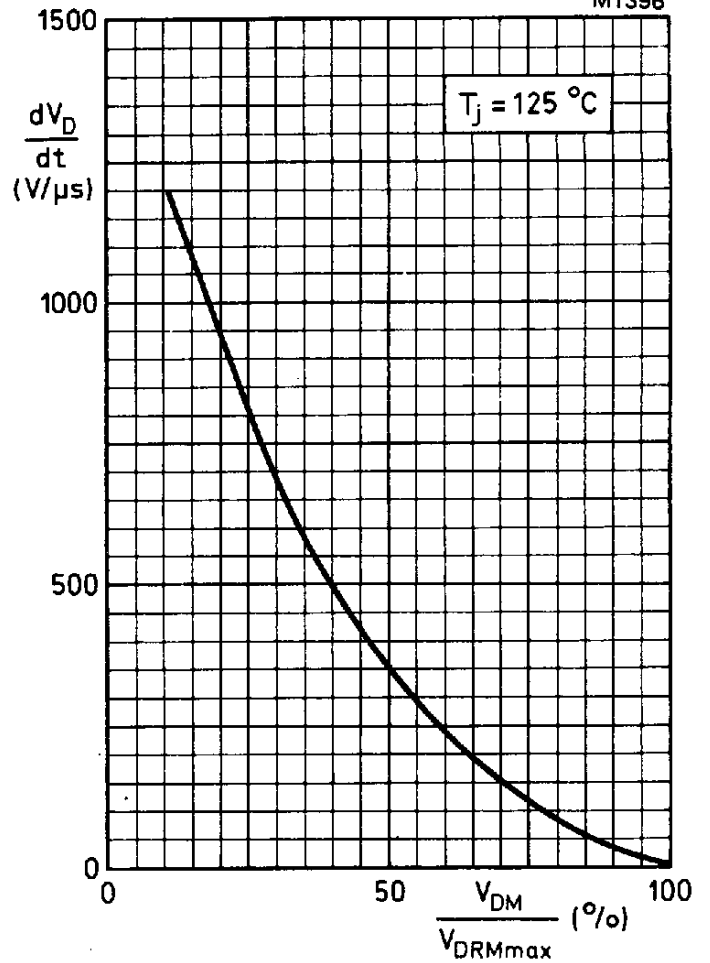


Fig. 9 Maximum rate of rise of off-state voltage that will not trigger any device (exponential method) as a function of applied voltage.

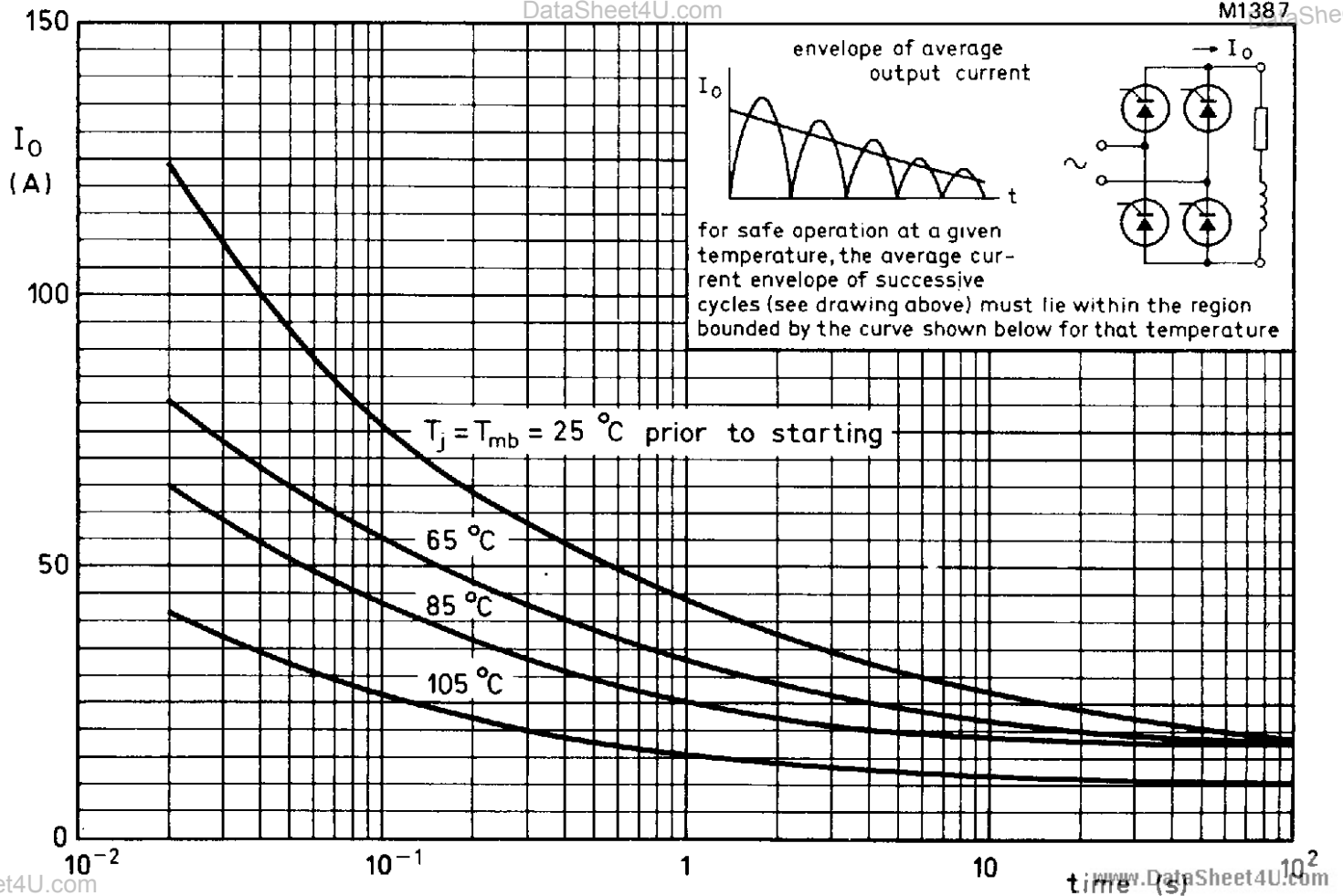
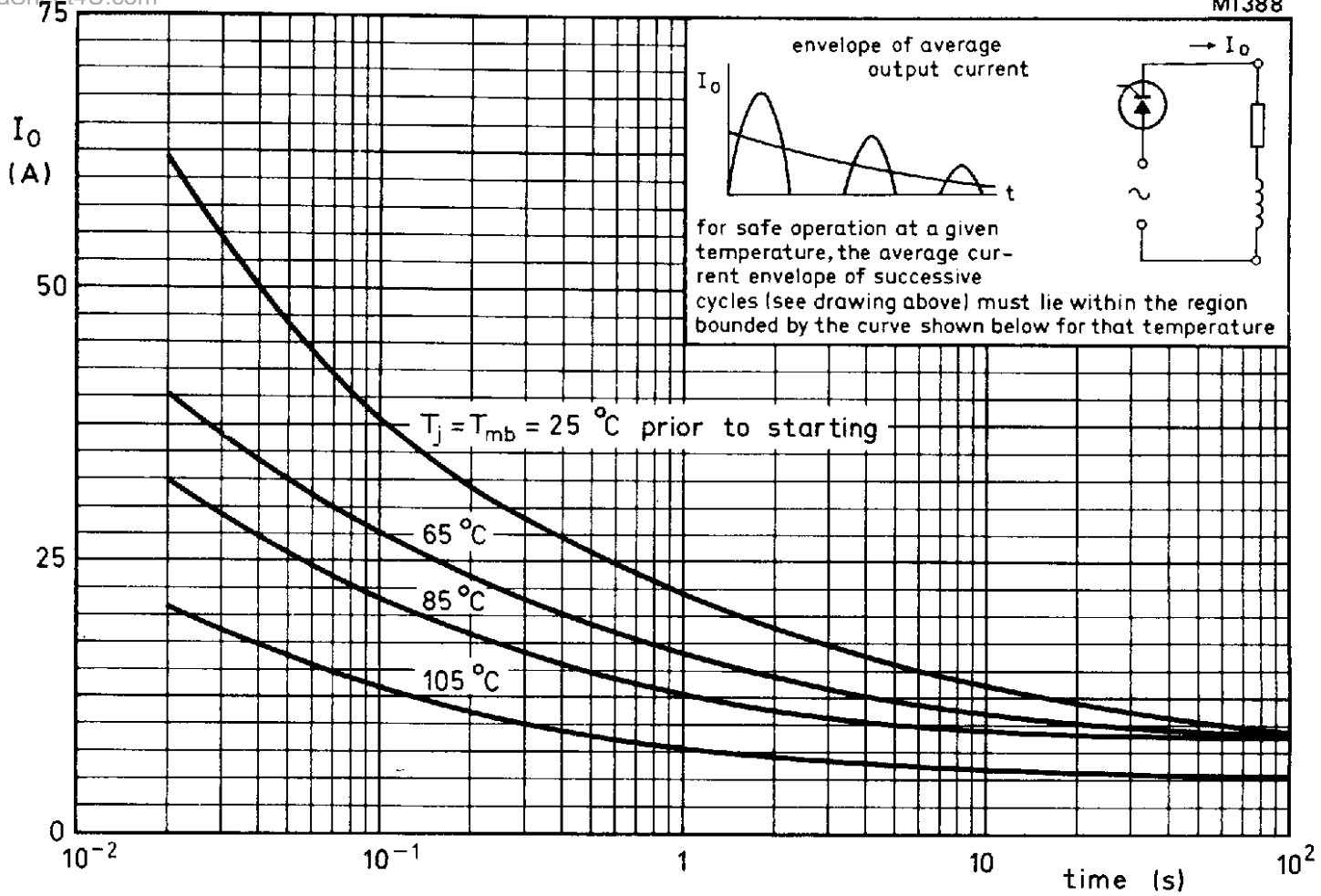


Fig. 10 Limits for starting or inrush currents.

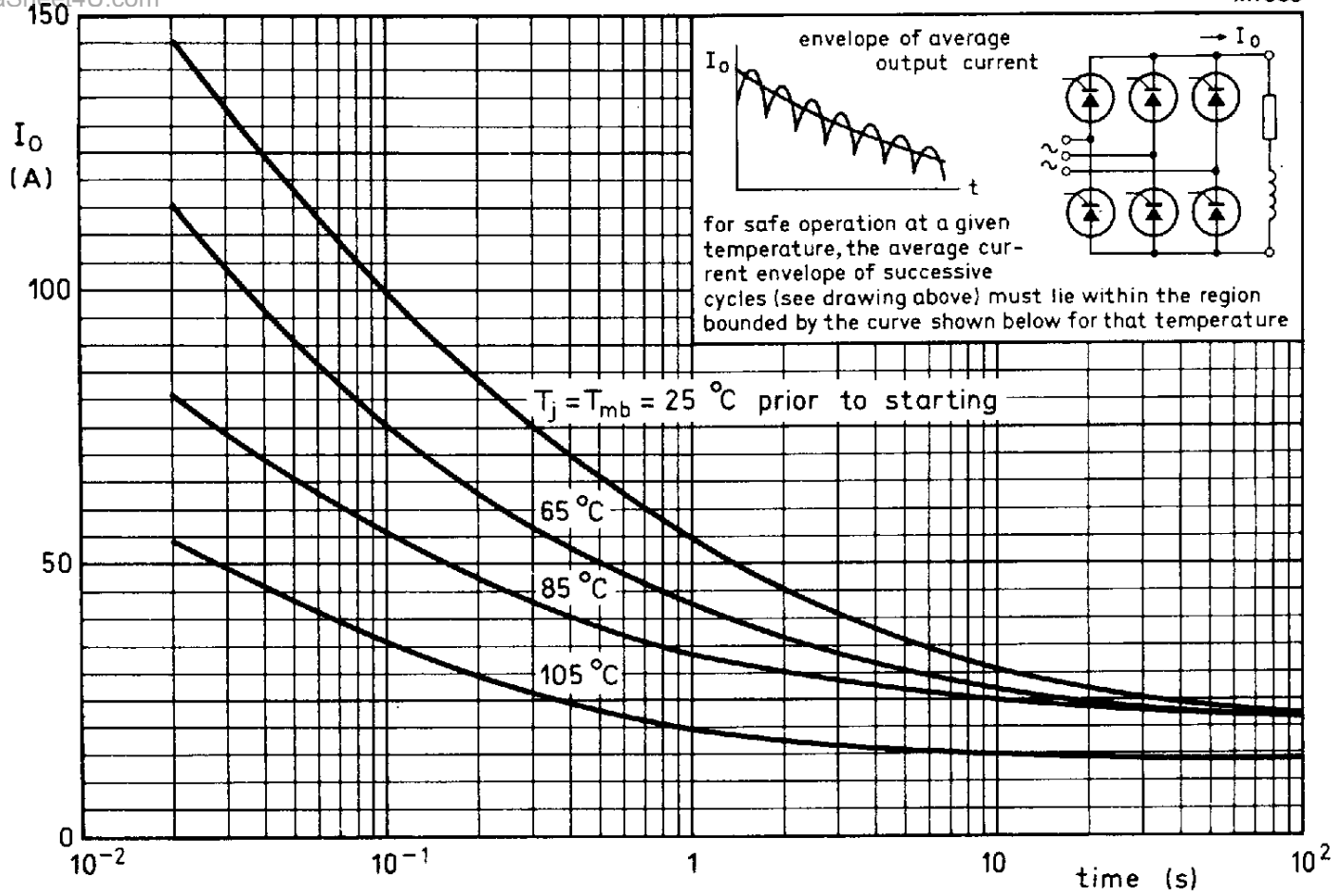


Fig. 11 Limits for starting or inrush currents.

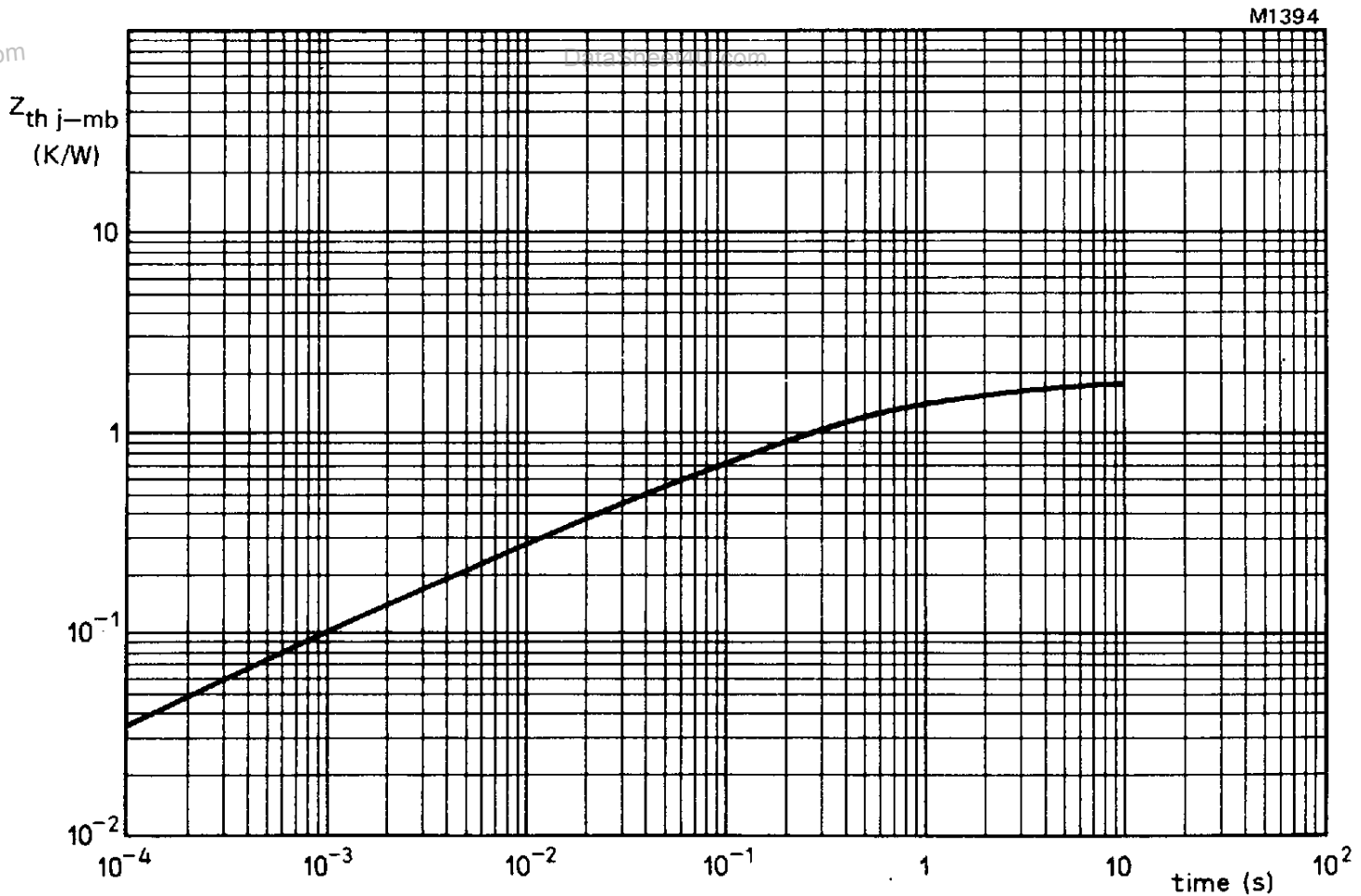


Fig. 12.