May 1990

BiMOS Precision Operational Amplifiers

Features:

- *Low V_{IO}: 200 µV max. (CA3493A)*
  500 µV max. (CA3493A)
- *Low $\Delta V_{IO}/\Delta T$: 3 µV/°C max. (CA3493A)*
  5 µV/°C max. (CA3493)
- *Low I_{IO} and I_I*
- *Low $\Delta/I_{IO}/\Delta T$: 150 pA/°C max. (CA3493)*
- *Low $\Delta/I_I/\Delta T$: 3.7 nA/°C max. (CA3493)*

Applications:

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3493A and CA3493 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3493A and CA3493 amplifiers are internally phase compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin compatible with the industrial types such as 725, 108A, OP-7, LM11 and LM714 where positive nulling is employed.

Because of their low offset voltage and low offset voltage-versus-temperature coefficient the CA3493A and CA3493 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

The op amps are functionally identical. The CA3493 and CA3493A operate from supply voltage of ±3.5 V to ±18 V and have operating temperature ranges of 0°C to +70°C and -25°C to +85°C, respectively.

These types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN S suffix) and 8-lead dual-in-line plastic (Mini-DIP E suffix) packages.

Circuit Description

The block diagram of the CA3493 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3493 amplifier are shown in Figs. 3 and 4, respectively.

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3493A	CA3493	
DC Supply Voltage	±18	±18	V
Differential-Mode Input Voltage	±5	±5	V
Common-Mode DC Input Voltage	(V+ − 4), V−	(V+ − 4), V−	V
Input Terminal Current	1	1	mA
Device Dissipation			
Without Heat Sink			
Up to 55 °C	630	630	mW
Above 55 °C	Derate Linearly 6.67		mW/°C
Temperature Range	−25 to 85	0 to 70	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	°C

*Short circuit may be applied to ground or to either supply.

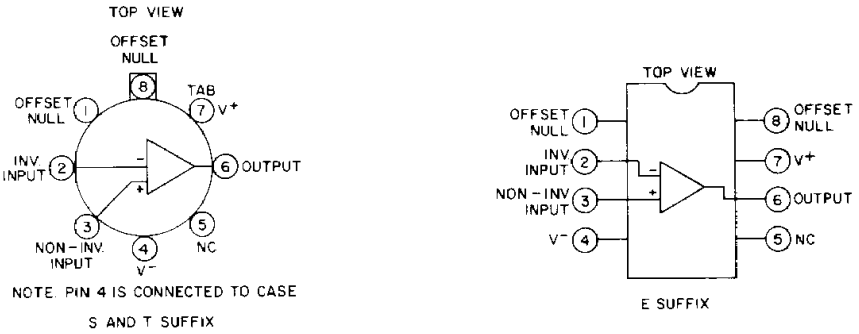


Fig. 1 - Functional diagram of CA3493A and CA3493.

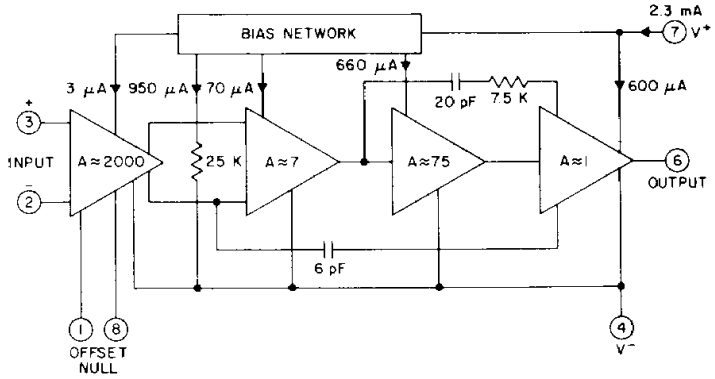


Fig. 2 - Block diagram of CA3493A and CA3493.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

ELECTRICAL CHARACTERISTICS at $T_A = 25\,°C$, $V^+ = 15\ V$ and $V^- = 15\ V$ unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, e_n p-p (0.1 to 10 Hz)	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n							
$f_O = 10$ Hz	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	—	—	24	—	nV/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	24	—	—	24	—	
$f_O = 100$ kHz	—	22	—	—	22	—	
Input Noise Current, i_n p-p (0.1 to 10 Hz)	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n							
$f_O = 10$ Hz	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	—	—	0.75	—	pA/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	0.72	—	—	0.72	—	
$f_O = 100$ kHz	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	110	115	—	100	110	—	dB
		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$	100	130	—	100	130	—	dB
		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)							
$R_L \geq 1$ KΩ	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ $f = 1$ kHz	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} = 20$ mV p-p, $f = 1$ kHz	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−25	—	85	0	—	70	°C

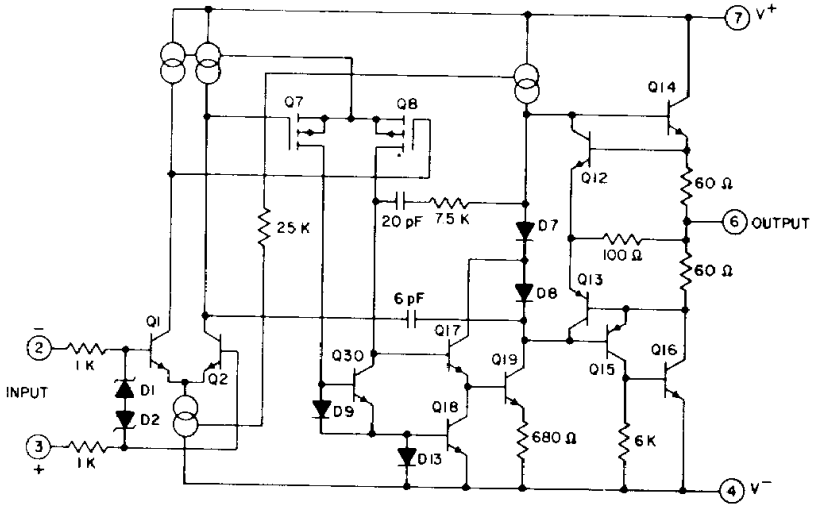


Fig. 3 - CA3493 simplified schematic diagram.

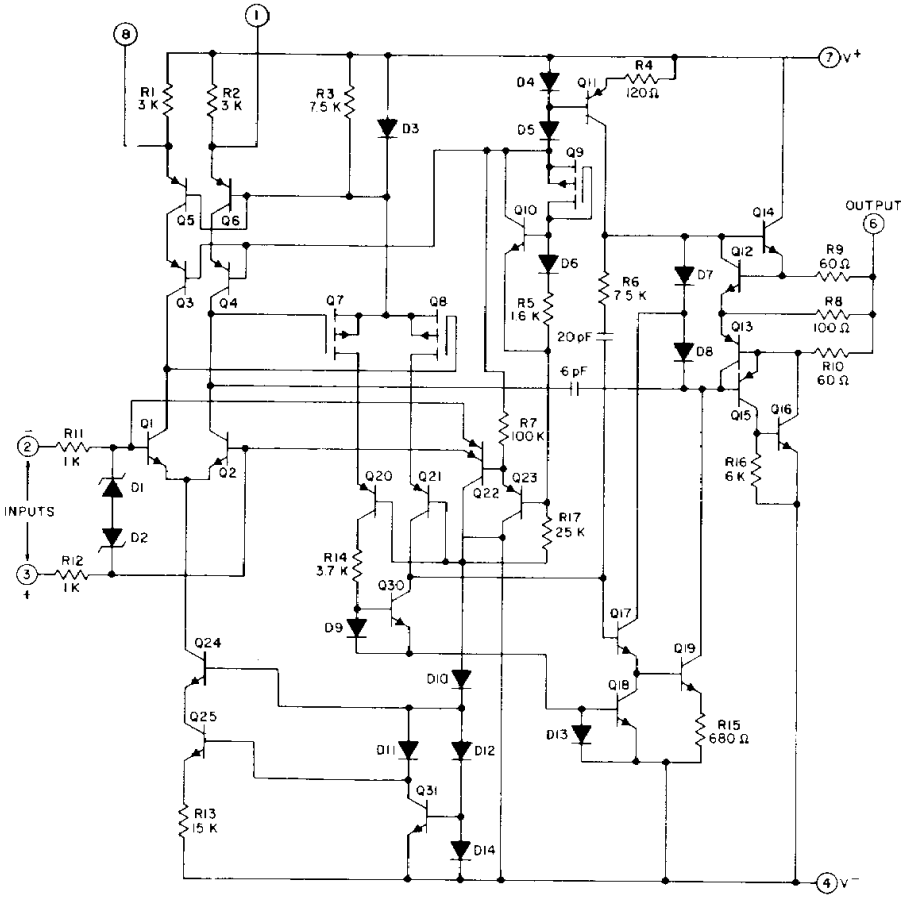


Fig. 4 - Schematic diagram of CA3493A and CA3493.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3493 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

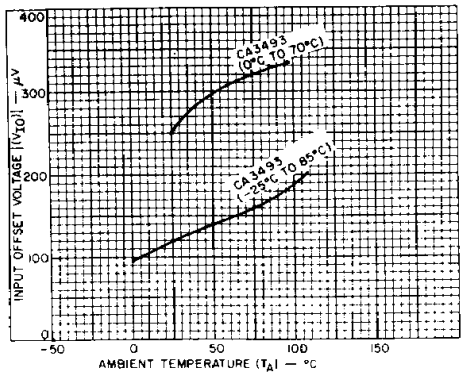


Fig. 5 - Typical input offset-voltage temperature characteristic for CA3493A and CA3493.

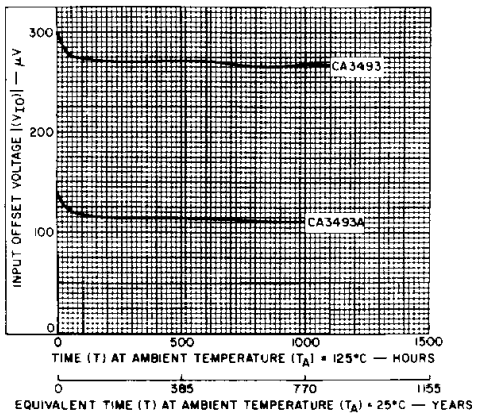


Fig. 6 — Input offset voltage vs. time.

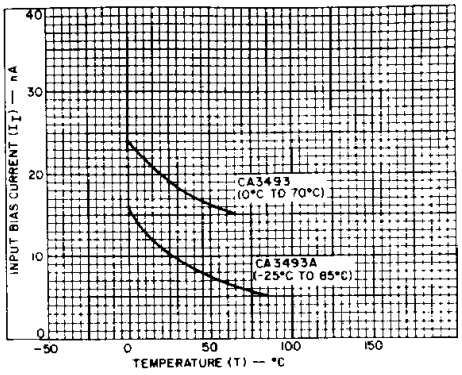


Fig. 7 — Typical input bias current vs. temperature

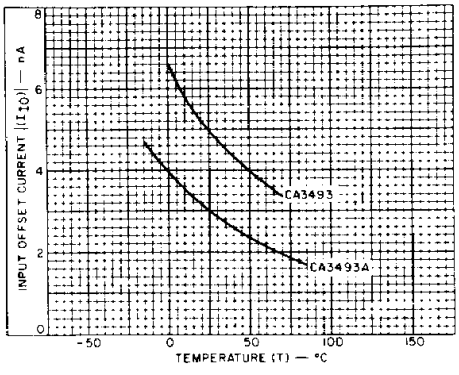


Fig. 8 — Typical input offset current vs. temperature.

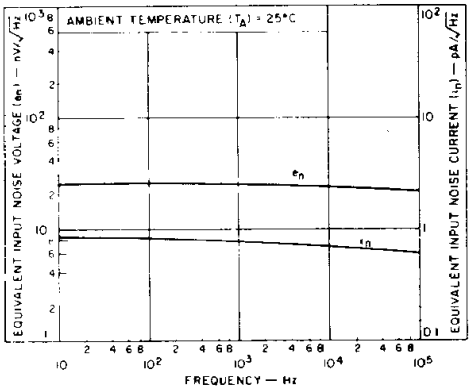


Fig. 9 — Input noise voltage and current density vs. frequency.

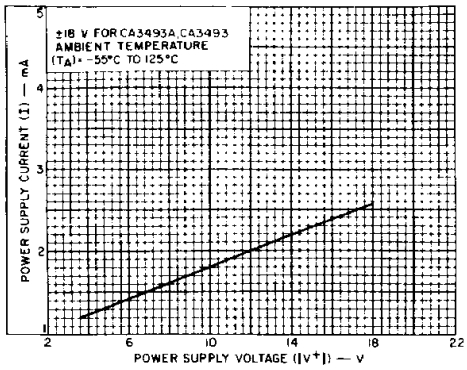


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

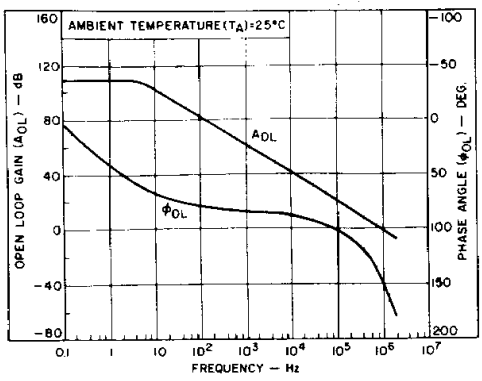


Fig. 11 - Open-loop gain and phase-shift response for CA3493.

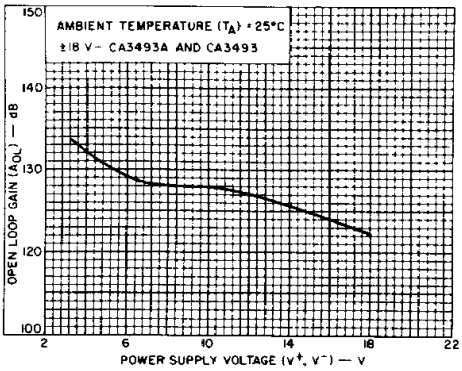


Fig. 12 — Open-loop gain vs. power-supply voltage.

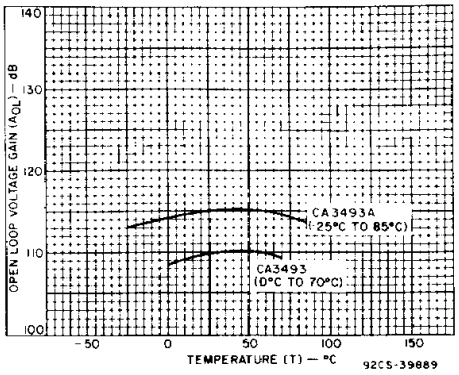


Fig. 13 - Open-loop gain vs. temperature for CA3493A and CA3493.

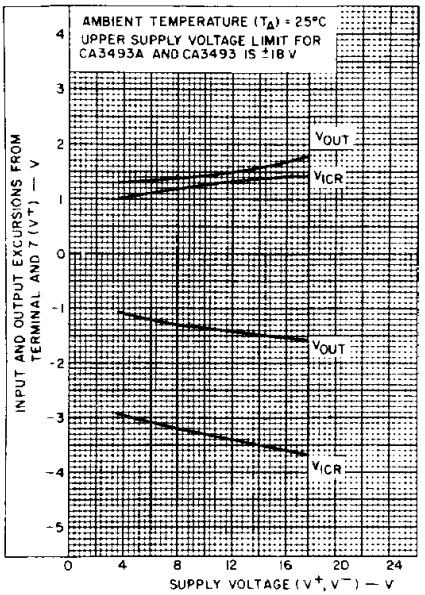


Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

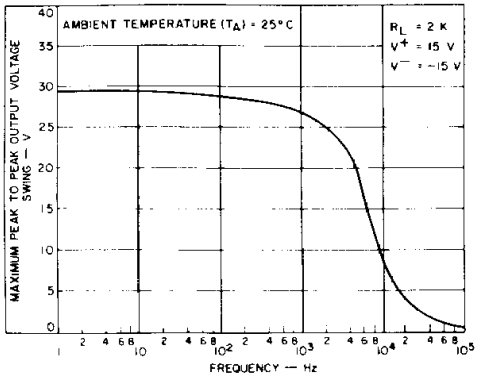


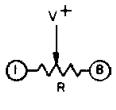
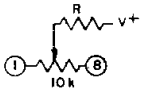
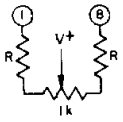
Fig. 14 — Maximum undistorted output voltage vs. frequency.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 8, with its wiper returned to V^+, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3493 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V^- supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3493A CA3493	10K 10K	50K 20K	10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

Test Circuits

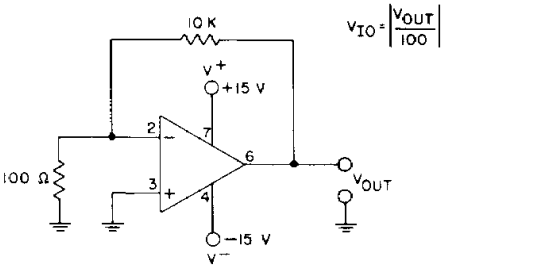
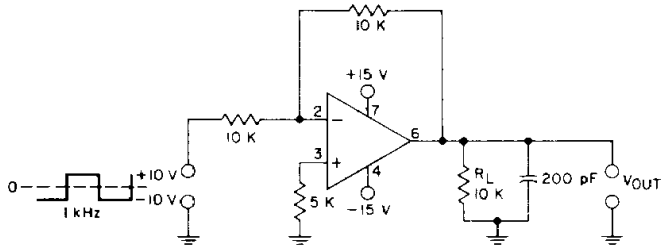
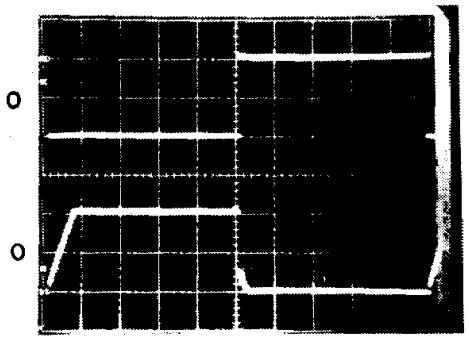


Fig. 16 - Input offset voltage test circuit.



a



TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

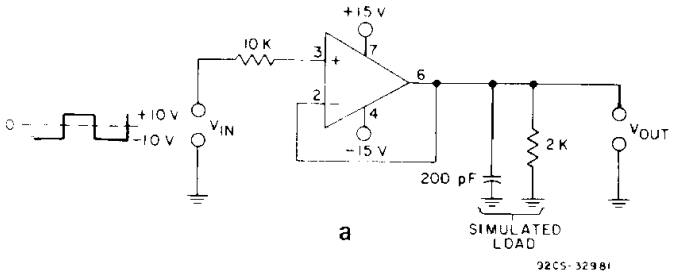
VERT. : $\frac{10V}{DIV}$

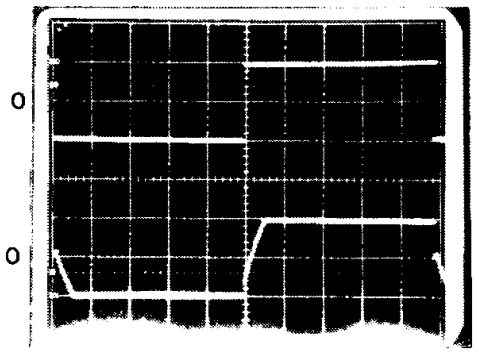
HOR. : $\frac{.1\ ms}{DIV}$

$V^+ = 15V$
$V^- = -15V$
$R_L = 10K$

b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\,V}{DIV}$

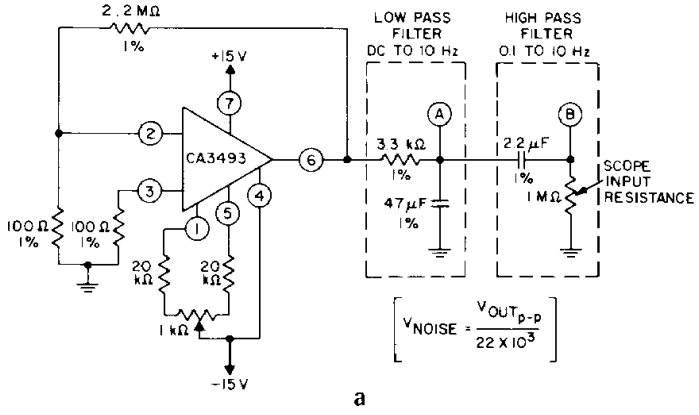
HOR : $\frac{.1\,ms}{DIV}$

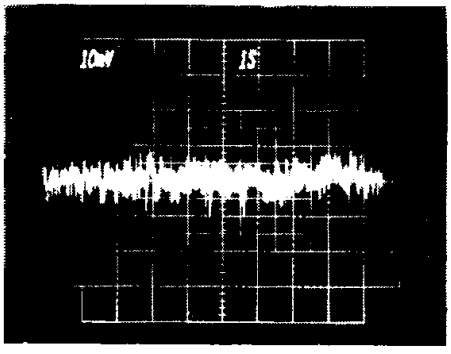
$V^+ = 15\,V$

$V^- = 15\,V$

$R_L = 2K$

Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.





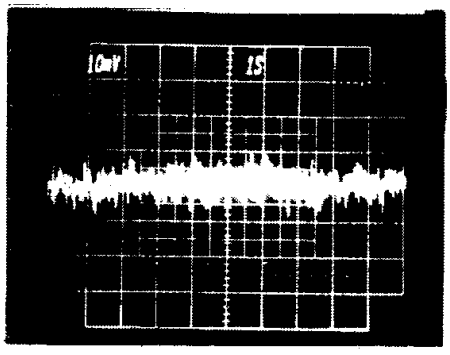
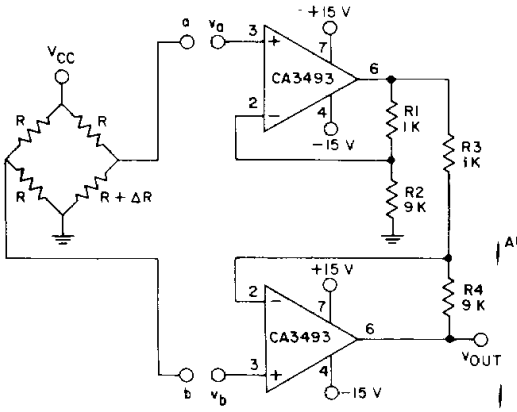


Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

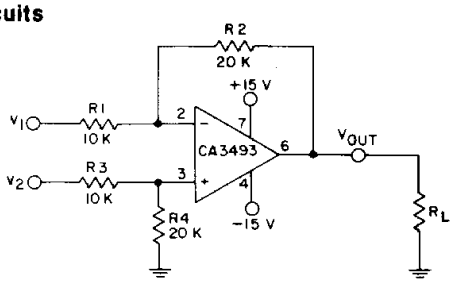
FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(10)$

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

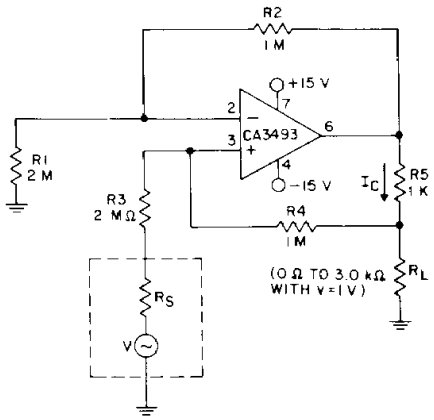
THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

Fig. 21 - Differential amplifier (simple subtractor) using CA3493.



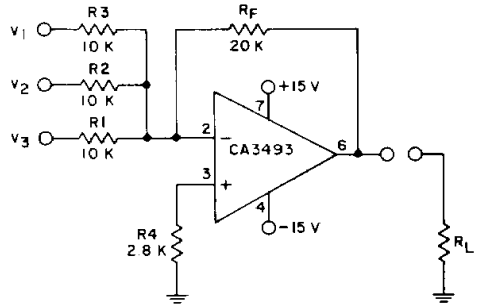
ALL RESISTORS ARE 1%

IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH V = 1 V

$$I_L = \frac{V}{R3}\frac{R4}{R5} = \frac{V}{(2\,M)(1K)} = \frac{V}{2\,K} = 500\ \mu A$$

Fig. 22 - Using CA3493 as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R2}V_2 + \frac{R_F}{R3}V_3\right)$$

$$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$$

ALL RESISTANCE VALUES ARE IN OHMS

Fig. 23 - Typical summing amplifier application.

The CA3493 is an excellent choice for use with thermocouples. In Fig. 24, the CA3493 amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

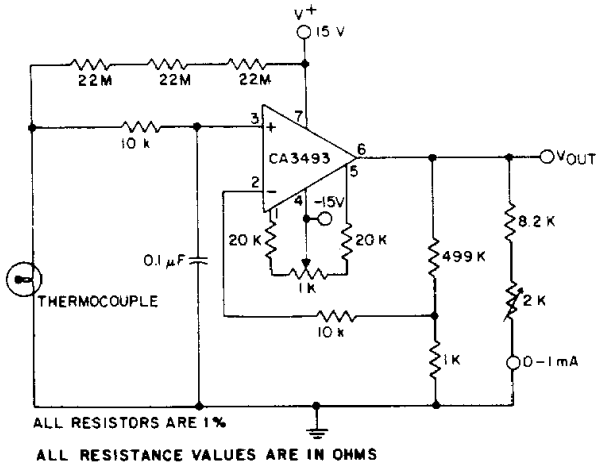


Fig. 24 - The CA3493 used in a thermocouple circuit.