CA3306, CA3306A, CA3306C

6-Bit, 15 MSPS, Flash A/D Converters

August 1997

Features

- CMOS Low Power with Video Speed (Typ) 70mW
- Parallel Conversion Technique
- Signal Power Supply Voltage . . . . . 3V to 7.5V
- 15MHz Sampling Rate with Single 5V Supply
- 6-Bit Latched Three-State Output with Overflow Bit
- Pin-for-Pin Retrofit for the CA3300

Applications

- TV Video Digitizing
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- High Speed Oscilloscope Storage/Display
- General Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision

Description

The CA3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low power consumption and high speed digitization. Digitizing at 15MHz, for example, requires only about 50mW.

The CA3306 family operates over a wide, full scale signal input voltage range of 1V up to the supply voltage. Power consumption is as low as 15mW, depending upon the clock frequency selected. The CA3306 types may be directly retrofitted into CA3300 sockets, offering improved linearity at a lower reference voltage and high operating speed with a 5V supply.

The intrinsic high conversion rate makes the CA3306 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3306s in series to increase the resolution of the conversion system. A series connection of two CA3306s may be used to produce a 7-bit high speed converter. Operation of two CA3306s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

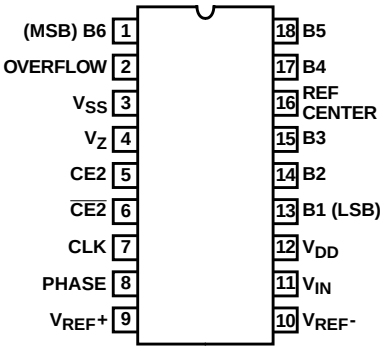
Sixty-four paralleled auto balanced comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

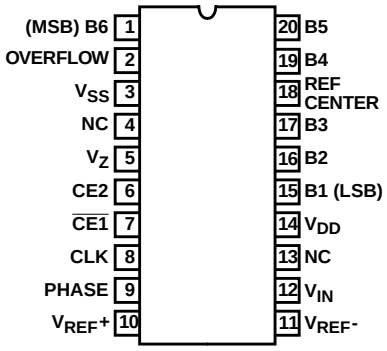
PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3306E	±0.5 LSB	15MHz (67ns)	-40 to 85	18 Ld PDIP	E18.3
CA3306CE	±0.5 LSB	10MHz (100ns)	-40 to 85	18 Ld PDIP	E18.3
CA3306M	±0.5 LSB	15MHz (67ns)	-40 to 85	20 Ld SOIC	M20.3
CA3306CM	±0.5 LSB	10MHz (100ns)	-40 to 85	20 Ld SOIC	M20.3
CA3306D	±0.5 LSB	15MHz (67ns)	-55 to 125	18 Ld SBDIP	D18.3
CA3306CD	±0.5 LSB	10MHz (100ns)	-55 to 125	18 Ld SBDIP	D18.3
CA3306J3	±0.5 LSB	15MHz (67ns)	-55 to 125	20 Ld CLCC	J20.B
CA3306J3	±0.5 LSB	10MHz (100ns)	-55 to 125	20 Ld CLCC	J20.B

Pinouts

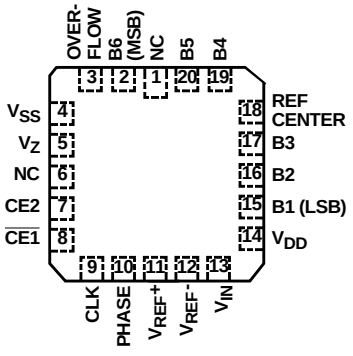
CA3306 (PDIP, SBDIP)
TOP VIEW



CA3306 (SOIC)
TOP VIEW



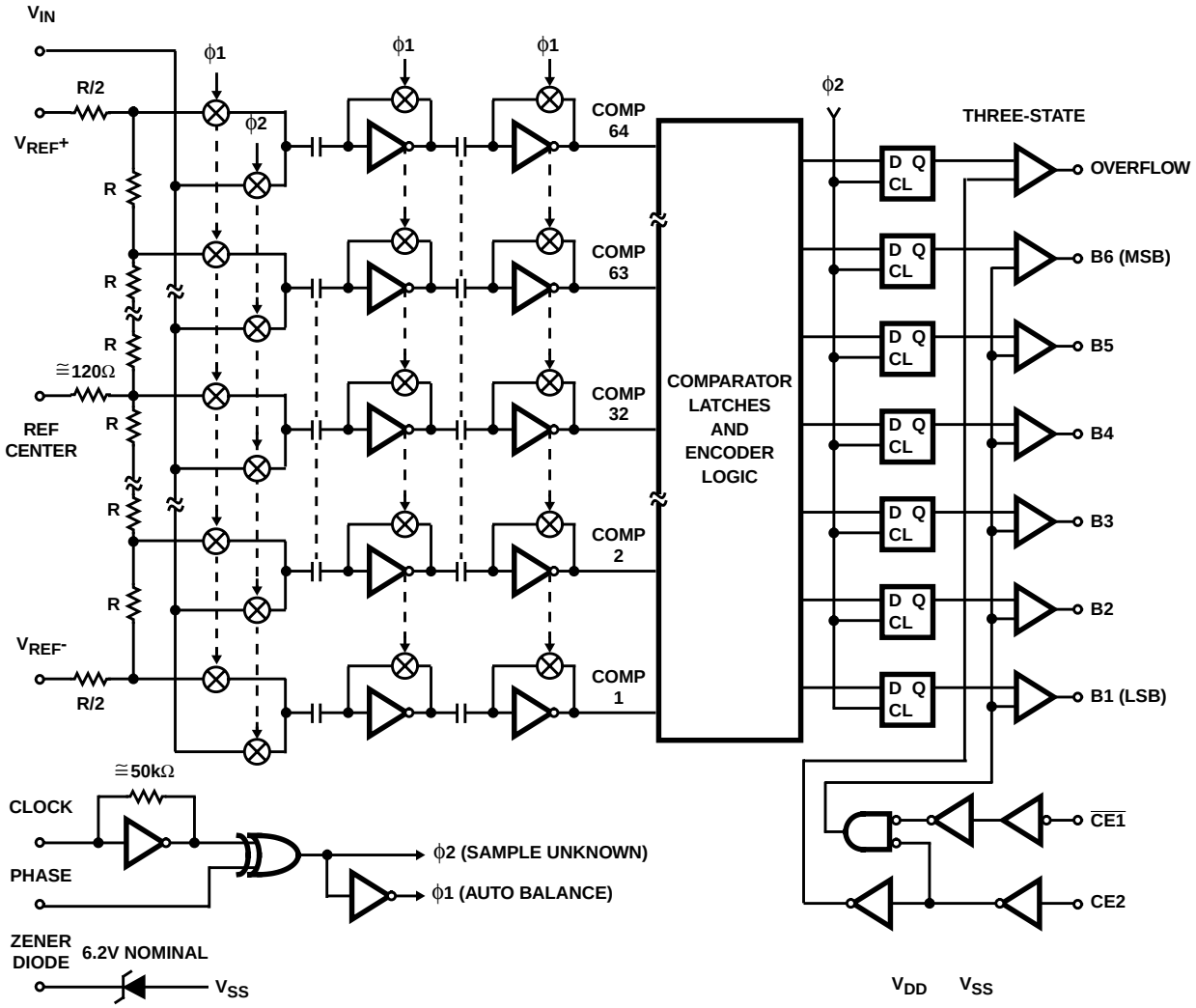
CA3306 (CLCC)
TOP VIEW



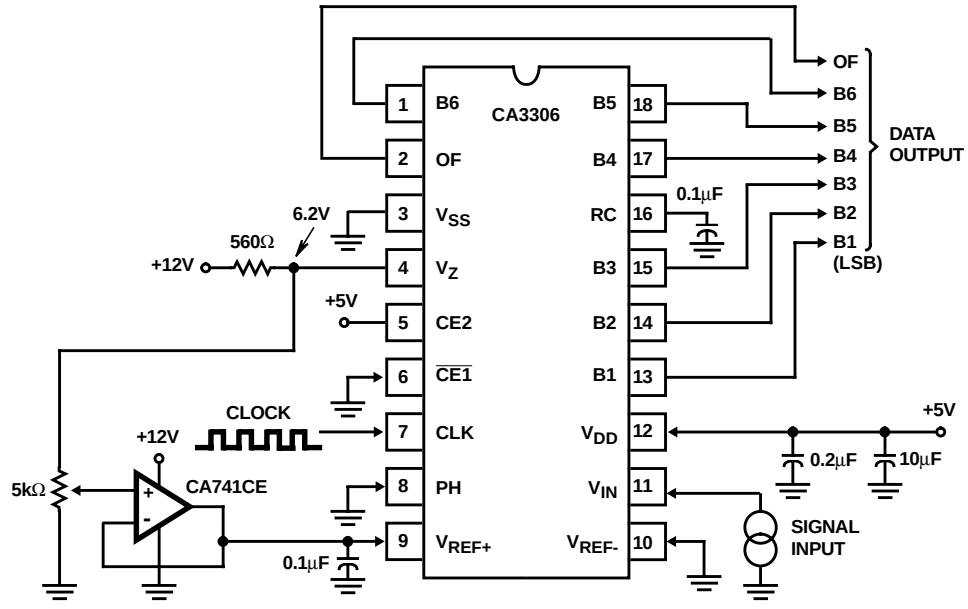
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3102.1**

Functional Block Diagram



Typical Application Circuit



Absolute Maximum Ratings

DC Supply Voltage Range, V_{DD}
Voltage Referenced to V_{SS} Terminal . . . . . -0.5V to +8.5V
Input Voltage Range
All Inputs Except Zener. . . . . -0.5V to V_{DD} + 0.5V
DC Input Current
CLK, PH, $\overline{CE1}$, CE2, V_{IN} . . . . . ±20mA

Operating Conditions

Supply Voltage Range . . . . . .3V to 8V
Temperature Range (T_A)
Ceramic Package (D Suffix) . . . . . -55^oC to 125^oC
Plastic Package (E or M Suffix). . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	75	24
PDIP Package	95	N/A
SOIC Package	115	N/A
CLCC Package	80	28

Maximum Junction Temperature
Hermetic Packages . . . . . 175^oC
Plastic Packages . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25^oC$, V_{DD} = 5V, $V_{REF}+$ = 4.8V, $V_{SS} = V_{REF}-$ = GND, Clock = 15MHz Square Wave for CA3306 or CA3306A, 10MHz for CA3306C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE						
Resolution			6	-	-	Bits
Integral Linearity Error, INL	CA3306, CA3306C		-	±0.25	±0.5	LSB
	CA3306A		-	±0.2	±0.25	LSB
Differential Linearity Error, DNL	CA3306, CA3306C		-	±0.25	±0.5	LSB
	CA3306A		-	±0.2	±0.25	LSB
Offset Error (Unadjusted)	CA3306, CA3306C	(Note 1)	-	±0.5	±1	LSB
	CA3306A		-	±0.25	±0.5	LSB
Gain Error (Unadjusted)	CA3306, CA3306C	(Note 2)	-	±0.5	±1	LSB
	CA3306A		-	±0.25	±0.5	LSB
Gain Temperature Coefficient			-	+0.1	-	$mV/^oC$
Offset Temperature Coefficient			-	-0.1	-	$mV/^oC$
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB Below Full Scale)						
Maximum Conversion Speed	CA3306C		10	13	-	MSPS
	CA3306, CA3306A		15	20	-	MSPS
Maximum Conversion Speed	CA3306C	(Note 4) $\phi1, \phi2 \geq$ Minimum	12	-	-	MSPS
	CA3306, CA3306A		18	-	-	MSPS
Allowable Input Bandwidth		(Note 4)	DC	-	$f_{CLOCK/2}$	MHz
-3dB Input Bandwidth			-	30	-	MHz
Signal to Noise Ratio, SNR $= \frac{RMS Signal}{RMS Noise}$		f_S = 15MHz, f_{IN} = 100kHz	-	34.6	-	dB
		f_S = 15MHz, f_{IN} = 5MHz	-	33.4	-	dB
Signal to Noise Ratio, SINAD $= \frac{RMS Signal}{RMS Noise+Distortion}$		f_S = 15MHz, f_{IN} = 100kHz	-	34.2	-	dB
		f_S = 15MHz, f_{IN} = 5MHz	-	29.0	-	dB
Total Harmonic Distortion, THD		f_S = 15MHz, f_{IN} = 100kHz	-	-46.0	-	dBc
		f_S = 15MHz, f_{IN} = 5MHz	-	-30.0	-	dBc
Effective Number of Bits, ENOB		f_S = 15MHz, f_{IN} = 100kHz	-	5.5	-	Bits
		f_S = 15MHz, f_{IN} = 5MHz	-	4.5	-	Bits

Electrical Specifications $T_A = 25^oC$, $V_{DD} = 5V$, $V_{REF}+ = 4.8V$, $V_{SS} = V_{REF}- = GND$, Clock = 15MHz Square Wave for CA3306 or CA3306A, 10MHz for CA3306C **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Positive Full Scale Input Range		(Notes 3, 4)	1	4.8	$V_{DD}+0.5$	V
Negative Full Scale Input Range		(Notes 3, 4)	-0.5	0	V_{DD} - 1	V
Input Capacitance			-	15	-	pF
Input Current		$V_{IN} = 4.92V$, $V_{DD} = 5V$	-	-	±500	µA
INTERNAL VOLTAGE REFERENCE						
Zener Voltage		$I_Z = 10mA$	5.4	6.2	7.4	V
Zener Dynamic Impedance		$I_Z = 10mA$, 20mA	-	12	25	Ω
Zener Temperature Coefficient			-	-0.5	-	$mV/^oC$
REFERENCE INPUTS						
Resistor Ladder Impedance			650	1100	1550	Ω
DIGITAL INPUTS						
Maximum V_{IN}, Logic 0		All Digital Inputs (Note 4)	-	-	$0.3 \times V_{DD}$	V
Maximum V_{IN}, Logic 1		All Digital Inputs (Note 4)	$0.7 \times V_{DD}$	-	-	V
Digital Input Current		Except CLK, $V_{IN} = 0V$, 5V	-	±1	±5	µA
Digital Input Current		CLK Only	-	±100	±200	µA
DIGITAL OUTPUTS						
Digital Output Three-State Leakage		$V_{OUT} = 0V$, 5V	-	±1	±5	µA
Digital Output Source Current		$V_{OUT} = 4.6V$	-1.6	-	-	mA
Digital Output Sink Current		$V_{OUT} = 0.4V$	3.2	-	-	mA
TIMING CHARACTERISTICS						
Auto Balance Time (ϕ1)	CA3306C		50	-	∞	ns
	CA3306, CA3306A		33	-	∞	
Sample Time (ϕ2)	CA3306C	(Note 4)	33	-	5000	ns
	CA3306, CA3306A		22	-	5000	ns
Aperture Delay			-	8	-	ns
Aperture Jitter			-	100	-	ps_{P-P}
Output Data Valid Delay, t_D	CA3306C		-	35	50	ns
	CA3306, CA3306A		-	30	40	ns
Output Data Hold Time, t_H		(Note 4)	15	25	-	ns
Output Enable Time, t_{EN}			-	20	-	ns
Output Disable Time, t_{DIS}			-	15	-	ns
POWER SUPPLY CHARACTERISTICS						
I_{DD} Current, Refer to Figure 4	CA3306C	Continuous Conversion (Note 4)	-	11	20	mA
	CA3306, CA3306A		-	14	25	mA
I_{DD} Current		Continuous ϕ1	-	7.5	15	mA

NOTES:

1. OFFSET ERROR is the difference between the input voltage that causes the 00 to 01 output code transition and $(V_{REF}+ - V_{REF}-)/128$.
2. GAIN ERROR is the difference the input voltage that causes the $3F_{16}$ to overflow output code transition and $(V_{REF}+ - V_{REF}-) \times 127/128$.
3. The total input voltage range, set by $V_{REF}+$ and $V_{REF}-$, may be in the range of 1 to $(V_{DD} + 1)$ V.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

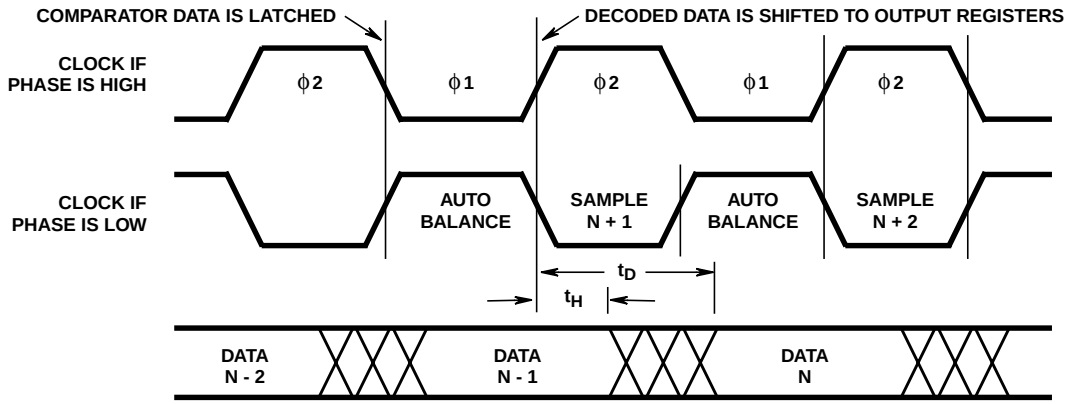


FIGURE 1. INPUT-TO-OUTPUT

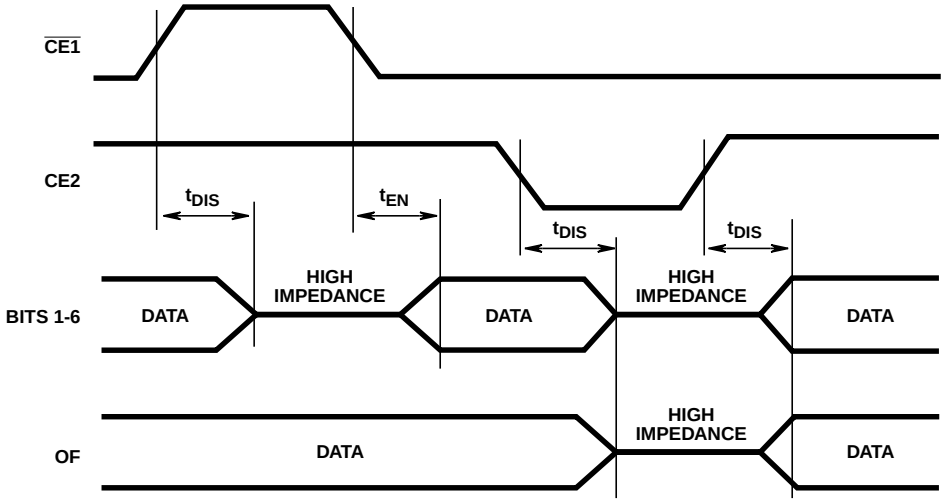


FIGURE 2. OUTPUT ENABLE

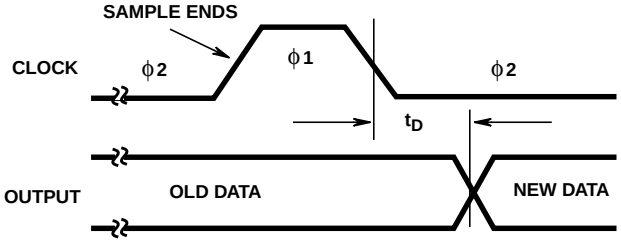


FIGURE 3A.

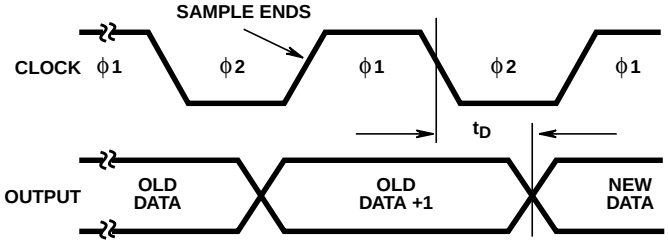


FIGURE 3B.

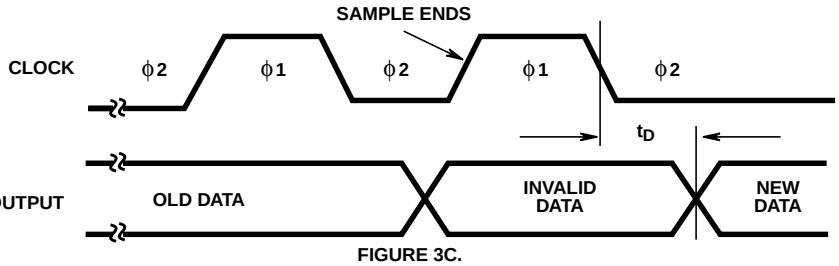


FIGURE 3C.

FIGURE 3. PULSE MODE

Typical Performance Curves

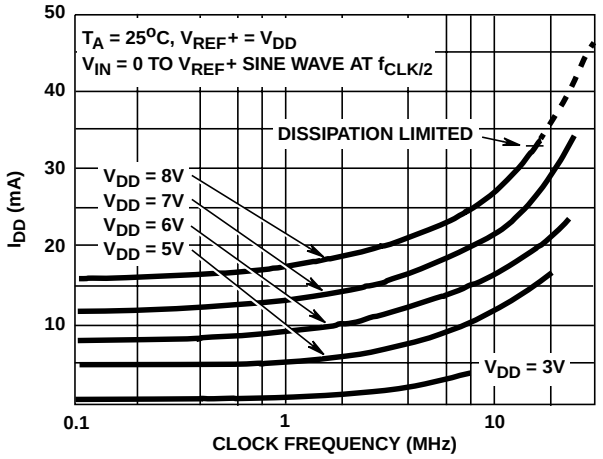


FIGURE 4. TYPICAL I_{DD} AS A FUNCTION OF V_{DD}

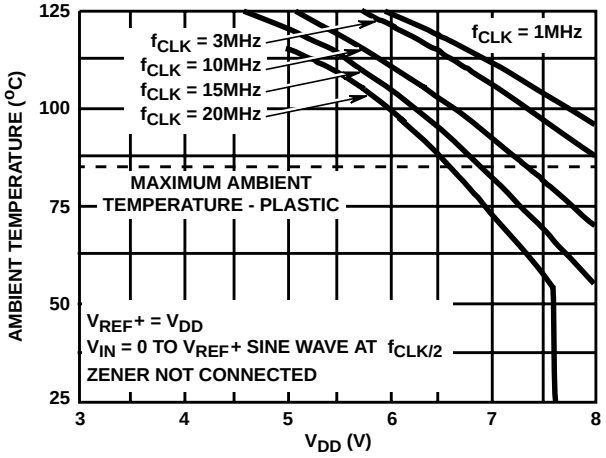


FIGURE 5. TYPICAL MAXIMUM AMBIENT TEMPERATURE AS A FUNCTION OF SUPPLY VOLTAGE

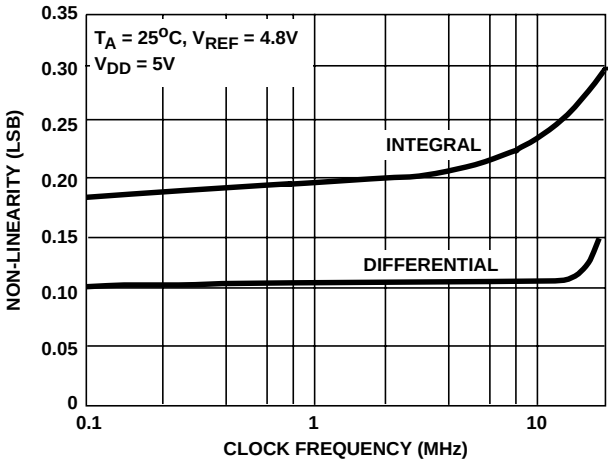


FIGURE 6. TYPICAL NON-LINEARITY AS A FUNCTION OF CLOCK SPEED

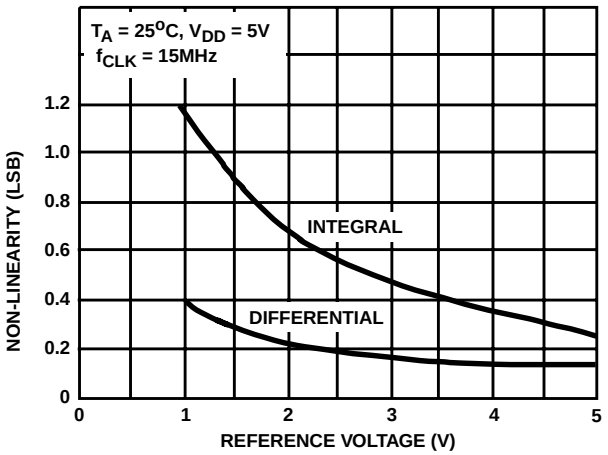


FIGURE 7. TYPICAL NON-LINEARITY AS A FUNCTION OF REFERENCE VOLTAGE

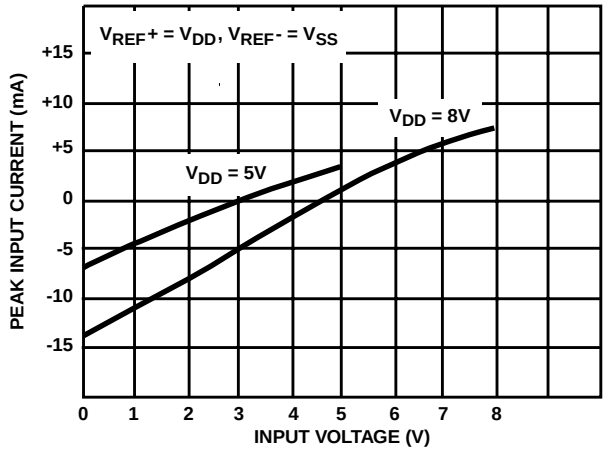


FIGURE 8. TYPICAL PEAK INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

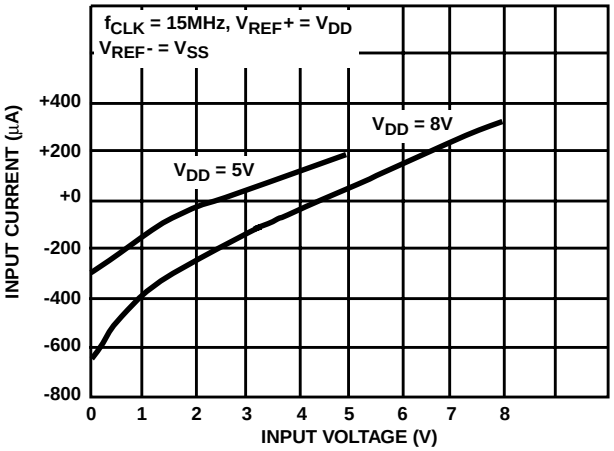


FIGURE 9. TYPICAL AVERAGE INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Typical Performance Curves (Continued)

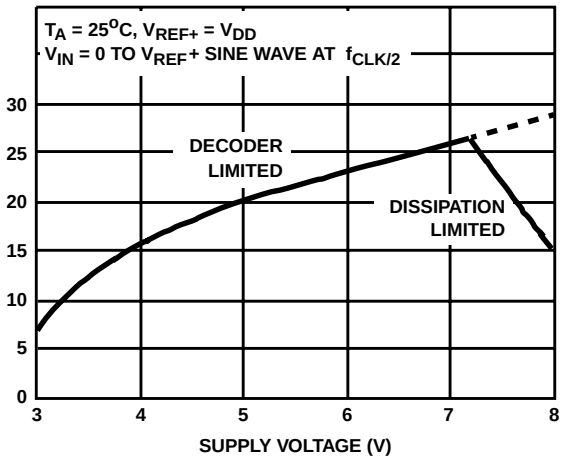


FIGURE 10. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

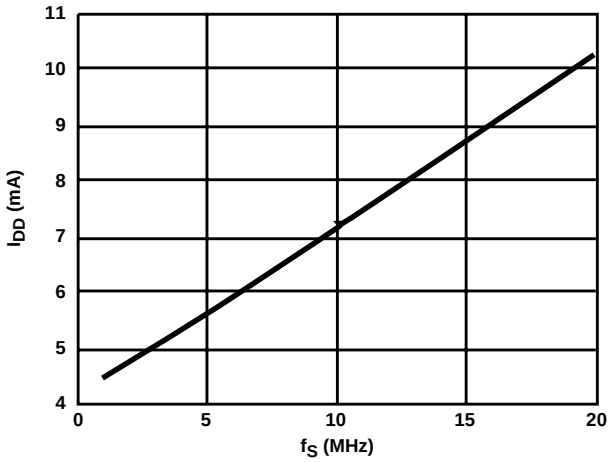


FIGURE 11. DEVICE CURRENT vs SAMPLE FREQUENCY

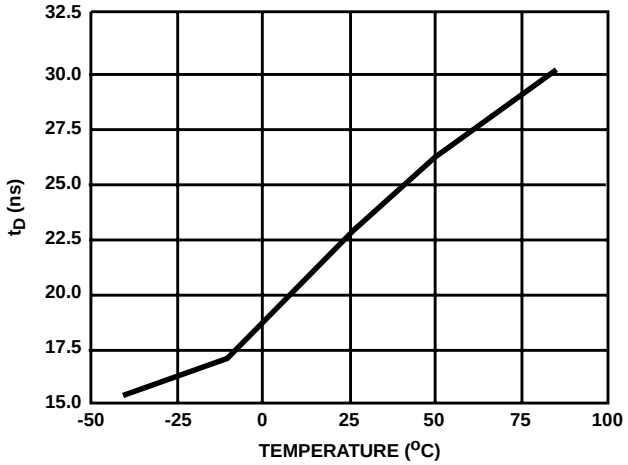


FIGURE 12. DATA DELAY vs TEMPERATURE

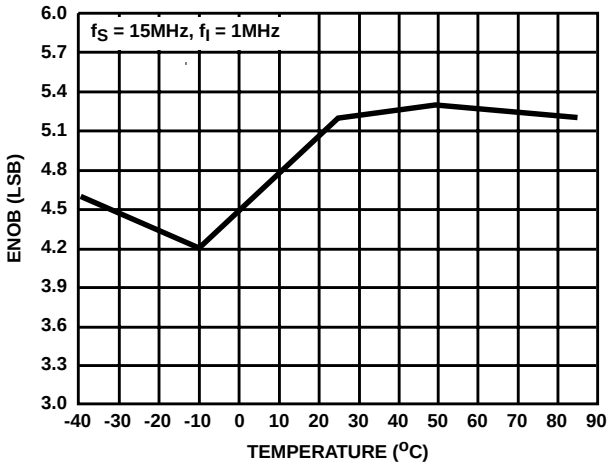


FIGURE 13. ENOB vs TEMPERATURE

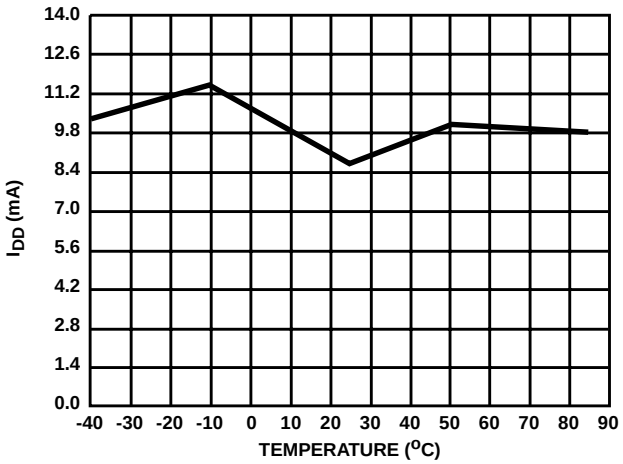


FIGURE 14. I_{DD} vs TEMPERATURE

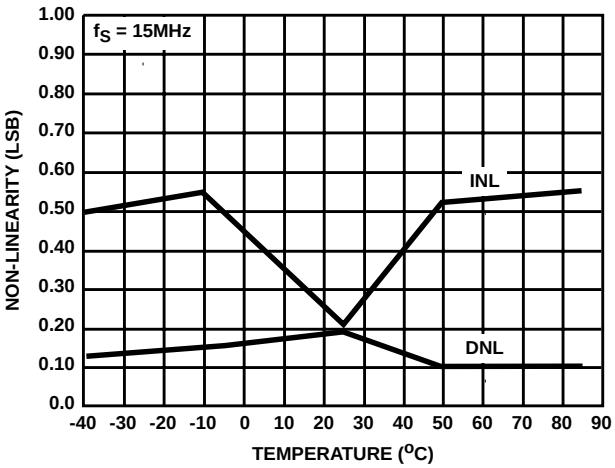


FIGURE 15. NON-LINEARITY vs TEMPERATURE

Typical Performance Curves (Continued)

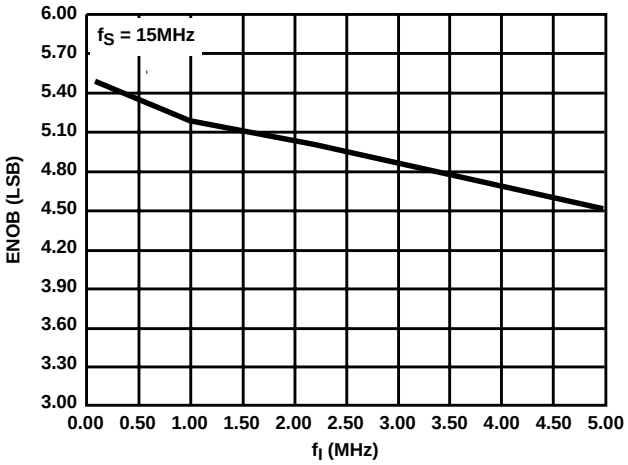


FIGURE 16. ENOB vs INPUT FREQUENCY

Pin Descriptions

PIN NUMBER		NAME	DESCRIPTION
DIP	SOIC		
1	1	B6	Bit 6, Output (MSB).
2	2	OF	Overflow, Output.
3	3, 4	V_{SS}	Digital Ground.
4	5	VZ	Zener Reference Output.
5	6	CE2	Three-State Output Enable Input, Active Low. See Table 1.
6	7	$\overline{CE1}$	Three-State Output Enable Input, Active High. See Table 1.
7	8	CLK	Clock Input.
8	9	Phase	Sample clock phase control input. When PHASE is low, “Sample Unknown” occurs when the clock is low and “Auto Balance” occurs when the clock is high (see text).
9	10	$V_{REF}+$	Reference Voltage Positive Input.
10	11	$V_{REF}-$	Reference Voltage Negative Input.
11	12	V_{IN}	Analog Signal Input.
12	13, 14	V_{DD}	Power Supply, +5V.
13	15	B1	Bit 1, Output (LSB).
14	16	B2	Bit 2, Output.
15	17	B3	Bit 3, Output.
16	18	REF(CTR)	Reference Ladder Midpoint.
17	19	B4	Bit 4, Output.
18	20	B5	Bit 5, Output.

TABLE 1. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B6	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't care

TABLE 2. OUTPUT CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 4.80 (V)	V_{REF} 3.20 (V)	BINARY OUTPUT CODE (LSB) OF	B6	B5	B4	B3	B2	B1	DECIMAL COUNT
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.10	0.08	0.075	0.05	0	0	0	0	0	0	1	1
2 LSB	0.20	0.16	0.15	0.10	0	0	0	0	0	1	0	2
•		•						•				•
•		•						•				•
•		•						•				•
•		•						•				•
$^1/_2$ Full Scale - 1 LSB	3.10	2.48	2.325	1.55	0	0	1	1	1	1	1	31
$^1/_2$ Full Scale	3.20	2.56	2.40	1.60	0	1	0	0	0	0	0	32
$^1/_2$ Full Scale + 1 LSB	3.30	2.64	2.475	1.65	0	1	0	0	0	0	1	33
•		•						•				•
•		•						•				•
•		•						•				•
•		•						•				•
Full Scale - 1 LSB	6.20	4.96	4.65	3.10	0	1	1	1	1	1	0	62
Full Scale	6.30	5.04	4.725	3.15	0	1	1	1	1	1	1	63
Overflow	6.40	5.12	4.80	3.20	1	1	1	1	1	1	1	127

NOTE:

1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Device Operation

A sequential parallel technique is used by the CA3306 converter to obtain its high speed operation. The sequence consists of the “Auto Balance” phase ϕ1 and the “Sample Unknown” phase ϕ2. (Refer to the circuit diagram.) Each conversion takes one clock cycle (see Note). With the phase control low, the “Auto Balance” (ϕ1) occurs during the High period of the clock cycle, and the “Sample Unknown” (ϕ2) occurs during the low period of the clock cycle.

During the “Auto Balance” phase, a transmission-gate switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/126],$$

Where: V_{TAP} (N) = reference ladder tap voltage at point N,
V_{REF} = voltage across V_{REF}- to V_{REF}+,
N = tap number (I through 64).

NOTE: This device requires only a single-phase clock The terminology of ϕ1 and ϕ2 refers to the High and Low periods of the same clock.

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the “Sample Unknown” phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a “low” state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a “high” state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase (ϕ2), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-bit 7-bit decode array and the results are clocked into a storage register at the rising edge of the next ϕ2.

A three-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable 81 through 86 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state (Table 1).

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3306 via the following steps. (Refer to timing diagram, Figure 1.) With the phase control in a “High” state, the rising edge of the clock input will start a “sample” phase. During this entire “High” state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, after the specified aperture delay, all 64 comparator outputs are captured by the 64 latches. This ends the “sample” phase and starts the “auto balance” phase for the comparators. During this “Low” state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay to as valid data at the output of the three-state drivers. This also marks the start of a new “sample” phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, ϕ2, during the standby state. The device can now be pulsed through the Auto Balance phase with a single pulse. The analog value is captured on the leading edge of ϕ1 and is transferred into the output registers on the trailing edge of ϕ1. We are now back in the standby state, ϕ2, and another conversion can be started, but not later than 5μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between ϕ2 and ϕ1, the lower the power consumption. (See Timing Waveform, Figure 3.)

The second method uses the Auto Balance phase, ϕ1, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two ϕ2 pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second ϕ2 pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes slightly longer, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of ϕ2 to ϕ1. (See Timing Waveform, Figure 3B.)

For applications requiring both indefinite standby and lowest power, standby can be in the ϕ2 (Sample Unknown) state with two ϕ1 pulses to generate valid data (see Figure 3C). Valid data now appears two full clock cycles after starting the conversion process.

Analog Input Considerations

The CA3306 input terminal is characterized by a small capacitance (see Specifications) and a small voltage-dependent current (See Typical Performance Curves). The signal-source impedance should be kept low, however, when operating the CA3306 at high clock rates.

The CA3306 outputs a short (less than 10ns) current spike of up to several mA amplitude (See Typical Performance Curves) at the beginning of the sample phase. (To a lesser extent, a spike also appears at the beginning of auto balance.) The driving source must recover from the spike by the end of the same phase, or a loss of accuracy will result.

A locally terminated 50Ω or 75Ω source is generally sufficient to drive the CA3306. If gain is required, a high speed, fast settling operational amplifier, such as the HA-5033, HA-2542, or HA5020 is recommended.

Digital Input And Output Interfacing

The two chip-enable and the phase-control inputs are standard CMOS units. They should be driven from less than 0.3 x V_{DD} to at least 0.7 x V_{DD}. This can be done from 74HC series CMOS (QMOS), TTL with pull-up resistors, or, if V_{DD} is greater than the logic supply, open collector or open drain drivers plus pull-ups. (See Figure 20.)

The clock input is more critical to timing variations, such as $\phi 1$ becoming too short, for instance. Pull-up resistors should generally be avoided in favor of active drivers. The clock input may be capacitively coupled, as it has an internal 50kΩ feedback resistor on the first buffer stage, and will seek its own trip point. A clock source of at least $1V_{P-P}$ is adequate, but extremely non-symmetrical waveforms should be avoided.

The output drivers have full rail-to-rail capability. If driving CMOS systems with V_{DD} below the V_{DD} of the CA3306, a CD74HC4050 or CD74HC4049 should be used to step down the voltage. If driving LSTTL systems, no step-down should be necessary, as most LSTTLs will take input swings up to 10V to 15V.

Although the output drivers are capable of handling typical data bus loading, the capacitor charging currents will produce local ground disturbances. For this reason, an external bus driver is recommended.

Increased Accuracy

In most cases the accuracy of the CA3306 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the operational amplifier. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2(V_{REF}/64)$$
$$= V_{REF}/128.$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}- and ground will accomplish the adjustment. Set V_{IN} to $^1/_2$ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF} and a negative voltage of about 2 LSBs. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the operational amplifier. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is $^1/_2$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}(127/128).$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overtlow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC) is available to the user as the midpoint of the resistor ladder. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 31 to 32 occurs at $31^1/_2$ LSBs. That voltage is as follows:

$$V_{IN} \text{ (31 to 32 transition)} = 31.5\ (V_{REF}/64)$$
$$= V_{REF}(63/128).$$

An adjustable voltage follower can be connected to the RC pin or a 2K pot can be connected between V_{REF}+ and V_{REF}- with the wiper connected to RC. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create unique transfer functions. The user must remember, however, that there is approximately 120Ω in series with the RC pin.

Applications

7-Bit Resolution

To obtain 7-bit resolution, two CA3306s can be wired together. Necessary ingredients include an open-ended ladder network, an overtlow indicator, three-state outputs, and chip-enabler controls - all of which are available on the CA3306.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 17. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry.

Doubled Sampling Speed

The phase control and both positive and negative true chip enables allow the parallel connection of two CA3306s to double the sampling speed. Figure 18 shows this configuration. One converter samples on the positive phase of the clock, and the second on the negative. The outputs are also alternately enabled. Care should be taken to provide a near square-wave clock it operating at close to the maximum clock speed for the devices.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-bit to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the CA3306 allows 12-bit conversions in the 500ns to 900ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Figure 19. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than $^1/_2$ LSB.
- An offset bias of 1 LSB (1/64) Is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

The first converter can be offset-biased by adding a 20Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.4V reference is used in the system, for example, then the first CA3306 will require a 6.5V reference.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Operating and Handling Considerations

HANDLING

All inputs and outputs of Intersil CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. “Guide to Better Handling and Operation of CMOS Integrated Circuits.”

OPERATING

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off. The zener (pin 4) is the only terminal allowed to exceed V_{DD}.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Application Circuits

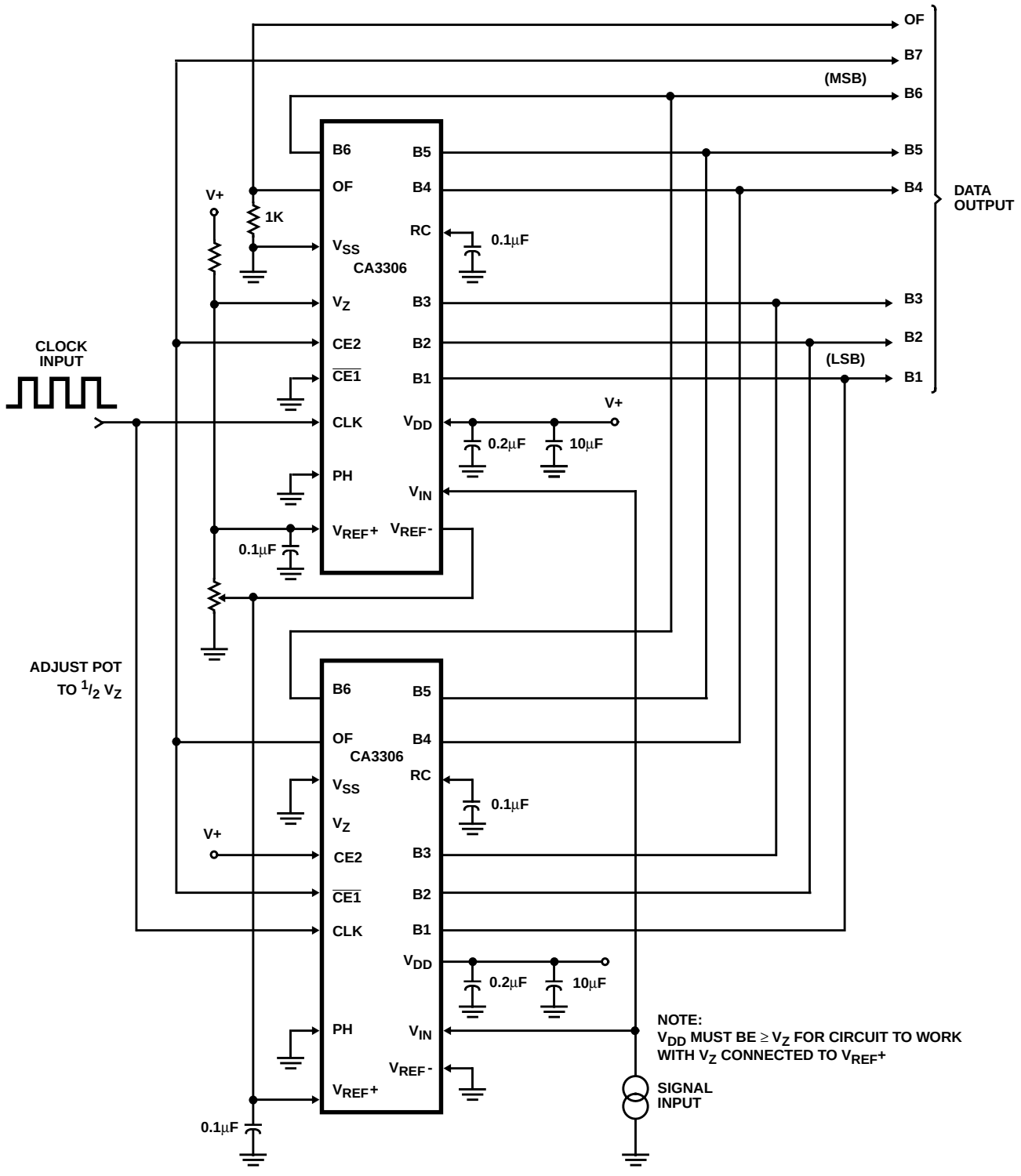


FIGURE 17. TYPICAL CA3306 7-BIT RESOLUTION CONFIGURATION

Application Circuits (Continued)

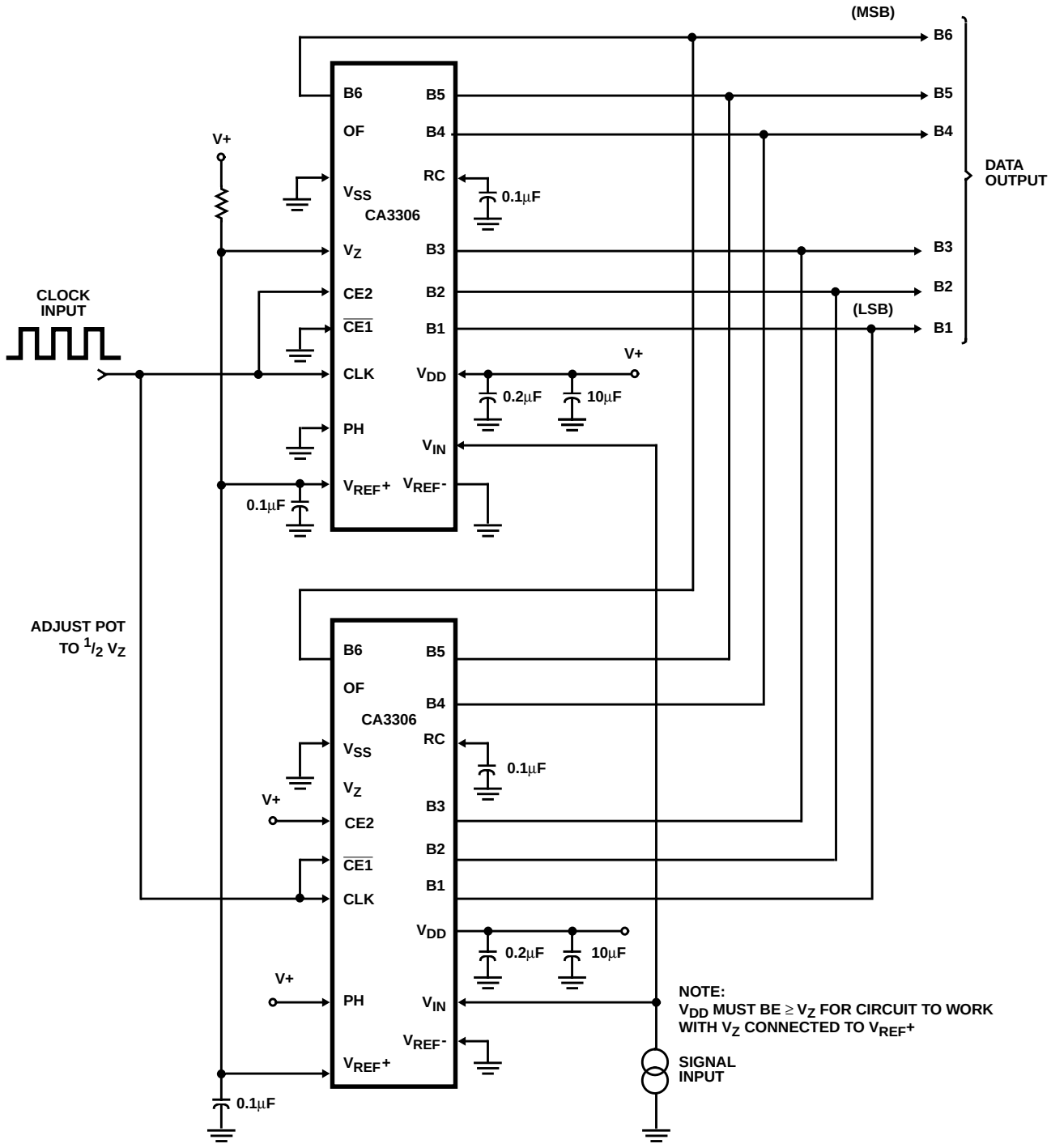


FIGURE 18. TYPICAL CA3306 6-BIT RESOLUTION CONFIGURATION WITH DOUBLE SAMPLING RATE CAPABILITY

Application Circuits (Continued)

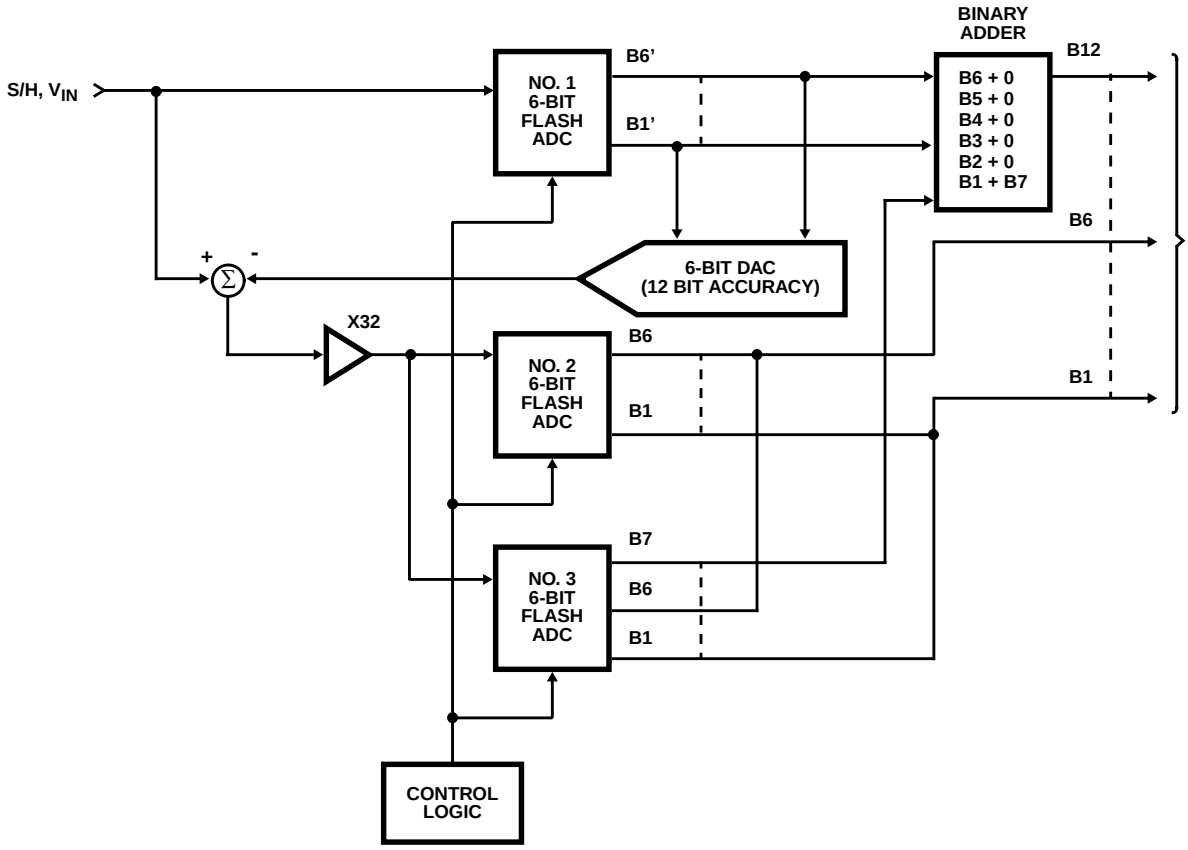


FIGURE 19. TYPICAL CA3306, 800ns, 12-BIT ADC SYSTEM

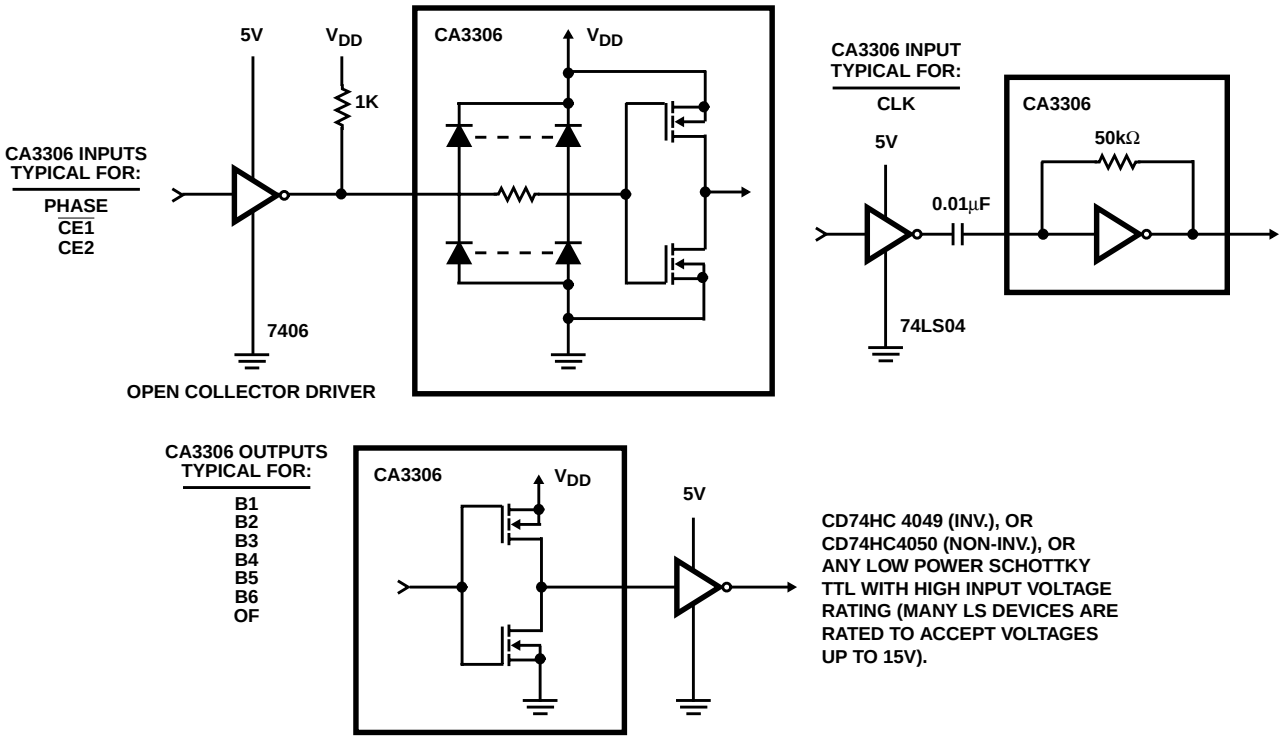


FIGURE 20. 5V LOGIC INTERFACE CIRCUIT FOR V_{DD} > 5.5V

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