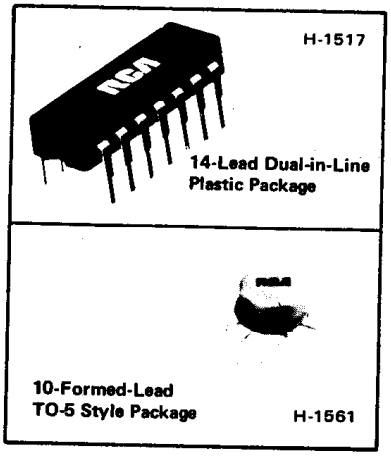
CA3064, CA3064E



TV Automatic Fine Tuning Circuit

Features:

- Cascode type high-gain amplifier (18 mV input for rated output)
- Internal voltage regulator
- Differential detector
- For use with either color or monochrome
- Differential amplifier
- Bipolar outputs
- Wide operating-temperature range; −55 to +125°C

RCA-CA3064 and CA3064E represent the third generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications. They provide all of the signal-processing components needed (with the exception of the tuned-phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The CA3064 is supplied in the 10-formed-lead TO-5 style package, and the CA3064E in the 14-lead dual-in-line plastic package. Both types operate over the temperature range of −55 to +125°C.

The CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1 but embody a higher-gain input amplifier which provides a 20-dB improvement in sensitivity. The increased sensitivity extends the application of a proven AFT system to the low-level if-amplifier stages in TV receivers.

Because the CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1, refer to Application Note ICAN-5831, "Application of the RCA CA3044 and CA3044V1 Integrated Circuits in Automatic Fine-Tuning Systems" for general application information.

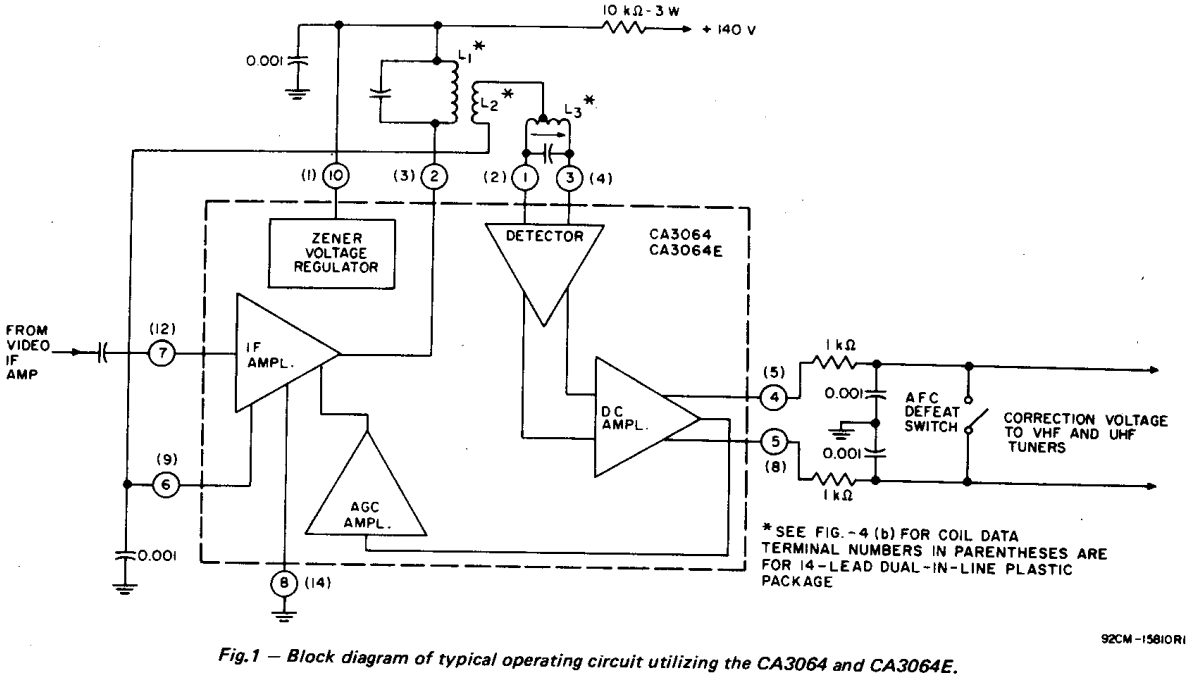


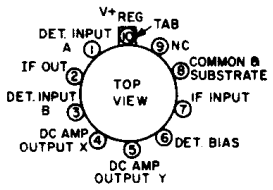
Fig. 1 – Block diagram of typical operating circuit utilizing the CA3064 and CA3064E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

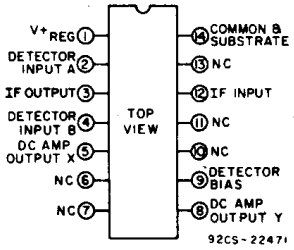
DEVICE DISSIPATION:
- Up to T_A = 25°C . . . . . 700 mW
- Above T_A = 25°C . . . . . derate linearly 5.6 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . . −55 to +125°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max.. . . . . 265°C



(a) CA3064



(b) CA3064E

Fig.2 – Terminal assignment diagrams.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 (3) and horizontal terminal 6 (9) is +20 to 0 volts. Terminal nos. in parentheses are for the 14-lead dual-in-line plastic package.

TERMINAL No.	9(6,7, 10,11, 13)	10 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (8)	6 (9)	7 (12)	8 (14)
9(6,7,♦ 10,11, 13)	← NO INTERNAL CONNECTION →									
10 (1)			+12 0	+10 -10	+12 0	+12 0	+12 0	+10 0	+20 0	▲
1 (2)				*	+10 - 10	*	*	+5 - 5	*	+5 - 6
2 (3)					*	*	*	+20 0	*	+20 0
3 (4)						*	*	+5 - 6	*	+5 - 6
4 (5)							*	*	*	+12 0
5 (8)								*	*	+12 0
6 (9)									+5 - 2	+2 0
7 (12)										+2 - 10
8 (14)										REF.SUBSTRATE & CASE■

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9(6,7, 10,11, 13)	-	-
10 (1)	50	50
1 (2)	1	0.1
2 (3)	20	20
3 (4)	1	0.1
4 (5)	5	5
5 (8)	5	5
6 (9)	5	5
7 (12)	1	1
8 (14)	50	50

▲ Terminal number 10 (1) may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor – provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♦ It is recommended that unused terminals 6,7,10,11, and 13 on the 14-lead dual-in-line-plastic package and terminal 9 on the TO-5 package be grounded to act as shields.

CA3064, CA3064E

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS		LIMITS CA3064, CA3064E MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS									
Device Dissipation	P_D	4	V^+ = 30V, R_S = 1.5kΩ	T_A = −25°C	-	135	150	mW	-
				T_A = +25°C	130	140	150		-
				T_A = +85°C	-	145	150		-
Current Drain at 10.5 Volts	I_T	4	$V_{10(1)}$ = 10.5 V		4	6.5	9.5	mA	-
Zener Regulated Voltage – DC Supply Voltage at terminal 10(1)*	$V_{10(1)}$	4	V^+ = 30 V, R_S = 1.5 kΩ		10.9	11.8	12.8	V	-
Quiescent Operating Current into Terminal 2(3)	$I_{2(3)}$	4			1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4(5)	$V_{4(5)}$	-			5	6.9	8	V	-
Quiescent Operating Voltage at Terminal 5(8)	$V_{5(8)}$	-			5	6.9	8	V	-
Output Offset Voltage between Terminals 4 and 5(5 and 8)	V_{4-5} (5-8)	-			-1	0	1	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER IN TO-5 STYLE PACKAGE)									
Input Voltage Sensitivity	V_I sensitivity	5	V^+ = +30 V, V_I = 18 mV		Correction Voltage Output as shown in table below.				
Input Admittance	y_{11}	-	f = 45.75 MHz, V^+ = 30 V, R_S = 1.5 kΩ		-	0.41 + j1.0	-	mmho	-
Reverse Transfer Admittance	y_{12}	-			-	0 +j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-			-	24.5 - j29	-	mmho	-
Output Admittance	y_{22}	-			-	0.04 + j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC									
Correction-Control Voltage at Terminal 4(5)	$V_{corr.\ 4(5)}$	5	V^+ = +30 V, V_I = 18 mV RMS, f_o = MHz as indicated	45.750 - 0.030	85	-	-	V	6,7
				45.750 + 0.030	-	-	25	V	
				45.750 - 0.900	80	-	-	V	7
				45.750 + 0.900	-	-	35	V	
				45.750 - 1.500		-	80	V	
				45.750 + 1.500	35	-		V	
Correction-Control Voltage at Terminal 5(8)	$V_{corr.\ 5(8)}$	5		45.750 - 0.030	-	-	25	V	6,7
				45.750 + 0.030	85	-	-	V	
				45.750 - 0.900	-	-	35	V	7
				45.750 + 0.900	80	-	-	V	
				45.750 - 1.500	35	-	-	V	
				45.750 + 1.500	-	-	80	V	

* Terminal numbers in parentheses are for 14-lead dual-in-line plastic package.

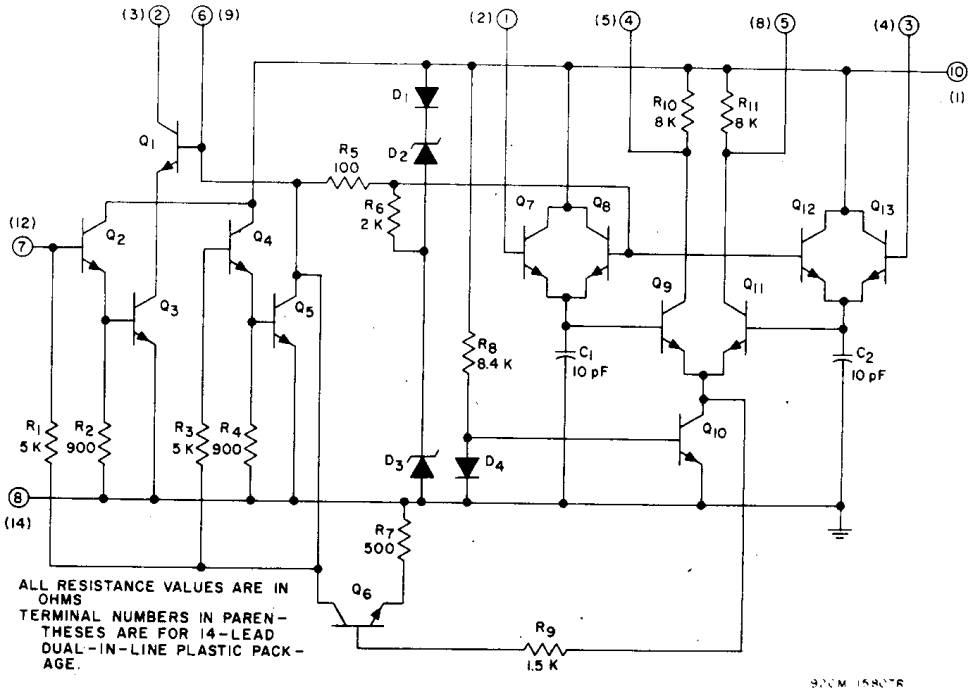


Fig.3 – Schematic diagram for CA3064 and CA3064E.

Circuit Description

The CA3064 and CA3064E integrated circuits can be considered as five functional blocks; an if amplifier-limiter, a balanced detector, a differential dc amplifier, an internally used AGC amplifier, and a zener voltage regulator. The 45-MHz amplifier limiter combination consists of emitter-follower input stage Q2 followed by a cascode-type amplifier Q1, Q3. The emitter-follower input stage Q2 is internally biased, therefore, capacitor coupling must be provided to the input at pin 7 (12) . The external load is connected to pin 2 (3) and should present a load impedance of about 1800 ohms at 45.75 MHz. The detector inputs at pins 1 (2) and 3 (4) from the external transformer are biased through the tertiary winding connected to pin 6 (9), which must be bypassed. The balanced detector is a high-efficiency type consisting of Q7/C1 and Q13/C2, which are internally biased by matching transistors Q8 and Q12. The dc amplifier consists of the differential amplifier Q9, Q10, Q11, and D4.

The amplifier detector system provides the sharply defined pull-in characteristics shown in figures 5 and 6. The AGC amplifier Q6 senses the detected signals at the collector of A10 and adjusts the gain to compensate for signal changes such as airplane flutter conditions. Diodes D1, D2, and D3 provide the internal voltage regulation.

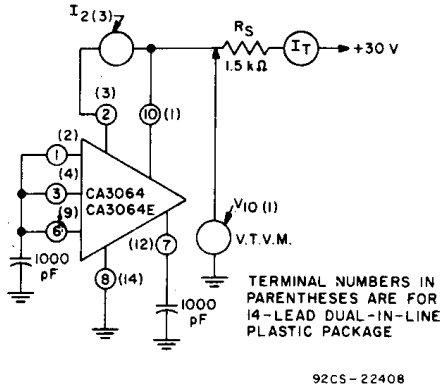
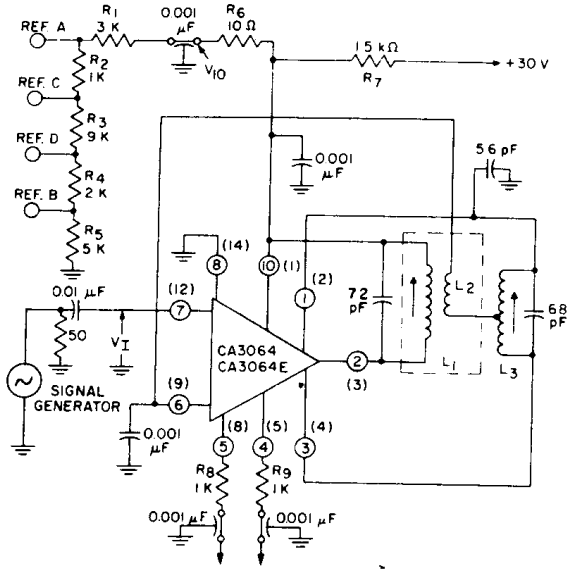


Fig.4 – Test setup: Measurement of total device dissipation, zener regulating voltage, quiescent operating current at terminal 2 (3).



CONTROL VOLTAGE OUTPUT

ALL RESISTORS ARE 1% TOLERANCE AND ARE IN OHMS
TERMINAL NUMBERS IN PARENTHESES ARE FOR 14-LEAD DUAL-IN-LINE PLASTIC PACKAGE

92CS-15813R1

L_1 IS ALIGNED FOR SYMMETRICAL BANDWIDTH ON EITHER SIDE OF 45.750 MHz
L_2 TERTIARY WINDING WOUND ON L_1 COIL FORM
L_3 IS ALIGNED FOR ZERO DIFFERENTIAL OUTPUT BETWEEN TERMINALS 4 AND 5 AT f_o = 45.750 MHz

* FOR COIL CONSTRUCTION DATA, SEE FIG.4(b).

REFERENCE VOLTAGE PERCENTAGES	
Ref. A	85% of $V_{10(1)}$
Ref. B	25% of $V_{10(1)}$
Ref. C	80% of $V_{10(1)}$
Ref. D	35% of $V_{10(1)}$

Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

Fig.5 (a) – Correction voltage test circuit for CA3064 and CA3064E.

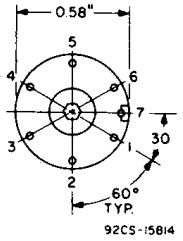
COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 – Discriminator Primary: 3-1/6 turns; #20 Enamel-covered wire – close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2-1/6 turns; #20 Enamel-covered wire – close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3-1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz. Start winding at Terminal #2; finish at Terminal #5; connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; –0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.



92CS-15814

Fig.5 (b) Coil form base terminal diagram.

The CA3064 and CA3064E are specifically intended for use in the AFT system of color television receivers. These devices are tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 (a) is the schematic diagram of the test circuit.

Figures 5, 6, and 7 show the control voltages generated at terminals 4(5) and 5(8) of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 30 kHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on terminal 10(1) and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is –30 kHz the control voltage at terminal 4(5) is greater than the reference A voltage; the control voltage at terminal 5(8) is less than the reference B voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit boards shown in Figures 8 and 10 and the parts layouts shown in Figures 9 and 11 should be followed as closely as possible.

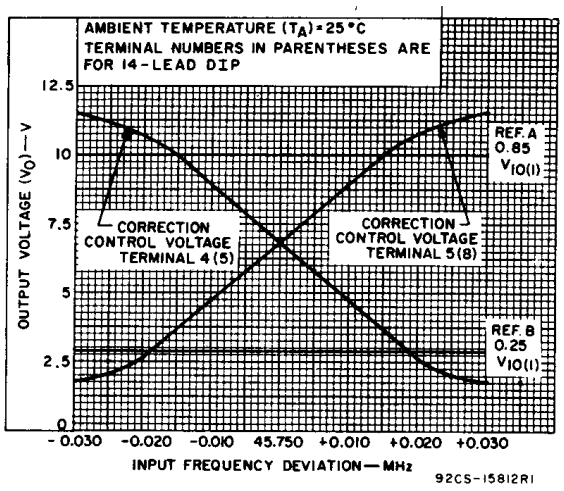


Fig.6 – Typical narrow-band dynamic control voltage characteristics.

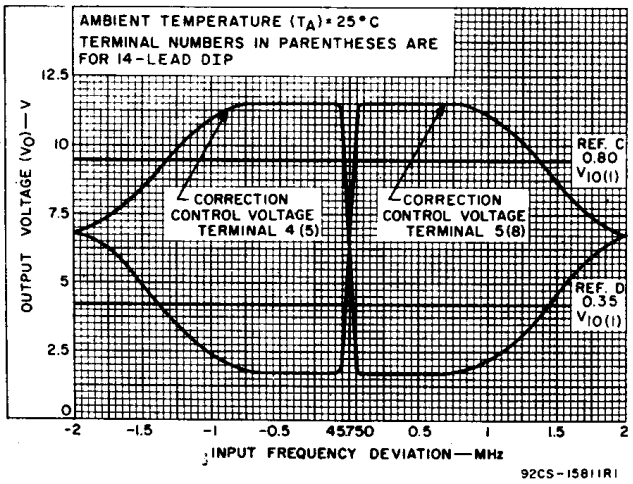


Fig.7 – Typical wide-band dynamic control voltage characteristics.

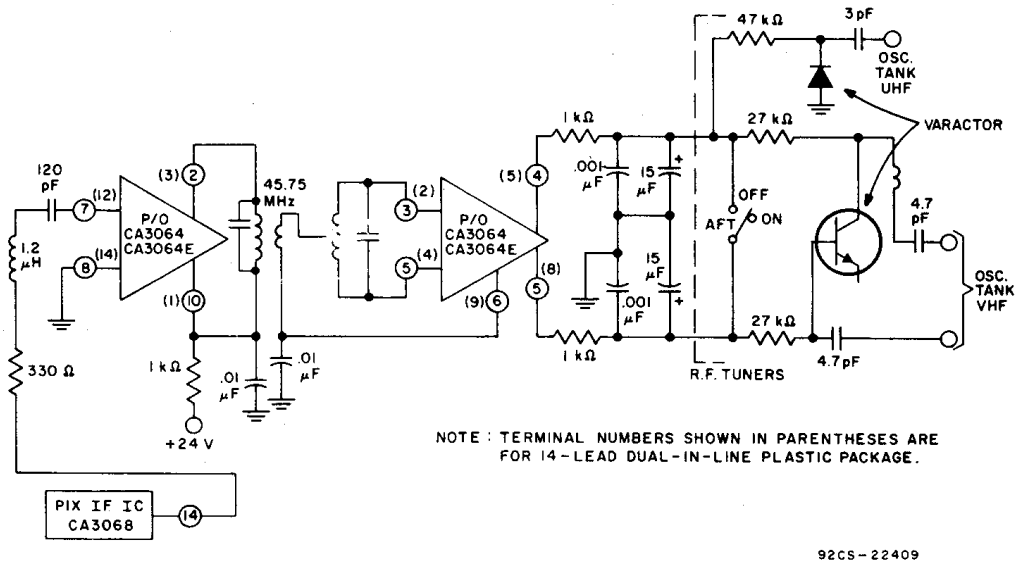
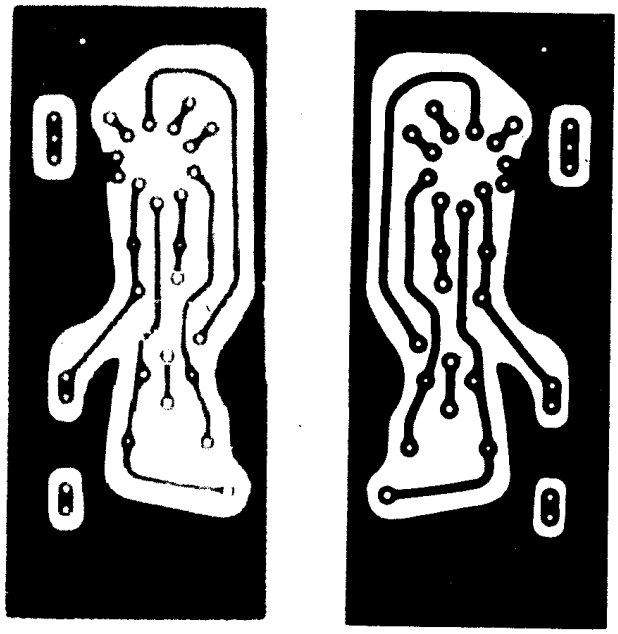


Fig.8 – Typical application of CA3064 and CA3064E AFT IC.



(a) Top view (b) Bottom view

Fig.9 – Printed circuit board for test circuit, full size (for TO-5 style package).

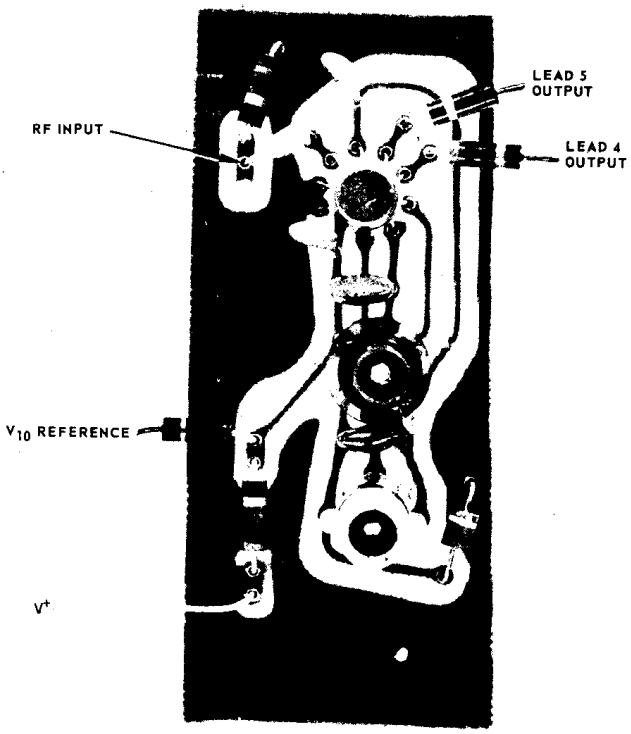
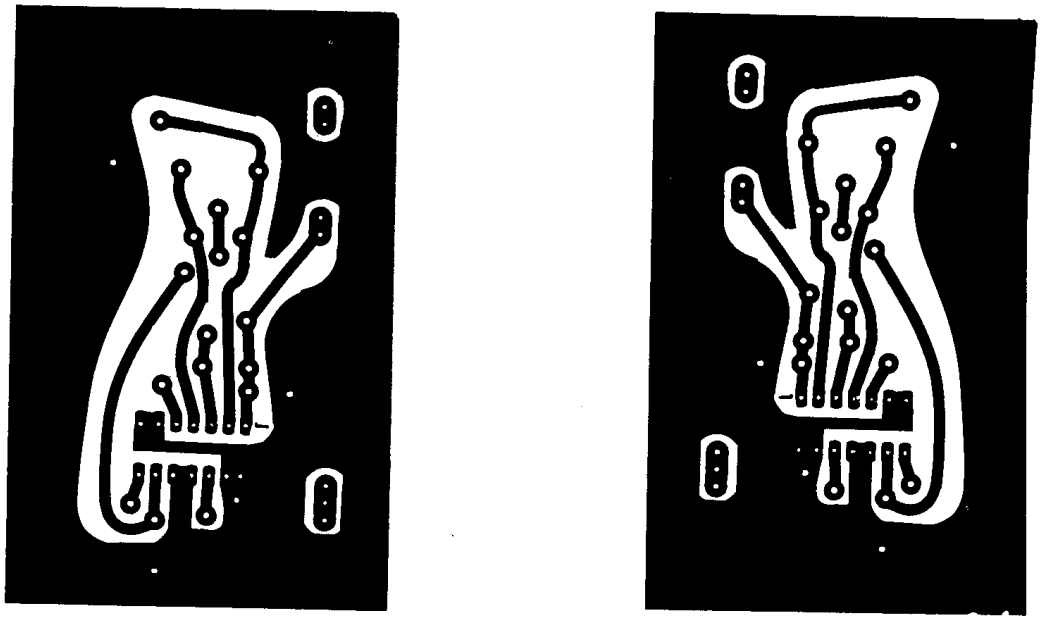


Fig.10 – Top view of wired test board (for TO-5 style package).



(a) Top view (b) Bottom view

Fig.11 – Printed circuit board for test circuit, full size (for 14-lead dual-in-line plastic package).

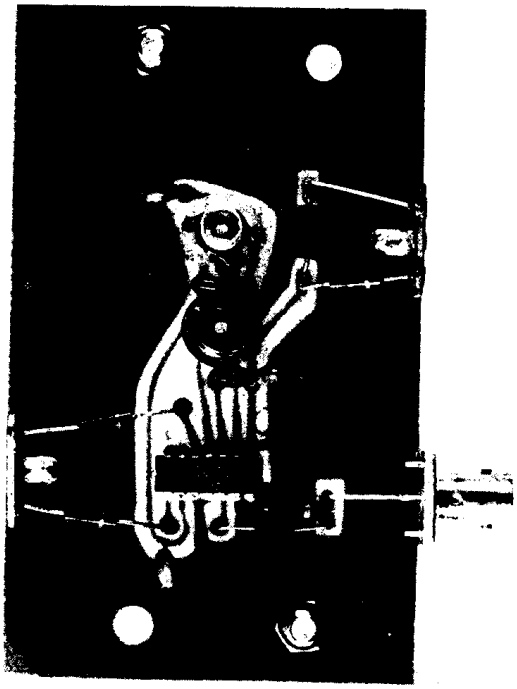


Fig.12 – Top view of wired test board (for 14-lead dual-in-line plastic package)