MTC-20172

'S' Interface Circuit for ISDN (SIC)

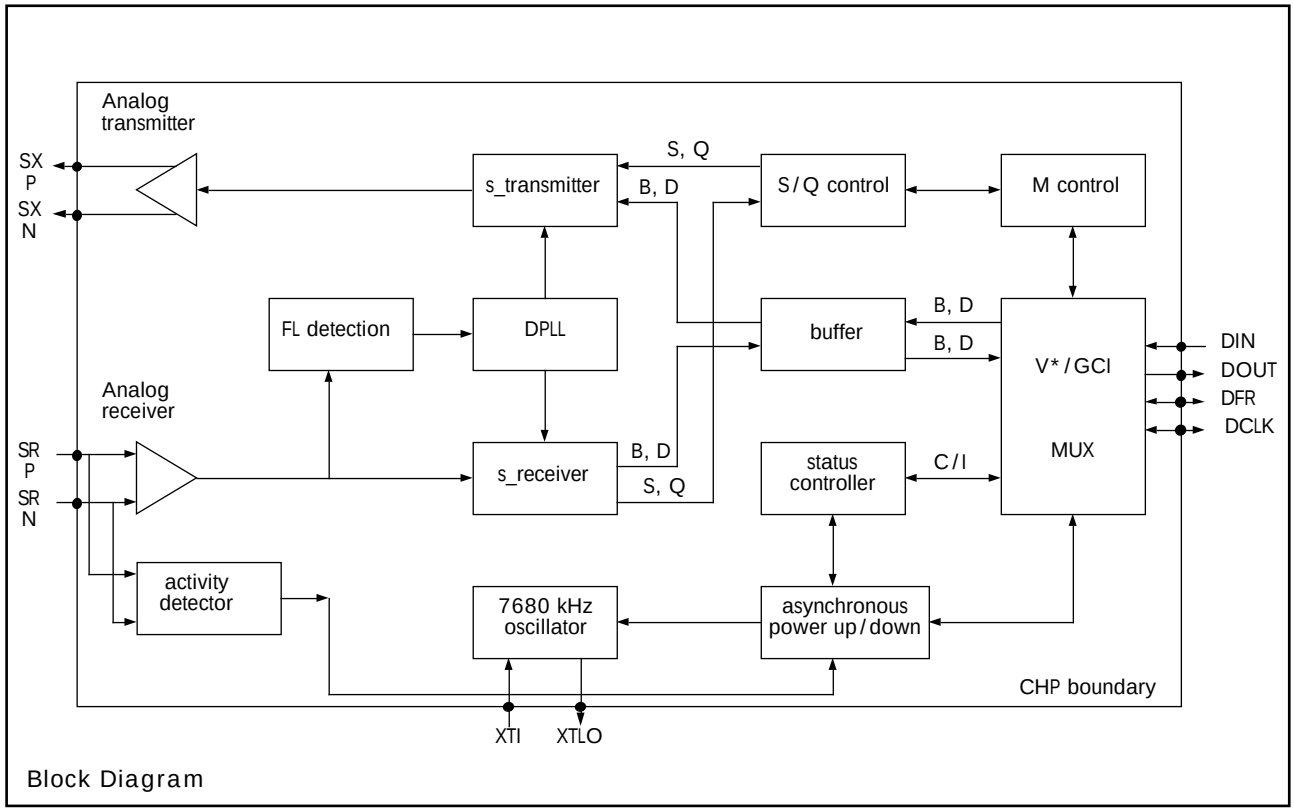
Data Sheet & Reference Manual

Rev. 1.1 February 1997
Application Specific Standard Products

Features

- Single chip 4 wire S_0-interface for ISDN
- Basic access at 144 kbits/s, with 2B+D
- Complying with CCITT I.430
- Applicable in all ISDN So-interface Configurations :
  - NT : Network Termination
  - TE : Terminal Equipment
  - LTS : Line Termination Subscriber
  - LTT : Line Termination Trunk
- Switching of Test-loops
- S-bus drivers with high-impedance when not powered
- Balanced S-bus receivers
- Line-length up to 1.2 km in point-to-point configuration
- Handles V*, IOM1™, IOM2 ™ and GCI digital interfaces
- Supports Multiframing
- Includes Maintenance channel
- Absorption of clock wander in LTT mode
- Operating power < 50 mW
  Stand-by power < 3 mW
- Single 5V supply

™ IOM is a trademark of Siemens



Block Diagram

ERRATA

Page 56, Table 6.4.b, shows incorrect command codes for the AId and AIL states. The correct table is given here.

6.5.8 Command and Indications for NT Applications.

Table 6.4.a : MTC-20172 SIC C/I : NT overview

NT	Downstr Command	Upstr. Indicat.		Downstr Command	Upstr. Indicat
0000	DR	TIM	1000	ARd	ARu
0001	-& * RES	(lsl)*&-	1001	-	-
0010	ssz=TM1	-	1010	ARL	-
0011	-& * TM2	-	1001	-	-
0100	RSYd	RSYu	1100	AId	Alu
0101	-	- ++	1101	-	-
0110	-	ei * &-	1110	AIL	-
0111	-	-	1111	did=DC	Dlu

++ *MAIC is NOT implemented.*
* *Marks functional differences (4 in total).*
& *Marks functional differences which are merged for both devices.*

6.5.8.1 Commands (Downstream) in NT Mode

Table 6.4.b : MTC-20172 SIC commands (DS) NT

0000	DR #	Deactivate Request	Forces MTC-20172 SIC to deactiv. the S-bus (=INFO0) followed by Dlu and did=DC
0001	*RES # &	RESET	Forces MTC-20172 SIC to soft reset, extended mode only, MTC-20172 SIC accepts it in basic mode (merged)
0010	ssz # = TM1	TEST-MODE 1	Forces MTC-20172 SIC to test-mode 1, sending single zeros
0011	*TM2 # &	TEST-MODE 2	Forces MTC-20172 SIC to test-mode 2, extended mode only, sending continuous zeros, command is extended to the basic mode of the MTC-20172 SIC
0100	RSYd	Resynchon-izing down	The U-interface is not synchronous, MTC-20172 SIC sends INFO2 {or SCZ}, see remark 1 below
1000	ARd	Activation Request down	MTC-20172 SIC forced to INFO2 transmission, receiver indicates the S-bus reaction
1010	ARL	Activat. req with S-loop	INFO2 transmission on the S-bus test loop2 switched (transparent loop)
1100	AId	Activation Indication	INFO4 transmission, normally only after Alu indication is received
1110	AIL	Activ. Indic. with S-loop	INFO4 transmission test loop2 switched (transparent loop)
1111	did= DC	Deactivate Confirmation	Deactivation confirmation, entering the power down state, INFO0 sent, critical timing to halt the clocks, see 6.2.4

* *Marks functional difference;*
& *Marks differences that are merged.*
\# *Unconditional commands, which force an unambiguous state.*

Remark 1: When the U-interface is resynchronizing, the basic mode sends Continuous Zeros, the extended mode sends INFO2. MTC-20172 SIC will send INFO2.

Remark 2: During loops, the MTC-20172 SIC simply ignores the incoming INFO3 from the S-bus. The receiver synchronizes on looped INFO2/4.

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13. Application Note : Network Terminator

List of Abbreviations

AGC	Automatic Gain Control
AMI	Alternating mark inversion
CLCC	Ceramic Leaded Chip Carrier
C/I	Control/Indication
CMOS	Complementary MOS (Metal Oxide Silicon) technology
D-AC	D-channel Access Controller
DIL	Dual In-Line package
DPLL	Digital Phase Locked Loop
ESD	Electro Static Discharge
ILC	ISDN - link - controller
IOM	ISDN Oriented Modular (interface), Siemens Trademark
ISDN	Integrated Services Digital Network
GCI	General Circuit Interface
HDLC	High-level Digital Link Control, see also LAPD
LAPD	Link Access Protocol for D-channel, CCITT Q.921
LCL	Longitudinal Conversion Loss
LSB	Least Significant Bit
LT	Line Termination, see Figure 4.1
LT-S	Line Termination at the S interface (S-bus toward TE)
LT-T	Line Termination at the T interface (S-bus toward NT)
MSB	Most Significant Bit
NT	Network Termination, see Figure 4.1
NT1	Network Termination, see Figure 4.1
NT2	Intelligent Network Termination, see Figure 4.1
PABX	Private Automatic Branch Exchange
PCBA	Printed Circuit Board Assembly
PLCC	Plastic Leaded Chip Carrier
PLL	Phase Locked Loop
RAM	Random Access Memory
RX	Receive
SDL	System description language
SIC	S-interface-circuit
SLMD	Subscriber line module digital
SIC	S-interface Integrated Circuit
TE	Terminal equipment, see Figure 4.1
TX	Transmit
UIC	U-Interface Circuit
VLSI	Very Large Scale Integration
X-tal	crystal

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1. General Description

The MTC-20172 is an enhanced version of the MTC-2072 SIC. In addition to the basic line interface functions, the MTC-20172 offers digital interfaces compatible with most commonly used standards (V*, IOM1™, IOM2™, GCI), as well as extended monitor channel functions and multi-framing. The use of state-of-the-art process technologies and restructuring of the analog functions results in greatly enhanced analog performance.

The S_0-interface circuit (SIC) enables full duplex digital data transmission (2B+1D) over the So-interface. The SIC can be used as a 'Network Termination' (NT), providing transparent data transmission from the digital interface to the So-interface and vice versa. As a 'terminal equipment' device (TE), the SIC is connected to a "layer 2" device (e.g. ISDN Link Controller; MTC-2074 ILC) which provides HDLC data formatting for the D channel, etc... To connect an ISDN PABX unit to the public network, an SIC can be used as a 'Line Termination Trunk side'-device (LTT). In addition, a 'Line Termination Subscriber side' (LTS) mode is available (fig.1), which is similar to NT but offers simpler activate/deactivate procedures.
A digital serial interface provides a link between the MTC-20172 SIC and, for example, the MTC-2071 4B3T U-Interface, the MTC-2074 ILC (HDLC and DMA controller) or other communication devices. The digital serial interface supports V*, IOM1™ , IOM2™ and GCI, so is compatible with many other integrated circuits for ISDN communications. The SIC contains all necessary functions for direct connection to the S_0-interface, and specifically the critical analog transmitter and receiver stages.

(See also section 4).

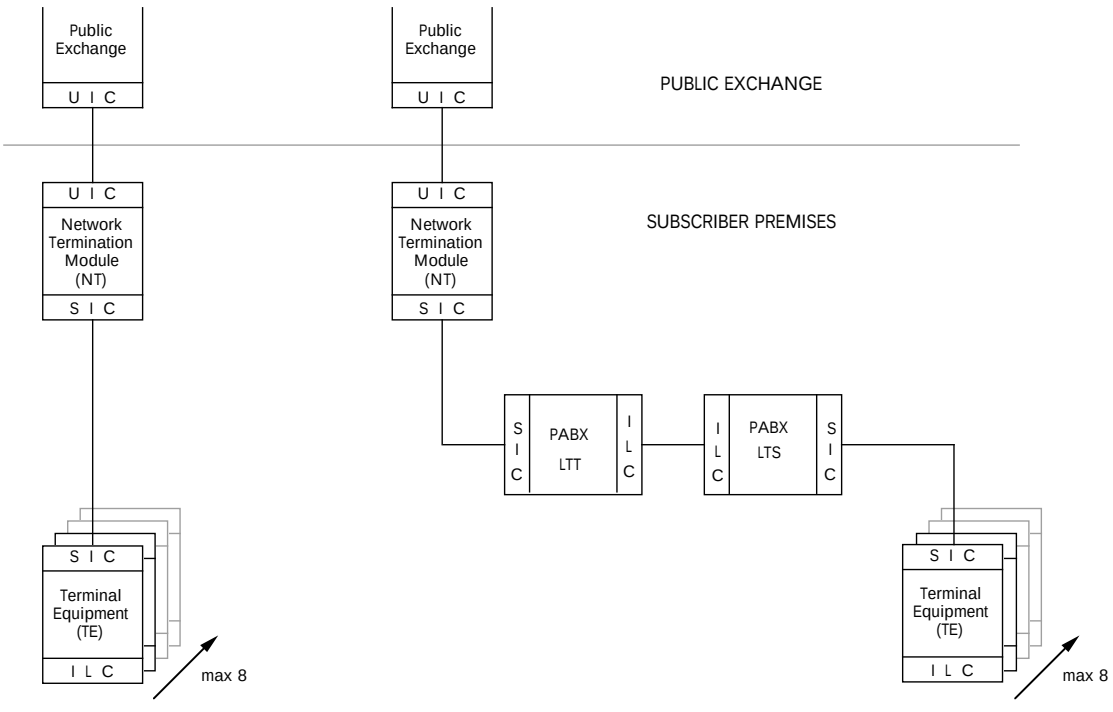


Fig. 1 : Typical Application

2. Interface and Operation Overview

2.1 The Digital Interface

Each ISDN configuration (NT, TE, LTS, LTT) is supported in either V* or in GCI standards. The serial interface is made up of frames of 125 µs. Each frame can have from 32 to 512 bit positions and is divided into channels of 32 bits. Each bit takes 2 cycles of the data clock DCLK (with a frequency from 512 kHz to 8192 kHz). The start of a 125 µs frame is synchronized with a DFR (Data FRame) signal of 8 kHz. In TE modes, the SIC is master of the digital interface, in NT, LTS and LTT modes, the SIC is a slave.

Depending on the mode selected, several frame formats are possible :

Normal Mode (fig. 2.1)
DCLK can go from 512 kHz to 8192 kHz with intervals of 16 kHz (32 to 512 bits/frame).

The rising edge of DFR marks the start of the frame and should be high for at least 2 DCLK periods.
Depending on the DCLK frequency, a maximum of 8 channels are available. The bits of the higher channels are unused.

This mode is applicable in all configurations.

V* Inverted Mode (fig. 2.2)
Inverted frame and data clock.
DCLK = 512 kHz (32 bits/frame)
DFR goes low for 1 clock cycle at the end of position 27.

Only 1 channel is available.
This mode is applicable in TE mode.

V* Inverted Multiplexed Mode (fig. 2.3)
Inverted frame and data clock.
DCLK = 4096 kHz (256 bits/frame)
DFR goes low for 1 clock cycle at the end of position 251.

8 channels are available.

This mode is applicable in LTT and LTS modes.

Remark: In LTS and LTT applications, there is automatic recognition of inverted multiplexed and normal modes.

A channel of 32 bits is divided into 4 bytes (fig. 2.4):

1st byte B1:
First transparent data channel of 64 kBits/s.

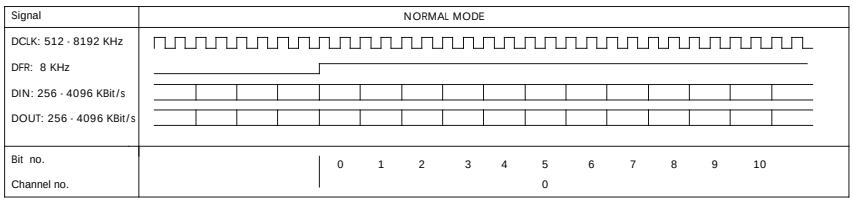


Fig. 2.1 : Timing in Normal Mode

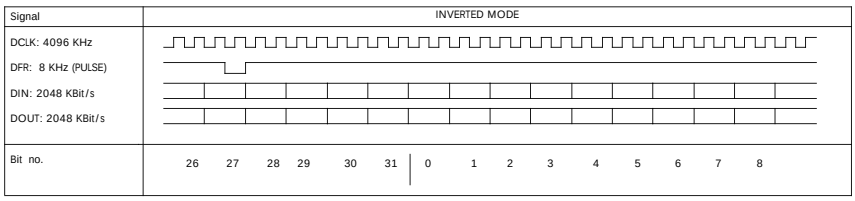


Fig. 2.2 : Timing in V* Inverted Mode

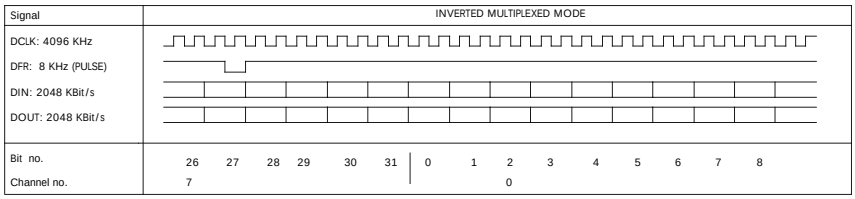


Fig. 2.3 : Timing in V* Inverted Multiplex Mode

2nd byte B2:
Second transparent data channel of 64 kBits/s.

3rd byte B2*:
Monitor channel, with (in TE and LTT) the D-channel status in the 5th bit position.

4th byte B1*:
D1, D2: Two transparent D-channel bits at 16 kBits/s.
C/I: Four Command/Indication channel bits. These are used for activation or deactivation and test modes.

The interpretation of the received command codes and the transmitted Indications follow the V* or the GCI C/I code tables.
MR, MX: Two handshaking bits to control the monitor channel access.

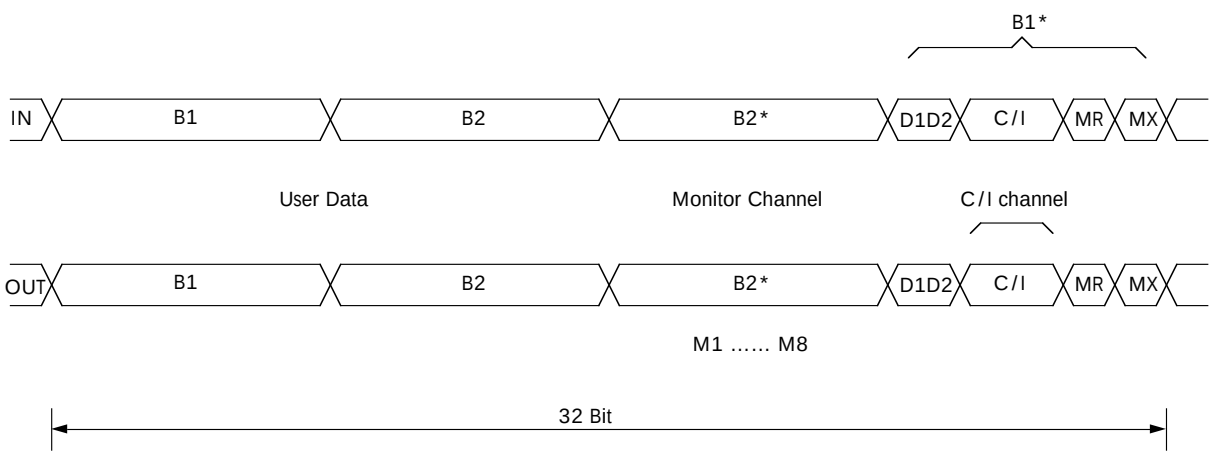


Fig. 2.4 : Format of a V* CGI Channel

The possible combinations of ISDN configurations, frame format and activation/deactivation procedures are shown in TABLE 2.1.

Table 2.1 : Possible Mode combinations

ISDN configuration	Frame format	DCLK frequency (kHz)	Available channel	Activation/ Deactivation according to
TE(†)	Inverted	512	1	V*
TE(†)	Normal	512	1	V*
LTS/LTT(†)	Inverted multiplexed	4096	1-8	V*
LTS/LTT	Normal	512-8192	1-8	V*
LTS/LTT(†)	Normal	512-8192	1	V*
NT(†)	Normal	512-8192	1	V*
TE	Normal	1536	1	GCI
LTS/LTT	Normal	512-8192	1-8	GCI
NT	Normal	512-8192	1	GCI

(†) Compatible with the MTC-2072 SIC.

2.2 The So-Interface - Functional overview

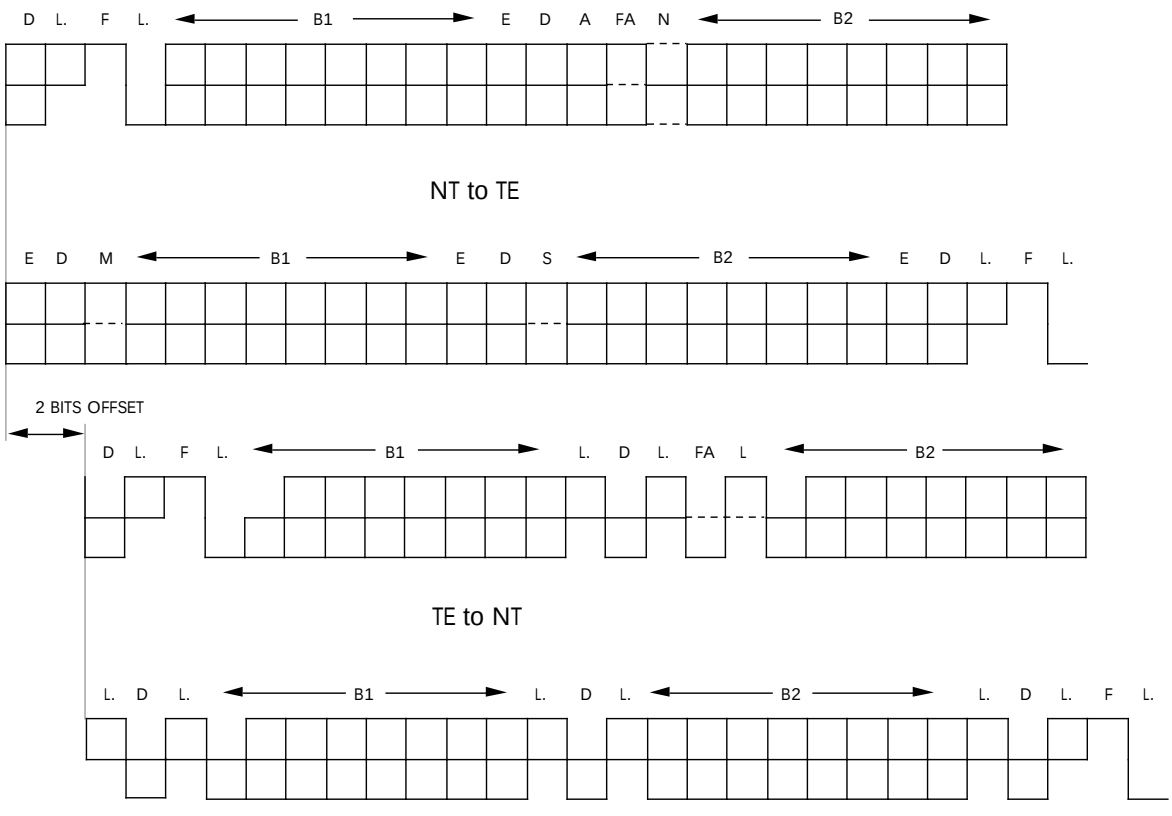
For transmission of data over the subscriber premises, the SIC provides the S_0-interface. This interface enables full duplex transmission of data (2B + 1 D-channel) over 4 wires at a nominal data rate of 192 kBits/s. An Alternating Mark Invert (AMI) code is used for the line transmission. The transmission of data over the S_0-interface consists of frames of 250 µs. Each frame is 48 bits wide, and contains 4 data bytes (2 B1, 2 B2) and 4 D-bits.

The frame structures are shown in fig.2.5.

A frame start is marked using a first code violation (no mark inversion). To allow secure synchronization of the receiver, a second code violation is generated before the 14th bit of the frame. To guarantee this second violation, an auxiliary framing bit pair FA and N (from NT to TE) or the framing bit FA with associated balance bit (from TE to NT) are introduced.

The first bit of the transmitted frame from TE to NT is delayed for 2 bit periods with respect to the frame received from the NT. Furthermore, an echo bit (E-bit) for the D-channel and an activation bit (A-bit) are provided, where DC-balancing is done by means of the L-bits.

The SIC supports multi-framing according to CCITT I.430 recommendations - the capability of transmitting an S-channel from NT to TE and a Q-channel from TE to NT of 800 baud is provided for. The S and Q data can be accessed via the monitor channel.



F : FRAMING BIT
L : DC BALANCING BIT
D : D-CHANNEL BIT
E : D-CHANNEL ECHO-BIT
FA : AUXILIARY FRAMING BIT

N : = $\overline{FA}$
B1 : BIT OF CHANNEL B1
B2 : BIT OF CHANNEL B2
A : ACTIVATION BIT
S : S-BIT
M : MULTIFRAMING BIT

Fig. 2.5 : So-Frame Format

The SIC can be used in a point-to-point and in a point to multipoint configuration (including extended passive bus). In the first configuration, the length of the cable is limited to aprox. 1.2 km (see fig.2.6).
In the bus configuration (point to multipoint), up to 8 terminals may be connected to the S_0-interface (fig.2.7).

The terminals must be connected in a range of 150 m. For the extended passive bus, the terminals must be clustered within a 25m range with a maximum cable length of about 1 km.

To avoid bus mismatching when multiple TEs are connected, the driver stages present a high impedance when they are not powered.

Controlled access to the shared data channels is realized within the SIC by a D-channel access procedure. Each terminal can be given a certain priority for D access. Via the echo bit, which is the reflection of the received D channel at the NT, it is possible for the terminal to detect the status of the D-channel. In order to try to gain access over the D-channel, a terminal has to see 8 to 11 consecutive ones in the echo-channel. The exact number depends on the priority given to the terminal. When several terminals try to gain access at the same time, collisions occur on the S-bus. The terminal that transmitted "one" but sees a “zero” in the echo channel detects the collision and loses the D-channel access.

The terminal that transmitted the "zero" gains the access. When a successful D-channel message is transmitted, the priority is decreased by 1 in order to guarantee fairness with the other terminals. The status of the D-channel of the TE/LTT is available at a device pin, or at the 5th bit position of the monitor byte. This enables the control of the D-channel by an external HDLC controller.

At the NT/LTS side, the echo bits of several NTs can be combined in an external common echo bus (wired AND) in an NT-star configuration. At the LTS side, the same external common echo bus can be used to share an external HDLC controller between several LTS SICs.

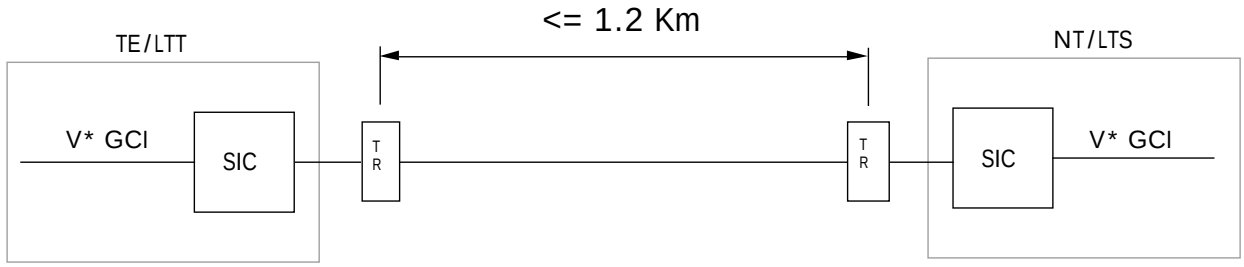


Fig. 2.6 : Point to Point Configuration

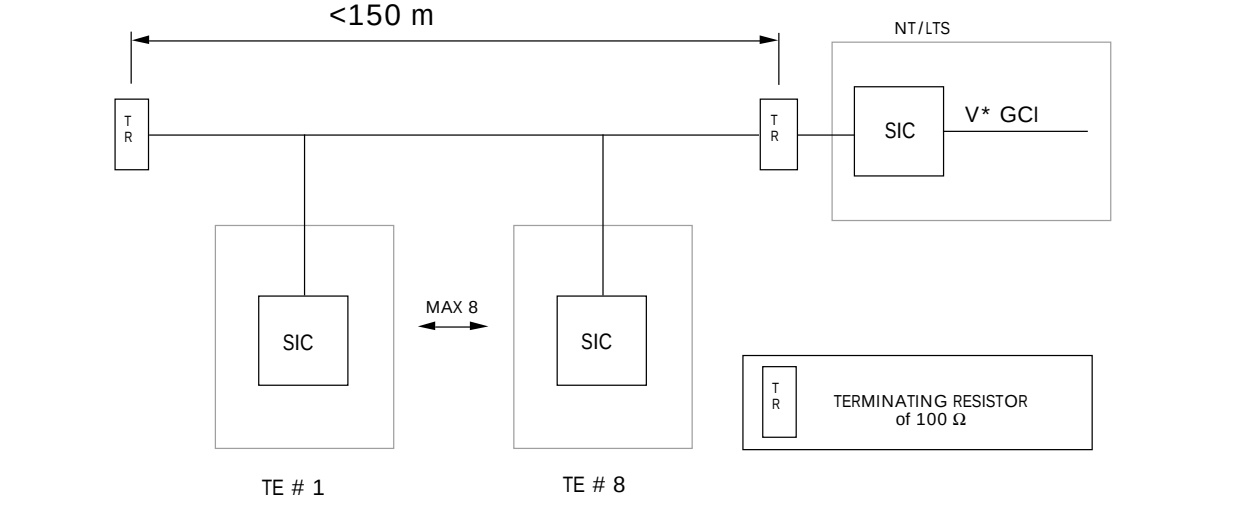


Fig. 2.7 : Point to Multipoint Configuration

2.3 The MTC-20172 SIC Operation Overview

The block diagram is shown in fig.2.8.

Data from the So-interface is received by the SIC receiver, which has a balanced input, an AGC stage, a filter and comparators with dynamically adapted thresholds. The timing of the received S_0-frame can either be a fixed (Only NT/LTS) or adaptive timing.

In the fixed timing case, the timing is locked to the transmitted frame, and the tolerable phase delay on the received So-frame is limited. In adaptive timing mode, delays up to 48 µs can be tolerated. The start of the received frame is detected in the FL-detection unit. An adaptive algorithm is used for compensation of the slope of the FL transition. A digital PLL recovers the received bit clock (192 kHz).

A second digital PLL generates the transmit bit clock (192 kHz), which is locked to the GCI frame in the case of NT/LTS, or is locked to the received So-frame in the case of TE/LTT applications. It is possible to compensate external circuits (e.g. filters) by adjusting the internal phase of the bit clocks by means of a device pin, or by means of a register accessible by the monitor channel.

These circuits work with a 7680 kHz ±100 ppm clock. This clock can be delivered to the SIC by an external generator, a UIC (for NT modes), or can be generated by an on-chip oscillator.

The serial B and D data from the V* GCI digital interface is stored into a buffer with a dynamic pointer structure, and is presented to the S_transmitter where the So-frame formatting is done. In the other direction, the S_receiver unit disassembles the received So-frame. The B and D data are stored in the buffer and multiplexed together with M, C/I, MX and MR into a digital V* GCI frame. The pointer structure of the buffer guarantees a minimum round-trip delay in NT, LTS and TE modes, and is able to compensate the clock wander in LTT mode. If the clock wander becomes too big, a warning is given in the C/I channel, and the internal pointers are reinitialized.

Activation/deactivation procedures are handled in the status controller. Two basic modes are available: A V* mode, compatible with the MTC-2072 SIC and other earlier ISDN devices, and an GCI compatible mode.

The S/Q control module handles the multiframing on the S and the Q channel of the So-interface. Multiframing is enabled in NT/LTS mode by a width modulation of the frame synchronization signal DFR every 40th GCI frame, a monitor programmable register, or by an auxiliary device pin.

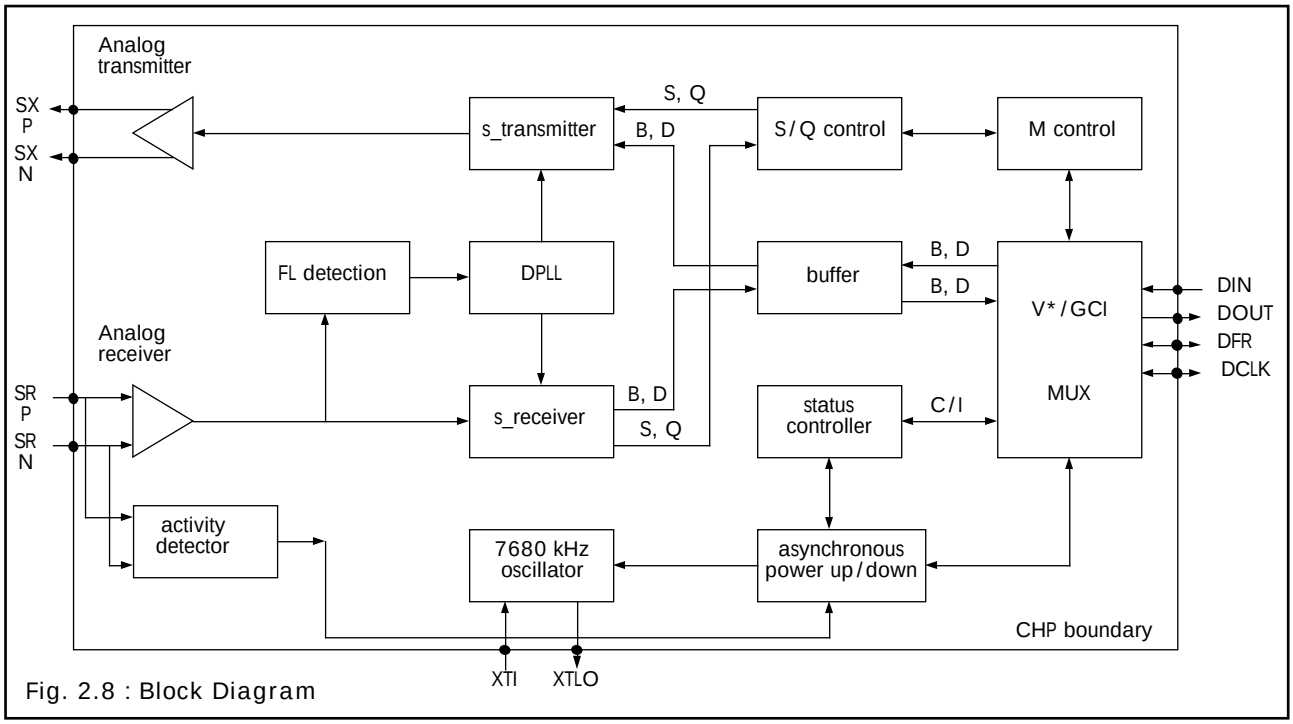


Fig. 2.8 : Block Diagram

The M control unit interprets and responds to messages on the monitor channel. Via this channel, access is possible to the S/Q bits and configuration registers. Observation of some user-defined input pins is also possible.

In order to reduce the power consumption of the components connected to the subscriber line, the SIC may be switched to a power down mode during idle periods. In NT and TE modes, the internal clock distribution and the oscillator are turned off, and the power consumption is less than 3 mW. The component is automatically powered up again during the line activation procedure. The power consumption when activated, with an applied DCLK clock of 512 kHz is less than 50 mW

2.4 Test Modes Summary

Two test loops may be closed in the SIC, which depend on the selected mode of operation. In both modes, all three channels (B1, B2 and D) are looped back as close as possible to the So-interface.

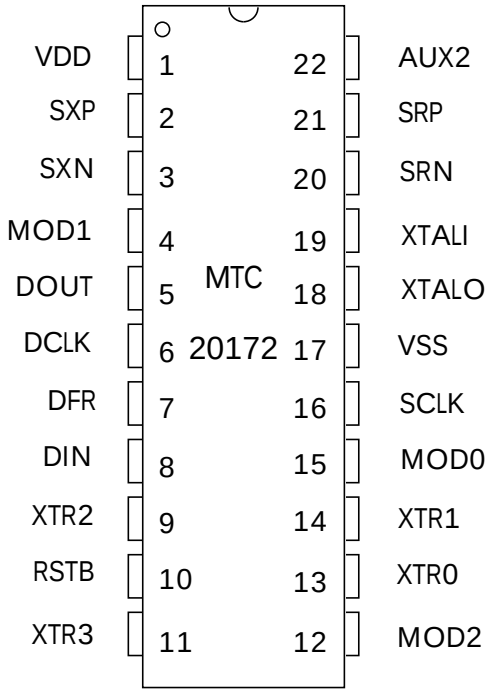
Loop 2 (NT, LTS) is a transparent loop (fig.2.9a) where the transmitted So-frame is also switched on the S-bus. Activation from the So-interface is not possible.

Loop 3 (TE, LTT) is a non-transparent loop (fig.2.9b) where the transmitted So-frame is not switched on the S-bus so as not to activate the NT/LTS. Activation from the S-bus is possible, and is indicated by a special code in the C/I channel.

Both loops are initiated over the C/I-channel and under control of a layer 2 component.

For further testing of the subscriber line, two test signals can be transmitted over the So-interface: A 96 kHz test sequence sending continuous AMI marks, and a 2 kHz test sequence sending single AMI marks. Both test modes are under control of the C/I channel and (in NT mode) by means of device pins.

a) 22 PDIL : MTC-20172-PD



b) 28 PLCC : MTC-20172-PC

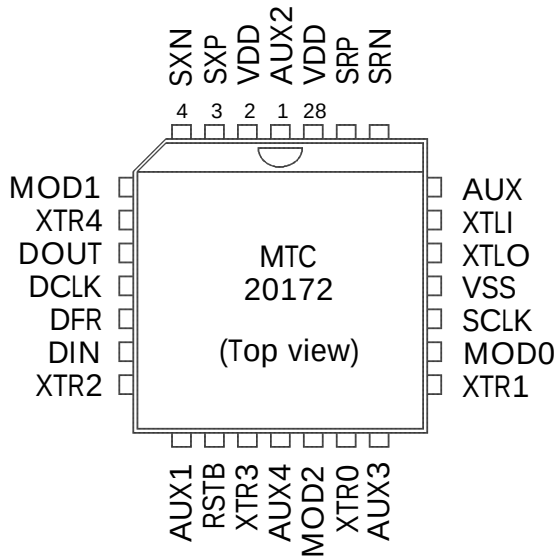


Fig. 2.9 : Pin Descriptions

3. Pin and Package Data

3.1 Package and Dimensions

The MTC-20172 SIC is available in two package styles. For specific requirements, please contact your Mietec representative.

28 pin plastic leaded chip-carrier (28PLCC). Details on the DIL and PLCC packages are shown in Figure 3.1 and in Figure 3.2 respectively.

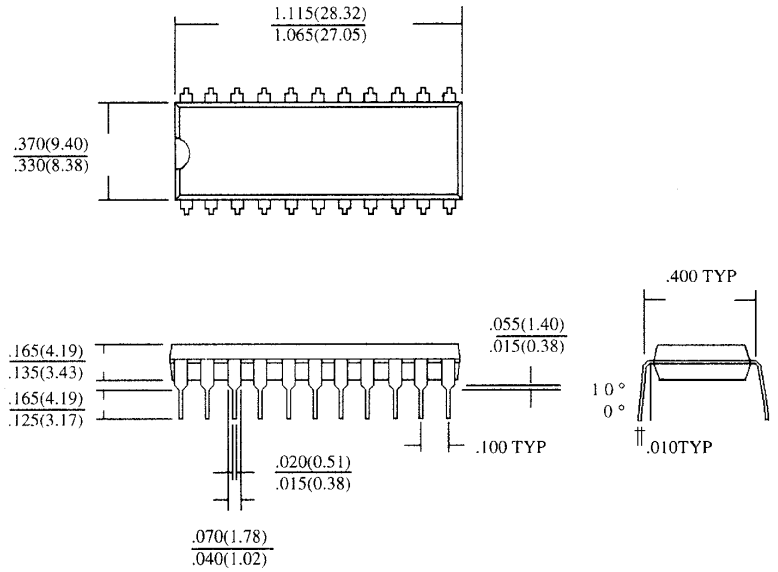


Fig. 3.1 : 22 pin DIL package and dimensions

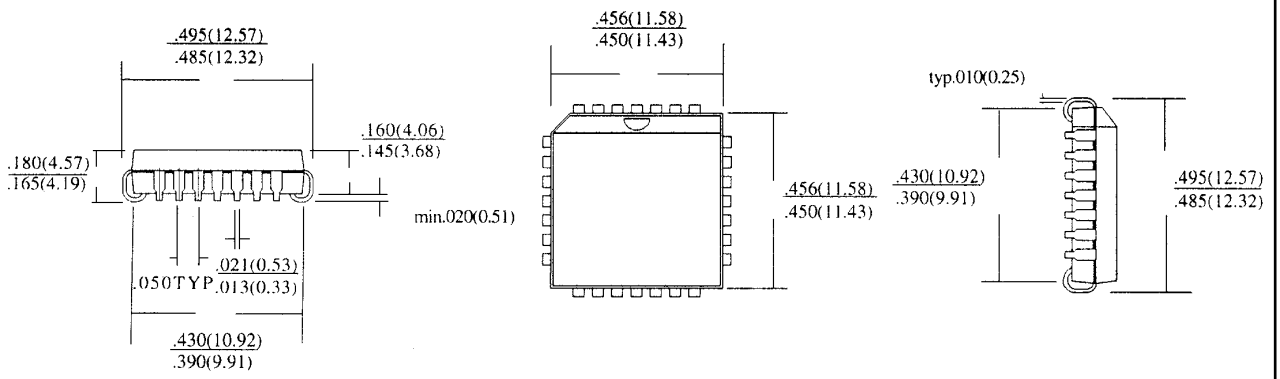


Fig. 3.2 : 28 pin Square PLCC Package and dimensions

3.2 Pin Allocation and Brief Description

Table 3.1 contains the pin number for the each package style, the pin name, I/O type, and a brief description. The I/O column describes the Input/Output buffer type used. The 22 pin plastic DIC version supports only the basic operation mode.

The I/O types are :

P = Power pin
IO = Input and push-pull output with tristate;
I = Input only;
IW = Input only, weak pull-up resistor internally;
O = Push-pull output, tristate possible;
OD = Output with open drain, no internal pull-up;
ODP = Output with open drain, internal pull-up in some modes;

AO = Analog output;
AI = Analog input;
AT = Analog test pin, input and output;
XI = crystal input; XO = crystal output.

S = Strap (user), fixed to 1 or 0.

Some pins have different I/O function or type depending on the mode, listed in Table 3.3 and paragraph 3.5. Detailed configuration of all pins in paragraphs 4.11 and 4.12, Tables 4.1 and 4.2. The electrical I/O properties are described in 9.5 and 9.6.

The pin configuration is found in Figure 3.3 and 3.4.

** see 6.5*

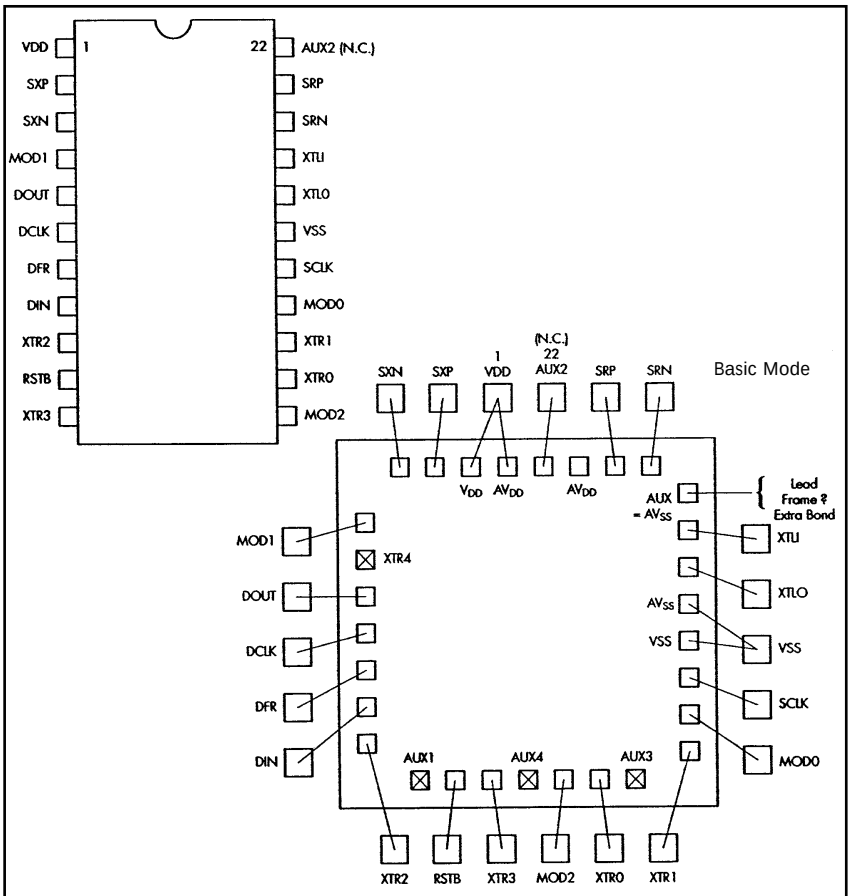


Fig. 3.3 : 22 pin DIP, Signal Names

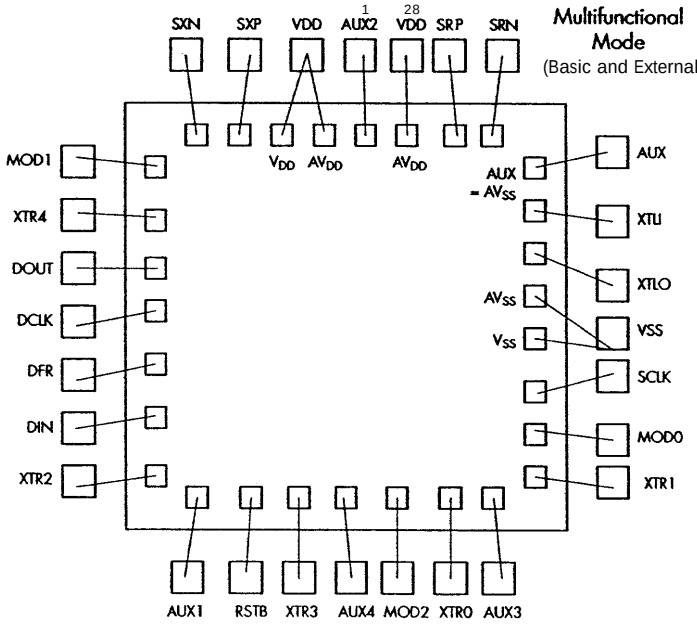


Fig. 3.4 : 28 pin Square PLCC Package, Signal Names

Table 3.1: Pin List and Description, 22 and 28 pin Package

28 pin	22 pin	pin name	I/O	Description
2	1	VDD	P	Supply voltage +5V 5%
22	17	VSS	P	Supply voltage 0V
13	10	RSTB	I	Reset signal, inverted polarity
1	22	AUX2	AT	Previously Rref input, analog I/O test pin, preferably left UNCONNECTED
24	19	XTLI	XI	Clock input, crystal connection input
23	18	XTLO	XO	crystal output, not used when clock supplied
3	2	SXP	AO	S-Bus positive transmitter output
4	3	SXN	AO	S-Bus negative transmitter output
26	20	SRN	AI	S-Bus balanced receiver input
27	21	SRP	AI	S-BUS balanced receiver input
10	8	DIN	I	Serial Data Input GCI
7	5	DOUT	O/ODP	Serial Data Output GCI, pull-up 3.5
8	6	DCLK	I(O)	Clock signal GCI bus, (Output TE mode)
9	7	DFR	I(O)	Frame signal GCI bus, (Output TE mode)
16	12	MOD2	I/S	Mode pin 2, \ to select NT/LT-S/LT-T/TE,
5	4	MOD1	I/S	Mode pin 1, > clock families on GCI
20	15	MOD0	I/S	Mode pin 0, / special features
14	11	XTR3	IO	Extra bidirectional pins, for special modes,
11	9	XTR2	IO	bus address selection or special extra
19	14	XTR1	IO	outputs
17	13	XTR0	IO/ODP	
21	16	SCLK	IO	Synchron. Clock (TE/LT-T), else strap/test
Extra pins for the 28 pin PLCC package				
28	-	VDD	P/S	Extra supply voltage +5V
25	-	AUX	P/S	Extra supply voltage, strapped at 0V
6	-	XTR4	IW/S	TX phase adjust strap see 5.4.3
12	-	AUX1	IO/ODP	Extra auxiliary in/out, generic use possible
18	-	AUX3	IO/ODP	Extra auxiliary in/out, generic use possible
15	-	AUX4	IO/ODP	Extra auxiliary in/out, generic use possible

see 4.11 & 7.7.4

The extra pins of the 28 pin package are not bonded in the 22 pin DIL: AUX and VDD (pins 22 and 28) are replaced by double bonding-wires to the VDD and VSS pins. The XTR4, AUX1, AUX3 and AUX4 have a weak internal pull-up resistor, because they are inputs, or are configurable as inputs. This avoids a floating bonding pad in the 22 pin package, which would cause unnecessary leakage currents on the input amplifier.

3.3 Input/Output Types in Function of the Modes

Table 3.2 : Input/Output types in function of the modes

	pos.	MOD2	MOD1	MOD0	AUX4	AUX3	XTR4 AUX1	SCLK	XTR3	XTR2	XTR1	XTR0	DOUT	DIN
BASIC	TE	0	0	0	o	od	iw	o	i	o	o	o	o	i
		0	0	1	o	od	iw	o	i	o	o	o	o	i
		0	1	0	o	od	iw	o	i	o	o	i	o	i*
	LT T	0	1	1	o	od	iw	o	s=1	s=TS	s=TS	s=TS	od	i
		0	1	1	o	od	iw	o	s=0	s=0	s=0	i	o	i*
	NT	1	1	1	o	od	iw	i	i	i	i	iodp	odp	i
	LT S	1	0	0	iodp	od	iw	s=0	i	s=TS	s=TS	s=TS	od	i
		1	1	0	iodp	od	iw	s=0	i	s=0	o	s=0	o	i*
		1	1	0	iodp	od	iw	s=0	i	o	o	s=1	o	i*
EXTENDED	TE	1	1	0	o	od	iw	s=1	i	o	o	o	od	i
	LT T	1	0	0	o	od	iw	s=1	o	s=TS	s=TS	s=TS	od	i
	LT S				iodp	od	iw		i				od	i
	NT	1	0	1	o	od	iw	i	i	i	i	iodp	odp	i
		1	1	0	o?	o?	i?	s=0	io?	s=1	io?	s=0	o?	i?
	TEST	0	1	1	o?	o?	i?	io?	s=0	s=1	s=x	io?	o?	i?
		0	1	1	o?	o?	i?	io?	s=0	s=0	s=1	io?	o?	i?
		MOD2	MOD1	MOD0	AUX4	AUX3	AUX1 XTR4	SCLK	XTR3	XTR2	XTR1	XTR0	DOUT	DIN

i = Input;
i = Input, remark on compatibility, see 3.6;*
iw = Input, weak pull-up internally, values see 3.6;
s = Input as Strap, fixed to 1 or 0;
o = Push-pull output, tristate possible;
od = Output with open drain, pull-up external;
odp = Output open drain, pull-up internal, NT, speed 256 kbit/s;
iodp = I/O bus open drain, pull-up internal, values see 3.6;
i? = Input, choice of type open, for test purposes;
o? = Output, choice of type open, for test purposes;

3.4 Values and Usage of the Pull-Up Devices

1) Pins Left Unbonded in the 22 Pin Package :

XTR4 is an input, left unbonded in the 22 pin package. To avoid a floating input, it has an on-chip pull-up resistor of nominally 100 kΩ.

AUX1, AUX3, AUX4 have a standard configuration shown in TABLE 3.3. They can also be reconfigured as generic inputs or as push-pull outputs, see 7.7.4. To avoid a floating input in the 22 pin package, they have an on-chip pull-up resistor of nominally 50 kΩ, which is compatible with the speed of the DE bus function (see 4.11, 4.12) of the AUX4 pin.

2) Other Pins :

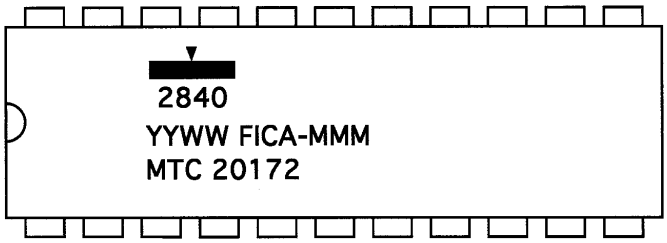
XTR0 pin serves as DE bus pin (see 4.11, 4.12) in certain modes. It has an internal pull-up of nominally 50kΩ in those modes.

DIN: In the MTC-20172 SIC, the DIN pin is a simple input.

DOUT: In the NT modes , the DOUT pin is an open drain with an integrated pull-up resistor of nominally 20 kΩ. This allows data rates of 256 kbit/s. Higher data-rates will require an additional external pull-up device to be used.

3.5 Device Marking

DIL



PLCC

2840	Manufacturers code
YYWW	Manufacturing date-code
MTC 20172	Product code
FICA	Manufacturers product code
MMM	Product mask revision code
LLLLLLLLL	Manufacturing lot number
AA	Assembly location code

4. General Functional Description

4.1 General Features

The main properties of the circuit are:

- Single Chip Transceiver on the 4 wire S-bus, single 5V supply;
- Handling of Basic Access at 144 kbit/s with 2B+D;
- Layer 1 functions of the CCITT I.430, including E- and D-channel access with priority in TE bus configuration;
- S-bus drivers with high impedance in power-off (no supply);
- Improved S-bus balanced receivers, compatible with the external unbalanced PCBA circuitry implemented in existing products;
- Handles attenuation on the S-bus up to 15 dB (CCITT minimum=7.5dB);
- Exceeds 1 km point-to-point and 200 m bus range;
- Has both fixed timing and adaptive timing as NT/LT-S;
- Can be used in LT-T mode, with clock wander up to 18 ms;
- Operating power consumption < 50 mW;
- Stand-by power < 1.5 mW;
- Dynamically configurable to the S- and the T-interface;
- S & Q bit channel on the S-bus, written/read via GCI-M-channel;
- Handles GCI, V*, IOM1™ and IOM2™ bus interfaces;
- Includes a maintenance M-channel for all GCI modes;
- Connectable to HDLC devices in TE/LT-T with access protocol;

4.2 Compatibility

The MTC-20172 SIC is a single component, which can cover all applications for an S-Bus device without HDLC.

It is pin-compatible with MIETEC MTC-2072 SIC and is functionally similar.

4.3 Improved Features

* The ternary S-bus receiver is balanced, backwards compatible with the unbalanced Mietec MTC-2072 SIC, and with improved line-length and noise immunity.

* The ternary S-bus drivers require a series resistance, and have a high impedance when SIC power is off. Pulse overshoots are limited on-chip, see 5.2.

* The serial bus is multifunctional, supporting V*, GCI, IOM1™ and IOM2™ timing, selected with straps or automatically recognized.

* The GCI C/I-channel is multifunctional, supporting the older V* version of the Mietec MTC-2072 SIC, or the GCI version of newer devices.

* GCI M-channel is added, e.g. for reading/writing the S/Q channel, and to select modes via software, overriding the strapped modes or the default state after reset; (new feature).

* An ECHO bus allows pooling of HDLC receivers on linecards (new feature).

* Multiframing on the S-bus is implemented (new feature).

4.4 Overview of the Use of the MTC-20172 SIC in an ISDN System

See Figure 4.1

The MTC-20172 SIC circuit is part of the TE, the NT1, the NT2 at the S- and the T-interface side. It can be used in 4 different positions:

1) NT mode: In the NT1 as master of the S-interface towards terminal equipment, or as master of the T-interface, towards the NT2.

2) TE mode: at the terminal equipment (TE) side linking the TE to S-interface in the direction of the NT1 or NT2.

3) LT-S mode: Inside the NT2 (e.g. a PABX) at the S-interface, which is equivalent to the master position in the NT1.

4) LT-T mode: Inside the NT2 (e.g. a PABX) at the T-interface, which is equivalent to the terminal position on the S-interface.

The MTC-20172 SIC allows the connection of terminals to this interface by performing all layer 1 functions.
Note that in PABX/NT2 applications the MTC-20172 SIC is configurable as linked to either the S- or the T-interface, while linked to the same internal GCI bus.

4.5 General Description of the S-Bus Interface

The MTC-20172 SIC can be used on the S-bus configured as a point-to-point connection or as a passive bus.

The bus connection can handle up to 8 terminals. It is either a short bus with the terminals dispersed over a length of 200m, or an extended bus with a cluster of terminals within a 25 m range.

The chip handles full-duplex transmission of two B-channels (64 kbit/s each) and one D-channel (16 kbit/s). It handles also the echo E-channel, the multiframing S and Q bits, ...

The MTC-20172 SIC contains all circuit parts necessary for the adaption of the S-interface, especially transmitter and receiver stages.

- S-bus outputs are balanced, allowing bus operation;
- S-bus inputs are balanced, compatible with the Mietec MTC-2072 SIC and other industry standart devices;
- Out-of-band noise is filtered;
- RX has AGC and an adaptive threshold, and corrects long-line distortion by optimizing the sample moment.
- NT/LT-T receiver bus type is selectable: Short bus with fixed timing, or adaptive timing for extended bus or point-to-point.

The S-bus transceiver stages must be connected to the bus via external interface circuitry (2:1 transformer) and protection against electrical overstress due to foreign voltages. See appendix A with application note.
When the MTC-20172 SIC is in an unpowered state (supply voltage = 0 V) the S-bus transmitter is high ohmic (see CCITT I.430 8.5.1.2).

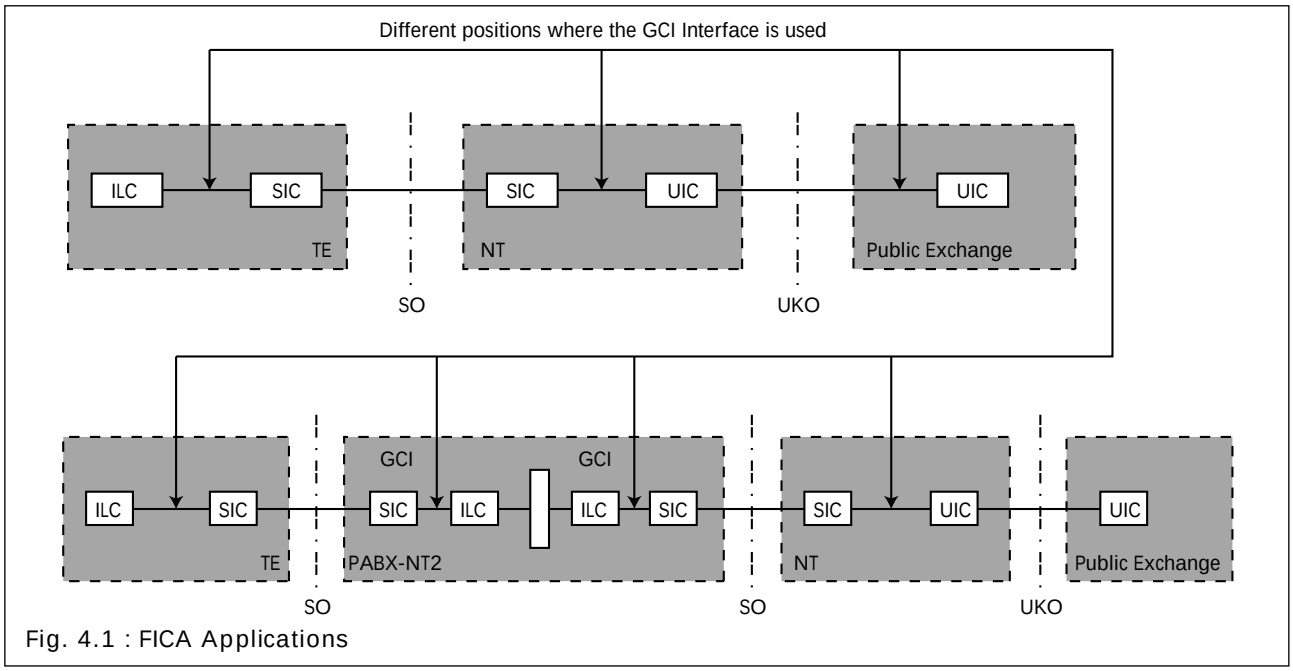


Fig. 4.1 : FICA Applications

This is needed in LT-T and TE applications, when multiple S-devices are sourcing on the same S-bus (short passive or extended bus).
In TE/LT-T, the S-bus transceiver provides the D-channel access protocol, in collaboration with an intelligent HDLC transmitter at the GCI bus side.

For details, please refer to chapter 5.

4.6 The GCI Interface

At the digital control interface, the MTC-20172 SIC is connected via a bidirectional serial interface - a digital bus called the General Circuit Interface (GCI), which is similar to the ISDN Oriented Modular (IOM™) interface.

This bus is logically organized as many parallel point-to-point links, each at 256 kbit/s.

The description of the GCI bus is available in separate documents. Details are provided in chapter 6.

4.6.1 The Physical Organization of the GCI Bus

The bus has a clock and a frame signal for timing, and two data lines (one for each direction).

In the TE mode, the clock and frame are generated by the MTC-20172 SIC. Then the timing is slaved to the S-bus and the network.

In the LT-T, the LT-S or the NT mode, the MTC-20172 SIC receives timing from the GCI interface.

In the LT-T, the MTC-20172 SIC must handle jitter, wander and slip between the GCI timing and the received S-bus clock.

The actual timing and speed of these 4 signals exists in several flavours and variants. The MTC-20172 SIC performs all the different timing variants of the V*, IOM1™ and IOM2™.

4.6.2 General Content of the GCI Bus

The GCI interface is organized with 4 channels at 64 kbit/s: B1, B2, M (Maintenance or Monitor), and B1* channel; Figure 4.2.

The B1 and B2 channels are transparent, switched at 64 kbit/s.

In ISDN applications, the B1* channel contains two D-channel bits, a 4 bits C/I 'command/indication' channel with the commands (towards MTC-20172 SIC) or the indications (from MTC-20172 SIC), and two extra bits (MR and MX) to control the M-channel. For details, please see chapter 6.

The D-channel contains HDLC-formatted messages. It is transported transparently (NT) or terminated by an HDLC transceiver (LT-S/LT-T/TE). In the TE/LT-T, a D-channel access protocol exists for the S-bus, which is controlled by the MTC-20172 SIC, and responded to by the HDLC transmitter. Via the command/indication (C/I) channel, commands to and status indications from the MTC-20172 SIC are exchanged with a control element (usually, a µ-controller) or with an other uplink or downlink ISDN circuit. Commands and indications are debounced to avoid erroneous behaviour.

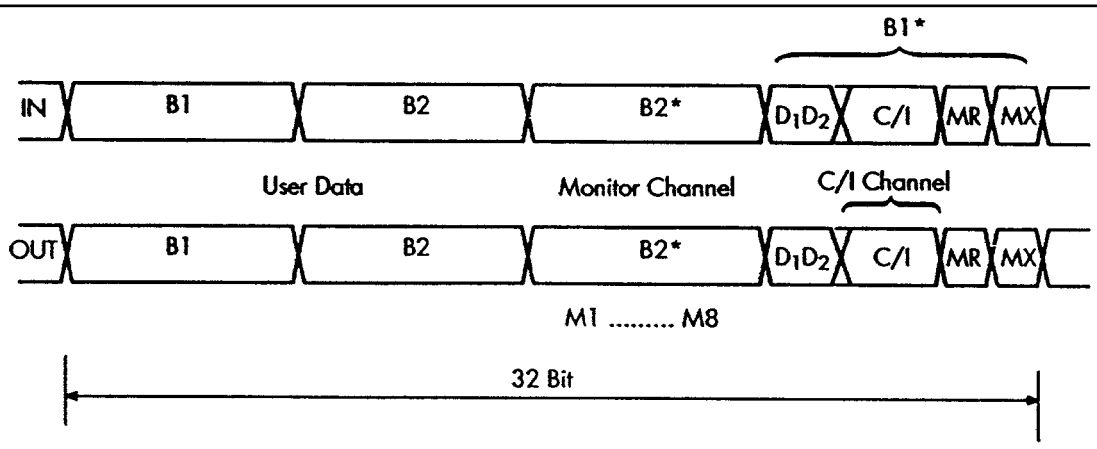


Fig. 4.2 : Frame Structure GCI

The M channel is a 64 kbit/s channel. It has a byte oriented structure, and the content is indicated and acknowledged with the MR and MX bits - the two last bits in the B1* channel. The content of the channel is used to write and read the internal MTC-20172 SIC registers. Its use is optional in the MTC-20172 SIC.

4.6.3 Power-down on GCI

For maximal power saving, the GCI bus can be halted completely and reactivated asynchronously from either side of the bus.

Section 4.9 gives a general description of the power-down features of the MTC-20172 SIC.

Chapter 6 gives the detailed behaviour.

4.7 GCI Clock-Synchronization in the ISDN Environment

In general, the downstream devices are slaved to the upstream devices.

Upstream MTC-20172 SIC (NT/LT-S):

A MTC-20172 SIC in the NT/LT-S position is master of the S-bus, and can sample the received (upstream) S-bus frames with a receive clock at exactly the transmitted frequency, but with an unknown phase.

In the NT/LT-S mode the MTC-20172 SIC receives the GCI timing, and must derive the 192 kHz S-bus bit-clock from it. As the GCI timing is not necessarily a multiple of 192 kHz, the MTC-20172 SIC generates a 192 kHz TX and RX clock from a crystal or from a clock input at 7680 kHz (±100 ppm). The 192 kHz clock is not a pure division by 40 of the crystal frequency, but is locked to the 8 kHz frame signal of the GCI interface. This is a DPLL action, where the 192 kHz clock period can be adjusted by ± 1 1/40 every 250 µs. Note that jitter on the 192 kbit S-bus signals is a combination of the jitter on the 7680 kHz before the DPLL and the effects of the DPLL locking to the GCI 8 kHz frame.

The S-bus RX clock in fixed timing (short passive bus) is derived from the same crystal, with the same frequency correction as the transmit clock but with a phase offset. The corrections of 1/40 of a bit period are used in an open loop mode here.
The S-bus RX clock in adaptive timing (extended bus, point-to-point) is also derived from the same crystal. However, the receiver must optimize the symbol sampling moment. This is an extra phase correction, which tracks wander and jitter of the received data.

The receiver tracks the RX data by locking on the F/L transitions.
Note: The timing stays identical for an internal analog loop from TX to RX, because then the MTC-20172 SIC uses adaptive RX timing as well. Even an external S-bus loop can be applied, provided that the receiver does NOT work with fixed RX timing.

Conclusion: in NT/LT-s, the MTC-20172 SIC has 3 different clocks, which are locked in frequency, but with unknown phase relation. Because the clocks are derived via PLL and DPLL blocks, the phase relation is not constant, but has some jitter and wander.

Downstream MTC-20172 SIC (TE):

In the TE mode, the timing is slaved to the S-bus and the upstream network. The MTC-20172 SIC generates a 192 kHz RX sampling clock from a crystal or from a clock input at 7680 kHz 100 ppm. This 192 kHz is locked to the 4 kHz frame signal of the S-bus. This DPLL action adjusts the 192 kHz clock period 1 1/40 every 250 µs.

The GCI clock and frame are generated by the MTC-20172 SIC, derived from the received S-bus timing. The transmit clock is also in fixed relation to the receive timing. To correct for external delays, the phase of the TX clock is adjustable, see section 5.4.3.

Conclusion: in TE mode the MTC-20172 SIC has all clocks locked to the 192 kHz RX S-bus data, with a fixed deterministic phase relation, except when loops are applied as explained below.

Downstream MTC-20172 SIC (TE) in analog loop:

When the downstream MTC-20172 SIC is looped (analog internal loop, not transparent) the linking and phase relation of the different clocks is completely different. The MTC-20172 SIC uses its local crystal as master clock and derives the S-bus TX and RX clock and GCI timing. The S-bus transceiver behaves as an upstream device. However, it monitors the RX signals to activate if desired.

Moreover, the loop is not transparent, i.e. no signal is sent to the actual S-bus.

Downstream MTC-20172 SIC (LT-T):

In the LT-T, the S-bus and the GCI timing are both enforced on the MTC-20172 SIC. They are not necessarily synchronized or even locked.

To allow the GCI clock to be synchronized on the S-bus clock, the MTC-20172 SIC has a dedicated clock output, called CP or SCLK, locked to the S-bus clock (see 4.11

and 4.12). This signal can be used in the PABX/NT2 system to lock the GCI timing to the ISDN. Once this synchronization (external to the MTC-20172 SIC) is active, the S-bus clock and the GCI timing will only wander and jitter. MTC-20172 SIC will accept wander of 18 µs.

Conclusion: In the LT-T, the S-bus receiver and transmitter timing are slaved to the S-bus and the upstream network, as in the TE mode. To accept wander of 18 µs, the MTC-20172 SIC has a long FIFO buffer between the GCI and S-bus side. If both clocks have different frequencies, the MTC-20172 SIC handles slips. (Details in 6.5.4).

Downstream MTC-20172 SIC (LT-T) in analog loop:

When the downstream MTC-20172 SIC is looped (analog internal loop, not transparent), the linking and phase relation of the different clocks is completely different. The MTC-20172 SIC uses the GCI timing as master, locks X-tal to the GCI frame, and derives the S-bus TX and RX clock from the crystal. The clock relationships inside the MTC-20172 SIC in LT-T position during the analog loop is identical to the LT-S device. However, it monitors the RX signals to activate if desired. Moreover, the loop is not transparent, i.e. no signal is sent to the actual T-interface.

4.8 Clock Speed

The master clock runs at 7680 kHz, ±100 PPM.

Internally, the S-bus transceiver part runs at 192 kHz. This is derived from the master clock, but locked to the ISDN network clock with a phase locked loop, adjusting one 7 MHz period every 250 µs. The ISDN network clock is sent downstream via the S-bus or the GCI interface.

The GCI part runs at the clock speed of its interface, which is minimally 512 kHz.

4.9 Power Saving / Deactivation of MTC-20172 SIC

The MTC-20172 SIC is controlled via the GCI interface. This interface is designed to be shut down and consequently reactivated in TE and NT modes. Shutting the bus down is commanded by the controller on the bus. Once the command is acknowledged, a fixed procedure is used to halt the clock (either by MTC-20172 SIC in TE, or by the controller in NT). Reactivating the bus can be done by the MTC-20172 SIC or the controller. Details are given in section 6.2.

When the GCI bus is going to be shut down, the S-bus transceiver is put to idle also. The S-bus transceiver enables an asynchronous signal detector, which can reactivate the MTC-20172 SIC on receipt of INFO via the S-bus. The MTC-20172 SIC then shuts down the internal 7 MHz clock distribution, and also the crystal output. If the clock is external, it may be also be put to idle, after the GCI bus is idle.

The MTC-20172 SIC can receive activation via the S-bus during the process of shut down via the GCI bus.

4.10 MTC-20172 SIC Activation

Activation of the MTC-20172 SIC depends on the position and mode.

4.10.1 MTC-20172 SIC Activation in NT Mode

Activation through the S-bus will be seen by the signal detector. The MTC-20172 SIC does not need crystal input or GCI clock to activate the GCI interface, which it does by asynchronously pulling the data line low. The master on the bus answers with GCI clock and frame, followed by commands via the C/I channel. The bus master also delivers the crystal frequency if it is generated externally to MTC-20172 SIC, simultaneously with GCI activation.

Activation through the GCI bus consists of clock and frame delivery, followed by commands via the C/I channel. MTC-20172 SIC will activate the S-bus transceiver according to the commands, including the crystal oscillator. If the master clock is generated externally it must be delivered to MTC-20172 SIC. Note that the internal clock distribution to the S-transceiver section is delayed for 2 ms (using the GCI frame clock), to allow the crystal clock to stabilize.

4.10.2 MTC-20172 SIC Activation in TE Mode

Activation through the S-bus is possible. The signal detector enables the crystal, the GCI clock and frame is activated, the receiver hunts for synchronization, indications and commands are exchanged via the C/I channel and the MTC-20172 SIC awaits further commands.

On activation through the GCI bus, the controller pulls the data line low (timing request). The MTC-20172 SIC enables clock and frame, and C/I codes are exchanged between the MTC-20172 SIC and the controller.

One major difficulty exists: Once the MTC-20172 SIC has acquired synchronization on the downlink data, the GCI frame must be adjusted to the received frames. This is needed to minimize transport delays of the B-channels. There is an optimal fixed relation between the received S-bus frame and the GCI frame, see 5.5.2.

The locking of the GCI frame to the S-bus frame causes a jump of the GCI frame pulse. To limit the number of phase jumps, the MTC-20172 SIC only adjusts the free-running GCI pulse when full synchronization on the S-bus frames is acquired.

4.10.3 MTC-20172 SIC Activation in LT/S and LT/T Modes

In this case, the GCI bus cannot be shut down.

The GCI clock and frame run continuously, but the MTC-20172 SIC can be forced in a low power state via the dedicated command. This command deactivates the S-bus transceiver. The crystal oscillator and the internal clock distribution stay enabled. The asynchronous signal detector is the only active part in the S-bus transceiver, the GCI part will react on new C/I channel commands, but runs no other activity internally.

4.10.4 Crystal Oscillator Operation

In the LT-T/LT-S modes, the crystal oscillator is permanently on, together with the clock distribution.

In the NT mode, the crystal oscillator is OFF during the power-down state, and the crystal clock distribution at wake-up is delayed after activation by 2 ms, by using the GCI frame clock.

In the TE-mode, the crystal will be shut down in the power-down state, except when the clock signals are requested to stay active via the ENCK- pin, see 4.12.

4.11 Modes of Operation

The TABLE 4.1 shows all Basic and Extended modes, as they are implemented in the MTC-20172 SIC.

The mode is determined by the state of the MOD2-0, XTR0-4, SCLK pins, as shown in Table 4.2.

The range of the DCLK clock is extended to any allowed GCI value, i.e. any multiple of 16 kHz above 512 kHz. The AUX1-4 pins offer extra input and output signals, as explained in 4.12.

Table 4.1.a: Basic modes of operation with the MTC-20172 SIC

APPLICATION									
	TE	TE	TE	LT-T	LT-T	NT	LT-S	LT-S	LT-S
Operation of IOM interface	Inverted Mode	Inverted Mode	V* Mode	GCI Mode or Inverted Mode#	V* Mode	V* Mode	GCI Mode or Inverted Mode#	V* Mode	V* Mode
MOD2 MOD1 MOD0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	o: 512kHz*	o: 512kHz*	o: 512kHz*	i: IOM	i: V*	i: V*	i: V*	i: V*	i: V*
DFR	o: 8 kHz*	o: 8 kHz*	o: 8 kHz*	i: 8 kHz	i: 8 kHz	i: 8 kHz	i: 8 kHz	i: 8 kHz	i: 8 kHz
SCLK (CP)	o:* 1536kHz	o:* 1536kHz	o: 512kHz*	o: 512kHz*	o: 512kHz*	i: /SCZ	i: fixed at 0	i: fixed at 0	i: fixed at 0
XTR3 (X3)	i: $\overline{\text{ENCK}}$	i: $\overline{\text{ENCK}}$	i: $\overline{\text{ENCK}}$	i: fixed at 1	i: fixed at 0	i: BUS	i: BUS	i: BUS	i: BUS
XTR2 (X2)	o: 2560kHz	o: 1280kHz	o: ECHO	i: TS2	i: fixed at 0	i: /SSZ	i: TS2	i: fixed at 0	o: 192kHz*
XTR1 (X1)	o: 3840kHz	o: 3840kHz	o: 3840kHz	i: TS1	i: fixed at 0	i: DEX	i: TS1	o: 7680kHz	o: 7680kHz
XTR0 (X0)	o: RDY	o: RDY	i: CON	i: TS0	i: CON	i/o: DE	i: TS0	i: fixed at 0	i: fixed at 1
AUX4	o:	o:	o: RDY	o: RDY	o: RDY	o:	i/o: DE	i/o: DE	i/o: DE
AUX3	o: BER	o: BER	o: BER	o: BER	o: BER	o: BER	o: BER	o: BER	o: BER
AUX2	i:	i:	i:	i:	i:	i:	i:	i:	i:
XTR4	i: X4	i: X4	i: X4	i: X4	i: X4	i: X4	i: X4	i: X4	i: X4
AUX1	i:	i:	i:	i:	i:	i: MFD	i: DEX	i: DEX	i: DEX

**: Indicates signals synchronized with the So-Interface*
#: Automatic selection between inverted and GCI mode
o: = output
i: = input

Table 4.1.b : Extended modes of operation of MTC-20172 SIC

	APPLICATION			
	TE	LT-T	LT-S	NT
Operation of GCI interface	GCI Mode	GCI or Inverted#	GCI Inverted#	GCI Mode or Inverted Mode#
		Submodes selected in SW		
MOD2 MOD1 MOD0	1 1 0	1 0 0		1 0 1
DCLK	o: * 1536kHz	i : V*	i : V*	i: V*
DFR	o: 8kHz*	i: 8 kHz	i: 8 kHz	i: 8 kHz
SCLK (CP)	i: fixed at 1	i: fixed at 1		i: $\overline{SSZ}$
XTR3) (X3)	i: $\overline{ENCK}$	o: * 1536kHz	i: BUS	i: BUS:
XTR2 (X2)	o: * 768kHz	i: TS2		i: $\overline{SSZ}$
XTR1 (X1)	o: PCK 32kHz*	i: TS1		i: DEX
XTR0 (X0)	o: RDY	i: TS0		i/o: DE
AUX4	o:	o: RDY	i/o: DE	o:
AUX3	o: BER	o: BER	o: BER	o: BER
AUX2	i:	i:	i:	i:
XTR4	i: X4	i: X4	i: X4	i: X4
AUX1	i:	i:	i: DEX	i: MFD

**: Indicates signals synchronized with the So-Interface*
#: Automatic selection between inverted and V mode*

Table 4.2 : Basic and Extended mode-selection pins in MTC-20172 SIC

	pos.	bus type	MOD2	MOD1	MOD0	SCLK	XTR3	XTR2	XTR1	XTR0
BASIC	TE	inverted	0	0	0					
		inverted	0	0	1					
		V*	0	1	0					
	LT-T	GCI / inverted	0	1	1		1	TS2	TS1	TS0
		V*	0	1	1		0	0	0	
	NT	V*	1	1	1					
	LT-S	GCI / inverted	1	0	0	0		TS2	TS1	TS0
		V*	1	1	0	0		0		0
		V*	1	1	0	0				1
EXTENDED	TE	GCI	1	1	0	1				
	LT-T LT-S	GCI / inverted	1	0	0	1		TS2	TS1	TS0
	NT	GCI / inverted	1	0	1					

GCI / inverted : Multiplexed mode, with multiple GCI channels; automatic type recognition, using frame signal; automatic recognition of clock frequency.

4.12 Functional Description of the Special Signals

The XTRi and AUXi pins have different functions depending on the modes, as described in the previous paragraph and TABLE 4.1.

In Alphabetical Order

BER : Bit Error Rate: each excessive violation seen during the S frame between position 14 and 48 indicates a link transmission problem, except in uplink frames during multiframing (see 5.1.7). Each error forces this BER output low for one S-bus bit period. All BER outputs can be tied to a single bus; see also 5.10.

BUS : Bus type configuration, "1" = short bus with fixed timing, "0" adaptive timing for extended bus or point-to-point (NT/LT-S), overridable via the GCI M-channel. It is preferable to tie the BUS strap to the fixed voltage via a resistor, because this pin is also used as the CP signal output in the extended modes.

CEB : Other name for the DE signal.

CON : Indicates connection to the S-bus, enables INFO1 (TE and LT-T). INFO3 transmission in response of INFO2 or INFO4, is allowed without CON after synchronization. This signal in NOT overridable via the GCI M-channel.

CP : In the TE and LT-T modes, the CP pin is a clock locked to the S-bus data frames, see TABLE 4.1. This clock can be disabled via the monitor channel, see 7.7.3. This simplifies clock selection logic which must route only one CP clock signal out of many active T-interfaces, to the PABX or NT2 clock system. In the extended modes the synchronized "CP" clock signal is put on pin XTR3. Details on all available clocks and their timing in 9.6.

DE : D-channel echo bus (I/O), enabled by DEX or monitor command; (NT and LT-S). All synchronized S-bus transceivers are delivering the received upstream D bits on this bus and sample the common echo bit via this bus. See also 5.6.

DEX : D-channel echo bus enable (NT star configuration, LT-S HDLC pooling configuration) See also 5.6. Strap, 1=enable, 0=disable; combined with DEX register bit via the GCI M-channel, see 7.7.3.

ECHO : This output reproduces the E-bits in the TE-mode, from the received S-bus data. These bits are synchronized with the D channel on the GCI data line. Used by intelligent HDLC controller, to start and abort a message; see 5.7.8.

ENCK- : When at 0, this input enables the crystal, the GCI bus timing and all other related clocks always (TE mode). When C/I command code goes to idle (1111) the bus is not shut down. Related to detailed GCI power-down, 6.2.

LP- : Loss of Power input and output; these signals are NOT IMPLEMENTED in the MTC-20172 SIC.

MFD : Multiframe Disable when 1, internal weak pull-up, allows multiframing via strap or digital control signal; overridable via monitor channel; see 5.9.2.

RDY : D-channel access protocol status in bus (TE and LT-T), signals the anticipated availability of the D-channel to an intelligent HDLC transmitter. "1" = clear to send; "0" = occupied or busy. See also 5.7.3.

SCZ- : Send Continuous binary zeros, inverted polarity; NT mode only, forces a test signal on the S-bus output, overrides C/I, activates the GCI bus to ensure crystal input active.

SSZ- : Send single zeros, inverted polarity; NT mode only, forces a test signal on the S-bus output, overrides C/I commands, activates the GCI bus to ensure crystal input active.

TM1- : Test Mode 1 (inverted) = SSZ-, send single zeros.

TM2- : Test Mode 2 (inverted) = SCZ-, send continuous zeros.

TS2-0 : Time slot number on the GCI bus (LT modes, mux'ed), represent a binary number 0 to 7; straps.

X4 : Extra strap input.

OTHER SIGNALS, non-digital, not dependent on the mode:

AUX : Strap/extra power supply, see 3.4.

Rref : Not used; position used as test for production test.

5. Detailed Operational Description of The S-Bus Interface

Introduction

An overview of the functional environment is given in chapter 4. In this chapter we give external and internal operational details of the S-bus interface. Detailed interface timing and electrical specifications are given in chapter 9.

5.1 General Characteristics

The S-interface realizes full-duplex transmission of two B-channels (64 kbit/s each) and one D-channel (16 kbit/s). In addition, the S-interface allows controlled access to the common D-channel and the activation/deactivation of each connected device.

5.1.1 Transmission Rate

The nominal transmission rate is 192 kbit/s in each direction. There is no requirement for special bit sequences in the B-channels.

5.1.2 Frame Structure

Data is transmitted within a frame of 48 bits in each direction. The nominal frame period is 250 µs, which gives a frequency of 4 kHz. The frame structure is not dependant on 'bus' or 'point-to-point' configuration. The frame structure is shown in Figure 5.1.

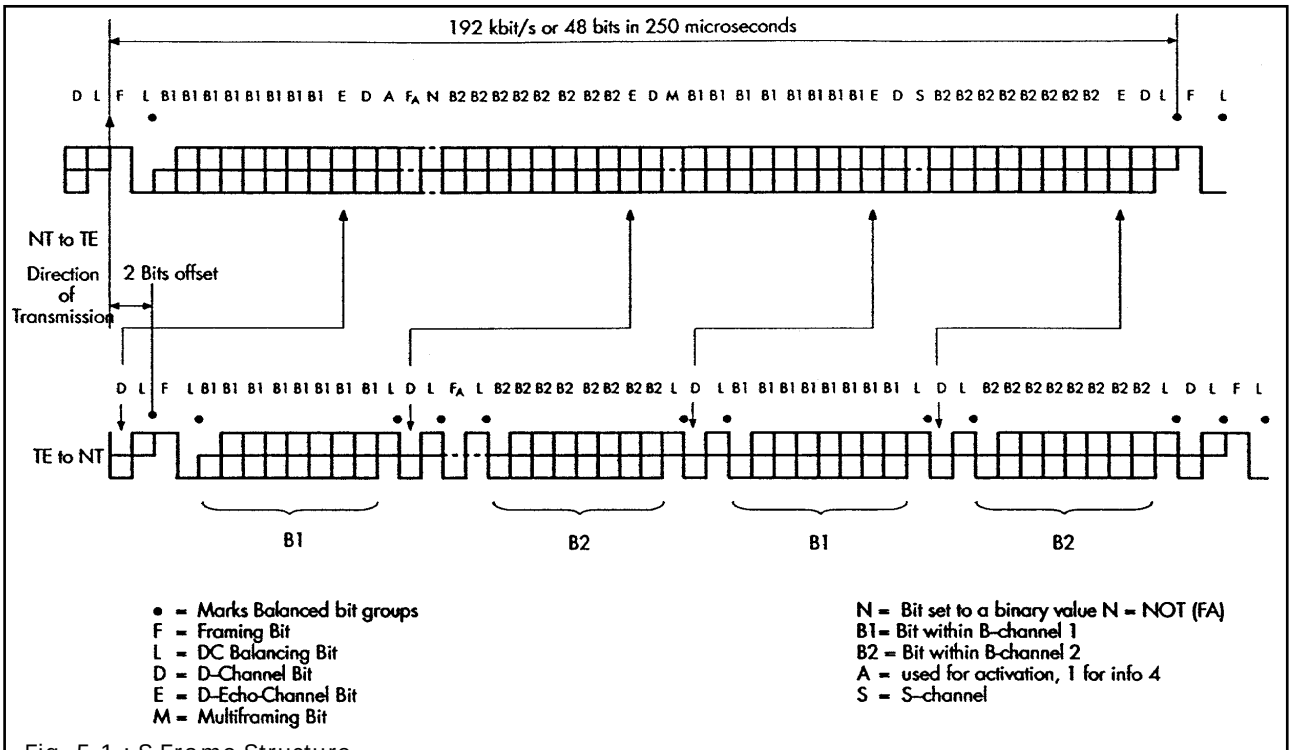


Fig. 5.1 : S Frame Structure

5.1.3 AMI S-bus Coding (general in RX and TX)

For both directions, a pseudo-ternary coding (AMI) is used. A binary '1' (high level logic) is coded as 'no signal' whereas a binary '0' state is represented by alternating positive and negative pulses (see Figure 5.2).

The polarity inversions, coupled with a minimal density of marks per frame, reduce the low frequency components of the signal. The 4 kHz frame always starts with a positive pulse (F-bit), followed by a negative balance bit L.

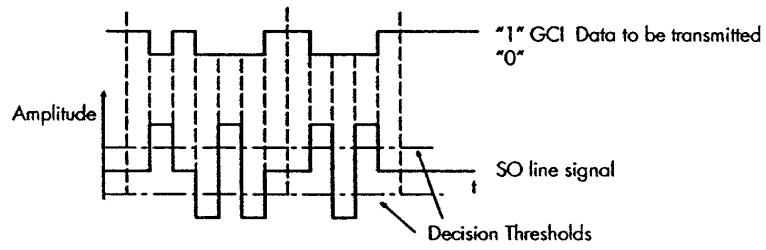


Fig. 5.2 : S Coding with AMI

5.1.4 Balance Bits

Inside the frame, several balance bits are present serving two purposes:

1) In both directions, they guarantee that the polarity of the first bit or F-bit is constant. They also increase the mark density on the link.

2) Moreover, in the uplink direction, the bits in the frame can be generated by different terminals. Therefore, the frame is subdivided into groups of bits, each sent by a single terminal, and terminated also with a balance bit. The first binary '0' of each group of bits (except for the framing signal) is coded as a negative pulse. The balance L-bit terminates those group with a positive mark if needed, to avoid violations of the mark inversion scheme. This allows the different B and D channel bits to be sent by different transmitters on a bus, because the AMI polarity is always fixed. In this way, no AMI violation can be caused by the multipoint nature of the BUS.

5.1.5 AMI Violations for Frame Synchronization

For synchronization purposes the AMI is violated twice per frame. A 48 bit frame always starts with a positive pulse (F-bit) followed by a negative balance bit L. The F-bit is a violation, because the last mark of the previous frame is positive also. The first binary '0' following a framing signal (F,L) is always negative, and is a second violation.

5.1.6 Frame Synchronization; Distance Rule

There are two AMI violations in the frame: The F-bit at the beginning is at a fixed position. The second violation must follow the F bit within 13 bit positions, because the frame contains an FA (auxiliary flag) at position 14, which is a binary 0, even if all other bits (2 to 13) are binary one.

After the FA, the next violation will be the F flag itself, at a distance much larger than 13 bit positions. This distance rule allows for fast and reliable frame flag detection

5.1.7 Frame Synchronization; Multiframing Exceptions

AMI violation delay in multiframing: At the TE/LT-T position, the received FA bit is occasionally a binary 1 in case of multiframing (see 5.9). However, the N bit at position 15 is a binary one, because it is the binary inverse of the FA (see 5.1.11.1). This guarantees a second violation within 14 positions after the F bit.

AMI violation exception in multiframing:

At the NT/LT-S position, the received FA bit is occasionally a binary 1 in case of multiframing. FA is followed by a balance bit L, which is then also at binary 1. If all B and D bits between F-L and FA-L are also at binary 1, then there is no second violation within the 14 positions. If the remaining bits (B and D channels) are also at 1 in the remainder of the 48 bit frame, then the second violation will be absent, and next F bit will not be a violation! This can delay the synchronization, and could trigger an INVALID loss of synchronization.

The delayed synchronization during multiframing is unavoidable.

To avoid an invalid loss of sync at the NT/LT-S when multiframing is on, all incorrect second violations (too late or missing) in the uplink direction are ignored if the FA bit was a binary 1 in the corresponding 48 bit frame in the downlink direction. Missing violations at the F bit position are ignored if the preceding 48 bit frame (downlink) had the FA bit at one.

5.1.8 Synchronization Principles, with Adaptive Bit-timing

1) The receiver first finds the AMI violations by oversampling.

2) Immediate bit-synchronization is given by the F-L transition.

3) The distance rule of the next violation within 14 positions is used to validate the F-bit.

4) Frame synchronization is acquired after 3 correct frames, with a correct F-bit violation and a second one within 14 bit positions.

5) The F-L transition of each frame locks a DPLL based on the crystal frequency in the TE/LT-T case. In the NT/LT-S, the F-L transition determines the adaptive bit sampling.

6a) At TE/LT-T, loss of sync after two frames not having F violation, or the second violation not following the distance rule at 14 bit. After the loss of sync, the TE/LT-T sends idle (INFO0, uplink).

6b) At NT/LT-S, loss of sync after two frames not having F violation, or second violation following the distance rule (at 14 bits), when no multiframing is active. The downlink signal stays active, but changes automatically from INFO4 to INFO2. In the case of multiframing, the missing second violation within the 14 bit distance, or the missing violation at the next F bit (for uplink frames with the corresponding downlink FA bit at binary 1), is ignored.

5.1.9 Synchronization Principles, Fixed Bus Timing at NT/LT-S

On a short passive bus, the position of the bit sampling can be fixed. The points 3), 4) and 6b) of the previous paragraph are executed. No oversampling is done, no DPLL action is needed to track the F-L edge. Note that the fixed timing is changed automatically to adaptive timing, when internal analog S-bus loops are requested. When EXTERNAL S-bus loops are used (e.g. for production test), only adaptive timing is suitable.

5.1.10 Pulse Polarity in the S-bus Frame

The receiver is polarity independent.

The transmitter in NT and LT-S mode has no polarity requirements. The transmitter in TE/LT-T must have a fixed polarity to allow a bus operation with multiple sources. See also 5.2.1.

5.1.11 Transmitted Frames:

Depending on the activation state of the interface, the MTC-20172 SIC can transmit different signals called INFO 0, 1, 2, 3, and 4. Moreover, two test signals are defined

5.1.11.1 Details on Downlink Frames: Network to Terminal

The downlink Frames transmitted by upstream devices contain an E-bit. During INFO4, the E-bit is the echoed D-channel bit received from the downstream devices, see 5.6. This D-echo-channel is used for the D-channel access procedure, see 5.7.

Two L-bits are used for DC-balancing, after the F-bit and the last bit the frame. In downlink direction some special bits are used, see Figure 5.1:

- A-bit used for activation (A=1 for INFO4, A=0 for INFO2);
- S-bit coded as binary zero, if no multiframing active;
- N-bit coded as N = .NOT. FA (applies to INFO2 and INFO4);
- M-bit at binary zero, except when multiframing (5.9);
- FA-bit, additional flag (bin. zero), except when multiframe.

Without multiframing active, S, FA, M bits are binary zeros. Multiframing is allowed to be active during INFO2 and INFO4, and influences the S, FA, M bits as described under 5.9.

Signals from network to terminal		Signals from terminal to network	
INFO0	No signal, open circuit	INFO0	No signal, open circuit
INFO2	Frame with all bits of B, D, and E-Echo channels, and a bit at binary zero, FA, M, S, N and L bits six ONEs follow the coding rules of 5.1.11.1	INFO1	Continuous signal with the following pattern : positive zero, negative ZERO,
INFO4	Frame with operational data on B, D, and E-Echo channels. Bit A set to binary ONE. FA, M, S, N, L bits follow the coding rules rules of 5.1.11.1	INFO3	Synchronized frames with operational data on B, D channels. FA and L bits according to normal coding of 5.1.11.2
TEST1	Send Single Zeros (SSZ), AMI marks, 250 µs distance forced via pin (NT) or C/I	TEST1	Send Single Zeros (SSZ), AMI marks, 250 µs distance forced via pin (NT) or C/I
TEST2	Send Continuous Zeros (SCZ), alternating marks, marks forced via pin (NT) or C/I	TEST2	Send Continuous Zeros (SCZ),alternating forced via pin (NT) or C/I
The B-channel and D-channel are transparently transmitted on the S-bus. When idle, these channels are all binary 1.			

5.1.11.2 Uplink Frames: Terminal to Network

The INFO3 frame transmitted at terminal-side consists of several groups of bits, each of them DC-balanced by an adjacent symmetry-bit L.
See Figure 5.1.

The uplink D-channel requires an access protocol, detailed in 5.7.

Downlink multiframing influences the FA-bit in uplink (Q-channel): If the MTC-20172 SIC receives the FA-bit as binary 0 (electrical mark), it will always answers with binary 0. If the MTC-20172 SIC sees the FA-bit as binary 1 it answers with binary 1, when multiframing is not active.

When using multiframing the FA-bit is coded as described in section 5.9.

5.2 S-BUS Transmitter Analog Blocks

5.2.1 Polarity

The polarity is such that the F bit puts the SXP pin at a positive voltage relative to the SXN pin.

5.2.2 MTC-20172 SIC Drivers, External Transformer and Circuits.

In the TE/LT-T position, 8 S-transmitters must be able to send information simultaneously on the S-bus in uplink direction. For this reason the drivers are current limited voltage sources, with a minimal series resistance when the current limitation is not active.

The outputs are balanced. The pulse height is a linear function of the supply voltage. The pulse shape has 5% margin around the nominal height, when the MTC-20172 SIC supply voltage is nominal. When the supply voltage has a 5% range, the pulse will be within the 10% tolerance of the CCITT recommendations.
See Figures 5.3 and 5.4.

The drivers are high ohmic when transmitting a binary one, or when the chip is not powered.

Impedance:

The drivers are a low-ohmic voltage source, connected with a series resistance to a transformer with a 2:1 winding ratio. At the SIC side of the transformer, the 50Ω nominal impedance of the bus is seen as a 200Ω resistance. The nominal pulse on the transformer is 1.5 V, at 7.5 mA. The open circuit voltage is 2.1 V (140 % of 1.5 V). The total driving resistance of the SIC plus the external series resistor must be 80Ω. (See 5.2.4).

When the bus impedance is lower than the required 50Ω, e.g. when shorted or when drivers are driving opposite polarities, the output current when driving a binary 0 (electrical mark) is limited below 13 mA in absolute value.

Longitudinal signals, protection circuitry and further details under electrical characteristics, see 9.5 and 12

5.2.3 Ternary Drivers:

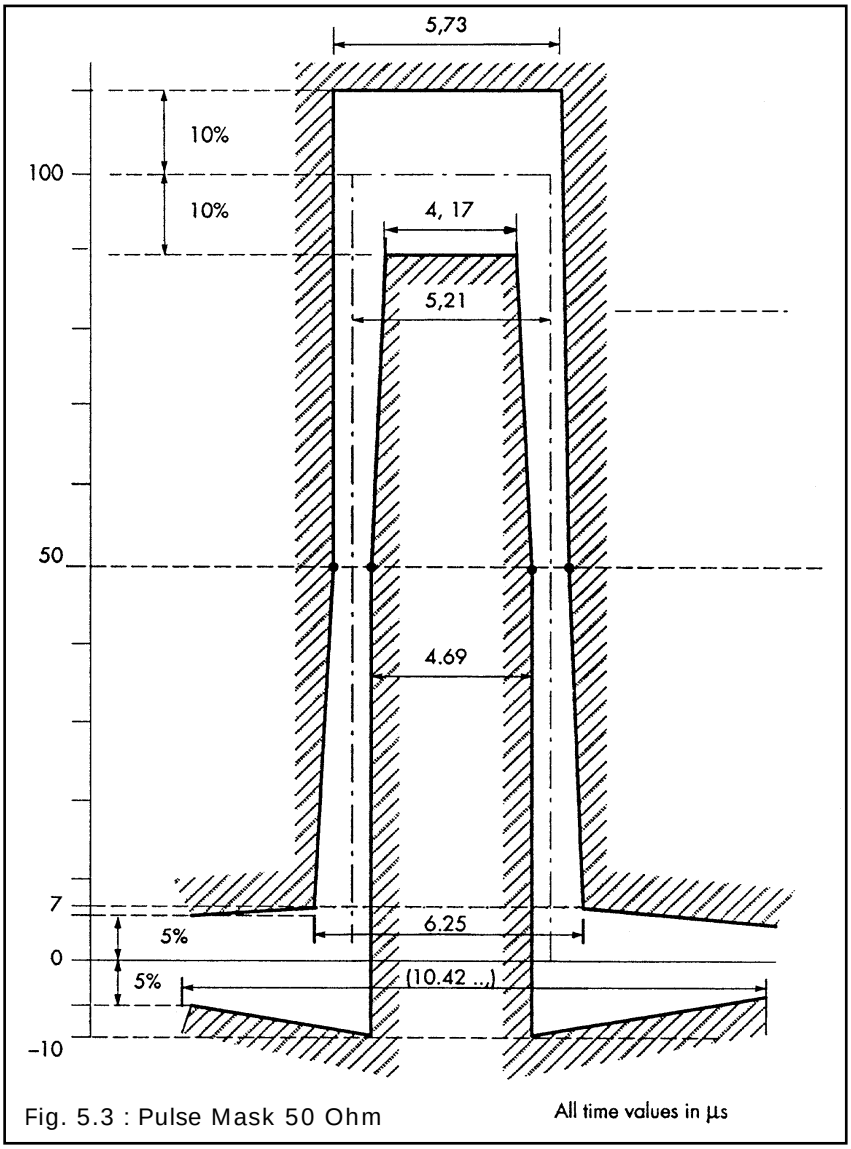


Fig. 5.3 : Pulse Mask 50 Ohm

High-Ohmic State when not Powered.

The S-bus drivers of the SIC will be in a high-ohmic state when not powered, i.e. when the bus is active, but the SIC is not powered. This is required to fulfil the CCITT requirements on output impedance in the TE (or LT-T) position, in parallel with other SICs. (This is achieved by using only n-type devices for the complete driver stage, because push-pull CMOS drivers always have parasitic diodes to both power supply and ground. These diodes limit the voltage between the SXP and SXN pins to less than 1.2V, by shorting the differential voltage via the power pins. On the S-bus, the amplitude of the voltage would drop to 0.6 volts, while the CCITT I.430, 8.5.1.2 requires currents below 0.6 mA when signals with peak amplitudes of 1.2 V are applied on the S-bus).

5.2.4 Ternary Driver: Compatibility and Evolution

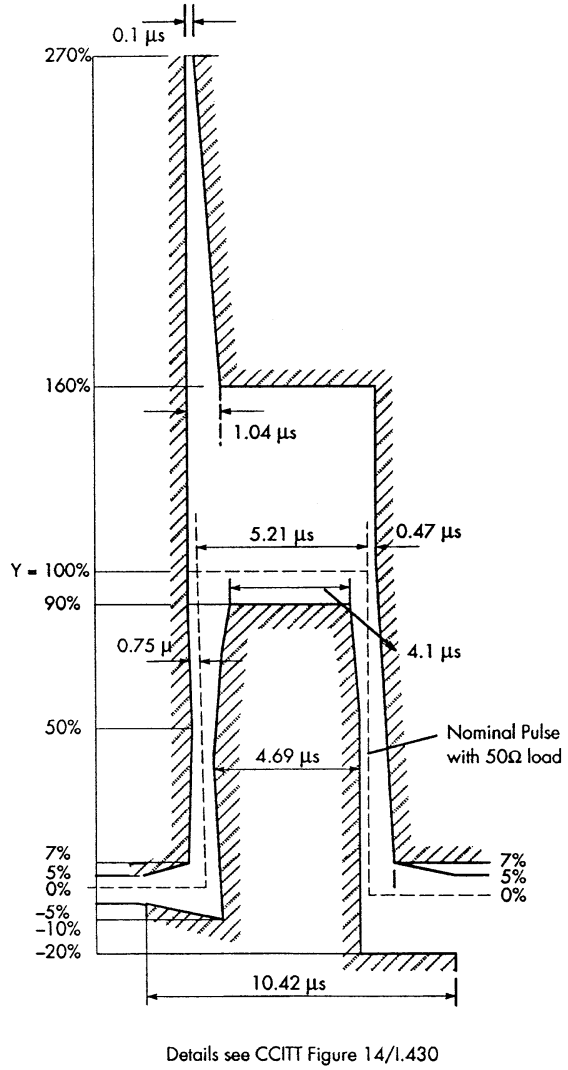
On the SIC, the ternary drivers require two series resistors of around 34Ω between with the balanced output drivers. The 34Ω includes the real part of the impedance of the sending transformer. When an MTC-2072 SIC is replaced by the MTC-20172 SIC, the extra resistors must be added to the PCB.

Originally the MTC-2072 SIC drivers were current sources, driving a known 7.5 mA in the transformer, with a simple voltage limitation. In the MTC-2072 SIC, a reference resistor (Rref) is used to generate the nominal 7.5 mA current.

The voltage drive with 80Ω in series limits overshoots on single pulses, compared to the older high-ohmic current drive. However, the peak-voltage on the bus goes to 140%, when multiple S components are driving the bus simultaneously.

Note also that the 80Ω series resistance could be considered necessary to fulfill the CCITT requirements on the driver output impedance when transmitting a zero, although the actual measurement technique specified by the CCITT is questionable, when the SIC drives the specified nominal 400Ω impedance. (CCITT I.430 8.5.1.2).

5.2.5 S-bus Transmitter Timing



Details see CCITT Figure 14/I.430

Fig. 5.4 : Pulse Mask 400 Ohm

and Framing; Jitter

The transmitter data are sent at 192 kHz. The 192 kHz is derived from the crystal frequency of 7 MHz, by division by 40. The transmitter framing is at 4 kHz. The timing is slaved to the downlink clocks, the 4 kHz S-bus frame is locked in phase to the available downlink framing, see 5.5.

5.2.5.1 Transmitter Timing and Framing at the NT/LT-S

With a DPLL, the 192 kHz clock is locked to the GCI interface at the NT/LT-S, by synchronizing the S-bus frame with the GCI frame. The DPLL locks the falling edge of the F/L frame signal on the GCI frame signal, see 5.5. Jitter will be according to the CCITT I.430 8.3.

5.2.5.2 Transmitter Timing and Framing at the TE/LT-T

The 192 kHz is locked, with a DPLL, to the downlink data. The transmit clock frame reference is derived from the RX F/L edge, as explained under 5.3.12.3. Jitter will be 2.5 % of a bit period when receiving a clean input signal. In the presence of noise and jitter on the downlink data, the uplink jitter will be larger. However, the TX clock is derived with a DPLL which can only adjust one 7 MHz period every S-bus frame, which limits jitter enhancement.

5.3 S-BUS Receiver: Analog Parts and Synchronization

The MTC-20172 SIC has an improved ternary receiver. It is fully balanced, to better reject longitudinal noise. It handles higher attenuations on the S-bus, with adaptive thresholds.

5.3.1 Transformer and Other External Devices.

The receiver is connected to the S-bus via a transformer with a 2:1 ratio, similar to the transmitter. Using a lower winding ratio reduces the useful signal sensitivity. Moreover, the bit detection thresholds will be not optimal, especially for the short bus applications. The input transformer (together with other filter elements) must also reject longitudinal noise signals, in order to fulfill symmetry requirements of CCITT's I.430 recommendation. Large common mode signals are not tolerated by the input stage of the MTC-20172 SIC. External series resistors are needed for minimal impedance, see 5.3.3. Moreover, external protection against foreign voltages is needed (see appendix A).

5.3.2 Ternary S-bus Receiver Polarity and Balanced Operation

The ternary S-bus receiver is polarity independent. It is fully balanced, which means that it can be connected to the balanced S-bus with a symmetrical transformer, with a grounded center tap at the S-bus side to better reject longitudinal noise. The balanced secondary is connected directly to the MTC-20172 SIC with 2 series resistors, as explained in 5.3.3.

The MTC-20172 SIC S-bus receiver is backwards compatible with the unbalanced ones (e.g. MTC-2072 SIC).

5.3.3 Ternary Receivers: Impedance While not Powered.

When the MTC-20172 SIC is under power, the balanced inputs are capacitive loads on the bus. However, in the TE (or LT-T) position, when the bus is active but the MTC-20172 SIC is not powered, a minimal input impedance is required by the CCITT I.430. With 1.2 V (peak) applied the current will be less than 0.6 mA.

Part of this current is drawn by the S-bus transformer with a parallel impedance of minimally 2.5 kΩ. The MTC-20172 SIC input structures present protection diodes to the power supply and ground (VDD and VSS pins). To guarantee a current below 0.6 mA external series resistors must be put between the MTC-20172 SIC receiver pins and the transformer. Note that these resistors also serve as input protection. Typically, 10 kΩ is needed in series (see appendix A).

5.3.4 Activity Detection:

When the device is in power-down state, a Line Signal Detector is enabled to detect the presence of incoming data. No clock must be present. The activated MTC-20172 SIC signals this via the GCI bus, see 6.2.

5.3.5 Sensitivity / AGC:

The receiver contains an AGC, which adjusts the gain of the received signal before synchronization, to optimize the detection of the frame violations.

After frame synchronization, the AGC slowly and continuously tracks the height of the F bit at the optimized sampling moment, to normalize the height of the rest of the frame and to improve the bit detection of the remainder of the frame. The AGC tracking is based on the comparison of the received F bit signal with two thresholds at 95 % and 105 % of the reference level. The range between the thresholds, where the AGC is stable, is larger than worse case AGC step to avoid continuous toggling of the gain (i.e. hysteresis).

The AGC uses the height of the F bit at the sampling moment to exclude the pulse overshoots which can exist on short passive buses, with reflections on high-ohmic cables.

The AGC reference level is put at 85% of the nominal pulse height, or -1.4 dB relative to the nominal signal. Stronger signals (above -1.4dB relative to nominal) are not amplified. This is necessary, so as to ignore signal overshoots caused by multiple drivers and by reflections on short buses, which can mask a weaker driver at -3.5 dB.

5.3.6 MTC-20172 SIC RX Signal Dynamics and Detection at TE/LT-T

At the TE/LT-T position, the signals are generated by a single source, and they are only distorted by reflections on the S-bus in the short passive bus situation. Those refections cause overshoots, which affect the AGC before synchronization is found. However, after synchronization, the slow AGC tracks the incoming signal at the optimal sampling moment of the F bit and the overshoots are ignored.

Signals above -1.4 dB relative to nominal are not amplified by the AGC. F/L bit detection is done at 33% of the nominal level. Detection thresholds for all other bits are at an optimal 42.5% of the nominal level, which is the ideal relative level of 50 % for all signals below -1.4dB, until the AGC gain saturates for signals below -15 dB.

5.3.7 MTC-20172 SIC RX Signal Dynamics at NT/LT-S

The incoming S-bus signals can be stronger than the nominal signals at the output of a single driver, because multiple drivers can enhance the F-bit up to 140%. The amplitude of the F-bit is therefore not a reliable indicator for the optimal detection levels of the individual bits of B and D channels.

On the short passive bus, the F-bit at around 140% of nominal can mask a distant driver at -3.5dB, according to CCITT I.430.

In the bus configuration, the ratio between individual B-channel bits and the F-bit ranges from 100% to 140%, depending on the number of drivers, with a worst case transmission cable loss of 3.8 dB or signal loss of 5.5dB.

In the point-to-point case, F and B-channel bits are equal, with losses limited to 7.5 dB by CCITT I.430, but accepted by MTC-20172 SIC up to 15dB.

5.3.8 MTC-20172 SIC RX Detection Levels at NT/LT-S

The detection levels and AGC setting is not influenced by the bus type selected at the NT (fixed timing or adaptive timing).

The presence of multiple drivers or a mix of weaker and stronger drivers is not recognized by the MTC-20172 SIC. However, the detection is improved by not applying any AGC when the F-bit is stronger that -1.4 dB relative to nominal, and by selecting 3 different absolute detection levels after the AGC stage, in function of the AGC gain.

5.3.9 Filtering:

The receiver filters the signal with a continuous-time filter. This is a first order filter, which is tuned to fix its 3 dB point at 192 kHz ±10 %. The delay of this filter is taken into account for the advance of the transmitter bit clock (TE/LT-T), see 5.3.12.3, or for the position of the fixed sampling moment on the short passive bus (NT/LT-S, fixed timing), see 5.3.10.

5.3.10 RX Frame Sync and Bit-sampling In NT/LT-S Short Bus Mode.

The bit-sampling moment is fixed, and coupled with the TX bit clock, which in turn is derived from the crystal clock, and locked to the GCI frame. The RX bit counters (giving the position of the uplink bits in the frame) are also locked to the downlink/TX bit counter. Uplink data are 2 counts late.

The fixed bit-sampling moment is advanced 5 periods of the 7 MHz clock, before the edges of the SIC transmit data stream. The advance is needed to allow an advance of 7% (or 3 periods) of the uplink data, allowed according to the CCITT to be sent by TE at zero distance, combined with a 1 period jump of the downlink data clock derived from the crystal.

This relationship is valid on the S-bus itself. Inside the SIC, the actual bit sampling is delayed to account for the nominal delay of the external transformer, the internal filters and driver delays. The total delay of the external devices is estimated at 100 ns, the internal delay is implementation related (see also 5.3.9).

Moreover, the sampling can be delayed extra by 5 periods of the 7 MHz clock via the XTR4 pin, and also via internal register programming; see 5.4.3.
The frame synchronization knows the F position, and applies the rules of 5.1.9 (i.e. without oversampling).

The NT/LT-S in fixed bus mode can be forced to loop the S-bus signals internally. Then SIC applies adaptive timing, to maximally test the device's functionality.

5.3.11 Frame Synchronization Details in Adaptive Timing.

The general synchronization rules are given under 5.1.8. They apply to NT/LT/TE.

During synchronization, the device oversamples the incoming bits with a fixed threshold, which is at 33 % of the nominal pulse height, with AGC active.

5.3.11.1 First Violation Detection

The oversampling is done at the 7 Mhz master clock, or a factor 40. A simple voting technique is used to detect a violation: The detector output increments a counter as long as the detected bits are marks of the same polarity or zeros. When a polarity change of the marks is seen, the counter is cleared. Whenever a sequence of more than 50 oversampled marks of the same polarity are seen, the receiver decides that a violation came in. The number 50 is not so large so as to allow synchronization on signals with flat edges.

After finding a single violation, the oversampling looks for the mark-to-zero and the subsequent zero-to-opposite-mark transition, which it then uses to estimate the actual F/L crossing; see 5.3.12 below.

5.3.11.2 Violation Validation

During the hunt for frame synchronization, the F/L transition forces the RX bit sampling clock and bit counter to a deterministic state, which is optimal; see 5.3.12 below.

The RX part now hunts for a next violation. In fact, the next mark must be a violation. This violation (polarity should be opposite, but this is ignored) must arrive before the counter indicates 14 received bits. If the second violation is found before 14 received bits, the F/L must be validated for 2 more consecutive frames.

In all following frames, the F/L transition is oversampled to lock the RX bit sampling clocks with DPLL movements of 1 period of 7 MHz.

If the F/L validation is not correct during the 2 subsequent frames, MTC-20172 SIC restarts the hunt of 5.3.11.1.

5.3.12 RX Bit-Synchronization in TE/LT-T and NT/LT-S Adaptive Bus

Bit-Synchronization is done only by detection of the F-L zero crossing. This is optimal for short buses and extended buses, where multiple signal sources are present, each with an independent bit timing. Only the F/L is a "stable" combination of all electrical drivers on the bus. For long point-to-point links, the same technique is used.

Each time the bit counters indicate the reception of F/L, the RX part oversamples the transition at 7 MHz.

The F/L crossing is used for several purposes:

1) It gives an immediate estimate of the RX data optimal sampling moment, after a first violation is found, via oversampling. (explained in 5.3.12.1)

2) It indicates how to correct the RX 192 kHz sampling clock each frame by one 7 MHz period; (DPLL action in adaptive RX sampling). (explained in 5.3.12.2)

3) It determines the reference point for the transmit clock in TE/LT-T mode. (explained in 5.3.12.3 and related to 5.2.5.2)

The "F-L zero crossing" is not detected. MTC-20172 SIC detects the transition mark-zero (instant t1) and the subsequent zero-opposite-mark (instant t2). During the F/L bits, the device oversamples the incoming signal with a fixed threshold, which is ALWAYS at 33 % of the nominal pulse height. AGC is active, see above.

In between t1 and t2, the RX part counts "Y", the number of zeros, ignoring possible marks. The zero count Y is less than the t2 - t1, because noise could force marks to be seen by the receiver during the interval.

The number "Y" of intermediate zeros is used to estimate the slope of the arriving signal, to predict the edge of the F/L transition. Y is limited to 15, which corresponds to a first order time constant of 2 µs for the S-bus data, filtered by the MTC-20172 SIC input filter. This is 2.5 times slower than the worst case point-to-point signal as specified in CCITT I.430 Figure 6.

Note that Y could be larger than 15 if the zero crossing is sought on a mark which is followed by a zero bit, i.e. when the violation is not the F bit followed by L.

5.3.12.1 Immediate Bit Synchronization at Instant T2

When the receiver is not synchronized, the receiver is oversampling and hunts for violations as explained under 5.3.11.1.

The F/L crossing is found at instant t2, and the 192 kHz bit clock and the 1536 kHz receiver clock are preset to predict an optimal sampling moment.

The data edge is estimated at instant (t2 - 2.00*Y).

For all modes (NT/LT-S and TE/LT-T) the optimal sampling precedes the theoretical edge by 8 periods of the 7 MHz clock. The advance is needed to allow a jitter of 7% (15% or 6 periods of 7 MHz) of the data, allowed according to the CCITT to be sent by any TE, combined with a 1 period DPLL correction needed at the NT/LT-S to correct for its own crystal.

Similar data jitter is also present at the TE when for example a 200 kHz interference signal, with amplitude 100 mVpp (peak to peak) is applied, as specified in CCITT I.430 8.6.2.1.

5.3.12.2 Continuous Bit Synchronization at Each F/L Crossing.

Once the receiver is synchronized on the data, the F/L edge is used on each frame to validate the sampling moment. The oversampling clock is used in the F/L window to validate the zero crossing.

At instant t2 (zero to opposite mark transition) the state of the counter generating the 192 kHz clock from the 7 MHz is compared with the optimal value, which should be loaded for an immediate bit synchronization as explained in the preceding section. If the difference (in nr. of periods of 7 MHz) is -1, 0, or 1, the counter is not changed, to provide hysteresis. If the difference is larger, the counters are adjusted with only 1 1, to limit the DPLL reaction.

In this manner, the sampling moment is adjusted with one 7 MHz period, every 250 µs. At the TE this allows a maximum frequency error of the crystal of 500ppm.

5.3.12.3 Optimal TX Bit Clock Derivation (ONLY at the TE/LT-T)

Once the receiver has reached synchronization, as explained in the previous paragraphs, the transmitter at the TE/LT-T can start sending INFO3. When starting to transmit, the transmit bit clock is forced at once to an optimal initial state, based on the downlink F/L edge. On each subsequent downlink F/L the transmit clock will be adjusted one period of the 7 MHz clock.

In the MTC-20172 SIC, the theoretical zero crossing is derived from the t2 and Y values, using the following formula, which incorporates the effect of the first order RX filter.

zero crossing time = t2 - 0.75 * Y - 5

On each subsequent received downlink frame, the DPLL does the following comparison: at instant t2 the TX clock counter should contain 0.75 * Y - 5. If the difference is within a dead zone of 1 1 period of 7 MHz around the optimal point the TX clock is not adjusted. Otherwise the clock is adjusted, but the maximal TX clock correction per frame is limited to 1 1 period of the 7 MHz. (Internally, the timing reference is corrected for other internal implementation delays besides the RX filter).

5.4 Timing Relation Between RX and TX on the S-Bus

The timing relation between RX and TX on the S-bus depends on the MTC-20172 SIC mode. Moreover, it can be trimmed, as described in 5.4.3.

5.4.1 S-bus Transmitter Versus Receiver Delay in TE/LT-T Mode

The CCITT imposes exactly 2 S-bus symbols, with a margin of +7% to -15% on the S-bus reference point. The downlink F/L framing signal is used as reference timing. Delays of the normal external devices (transformer) and internal MTC-20172 SIC filters are taken into account, during implementation, to advance the TX frame relative to the received F-L transition. In some applications, the external circuits add delay in the receiver path. For that reason the SIC device can force an extra time advance of the TX frame via the XTR4 strap.

5.4.2 S-bus Receiver Versus Transmitter Delay in NT/LT-S Mode

The Delay between transmitted and received frames at NT/LT-S is 2 bits plus the round-trip-delay across the S-interface, in normal operation. Worst case delay between downlink frames and uplink frames is 42 µs (see CCITT) or 8 bits. Longer delays cause problems for correct transmission of the E-channel bits, see 5.6. In loopback mode, the delay is zero.

The receiver in NT mode is designed to accept any delay while in adaptive sampling mode. This is convenient when looping the S-bus signals. E-channel operation is only correct if the delay is 0 to 8 bits.

5.4.3 Delay Trimming Via XTR4 Pin

The XTR4 or X4 pin can be used at NT/LT-S with fixed timing and at TE/LT-T.

In some applications the XTR4 pin can be used to trim for the delay of an external filter circuit.

The delay trimming has different effects:

In NT/LT-S with fixed timing on short bus, XTR4 at 0 delays the sampling moment with 5 periods of the 7 MHz clock, or 650ns. In the adaptive timing, no effect is seen.

In TE/LT-T mode XTR4 at 0 advances the normal transmit instant (2 symbols relative to the received frame) with 5 periods of the 7 MHz clock, or 650 ns. The delay is reduced.

5.4.4 More Delay Trimming.

The delay trimming can also be controlled via the GCI M-channel, adding 650 ns to the effect of the XTR4 pin. See 7.7.3 on internal registers.

5.5 Frame Relation Between GCI and S-Interface

In all modes of the MTC-20172 SIC except the LT-T mode, there is a strict relation between the S-bus frame and the GCI bus frames.

5.5.1 S-bus Transmitter Bit and Frame Clock NT/LT-S

If the MTC-20172 SIC is in the Network position, the 192 kHz S-bus bit clock is derived from the crystal clock, which is locked to the 8 kHz frame of the GCI bus.
The leading edge of the F-bit starts the frame on the S-bus. The DPLL inside MTC-20172 SIC forces this F-bit edge in a fixed range relative to the frame signal of the GCI bus.

Phase Relation Rule (NT/LT-S):

The F-bit start is situated in a 520 ns zone, starting with the edge between bit0 and bit1 on the GCI bus. The uncertainty is caused by the DPLL actions which will correct the 192 kHz S-bus clock in steps of 130 ns, i.e. one 7.6 MHz period.

Figure 5.5 shows the timing relation between the S-bus frames and the GCI bus for DCLK at 512 kHz (NT).

This phase relation optimizes the total roundtrip delay on the S-bus for each B-channel, if the GCI clock is 512 kHz. The delay of the NT with S-bus looped is only 125 µs for both B-channels at the GCI side. (This is the minimum).

For GCI clock speeds higher than 512 kHz, the round-trip delay can not be optimized for both B1 and B2 channel simultaneously. At least one B-channel has a 250 µs delay.

For simplicity, the S-bus frame and the GCI frame will keep the same phase relation independent of the used GCI

channel and for all GCI clock speeds. In this way, the B-channel roundtrip delay over the looped S-bus is maximally 250 µs.

The S-bus frame is locked to the GCI frame, with of course two random locking positions possible at a 125 µs distance. This forces all D-channels and E-channels of a group of SICs on a LT-S GCI bus to coincide. This allow the use of a common echo-bus to link multiple D-channels in a star configuration to a single HDLC controller at the LT-S side, see 5.6.

5.5.2 S-bus Transmitter Clock and Frame in TE Mode

In the TE position, the MTC-20172 SIC will lock on the 192 kbit/s received AMI data. The frame transmitted at the terminal side is delayed by two bits with respect to the received frame (see 5.4.1), adjustable according to 5.4.3.

The frame relation between the linked downlink and uplink S-bus frames and the local GCI bus of the TE is also fixed. The relationship is deterministic: it has minimal B-channel delay for both possible clock speeds of the GCI bus (i.e. 512 or 1536 kHz).

Phase Relation Rule (TE):

The downlink frame starts with the F-bit, which is followed by a balance bit L. The MTC-20172 SIC will force the leading edge of bit 0 of the B2 channel on the GCI bus to coincide with the internal sampling moment of the L-bit. The edge of the 8 kHz GCI frame signal precedes this instant by exactly 16 clock periods of the DCLK clock (i.e. 512 or 1536 kHz).

Figure 5.6 shows this for the 512 kHz case. Round-trip delay with GCI data looped is 125 µs.

Note that before the S-bus receiver is locked to the uplink device, the GCI clock and frame are asynchronous.

When synchronization is acquired, the MTC-20172 SIC will put the GCI frame in the optimal position (single jump). See also 4.10.2.

TE-mode exception: The clock relation is not applicable in TE-mode when the transmitter signal is looped back to the receiver. During this non-transparent analog loop, the MTC-20172 SIC uses its local crystal as master clock, and locks the GCI clock to the crystal. Note also that activation via the S-bus is possible during the loop mode.

5.5.3 Transmitter Clock and Frame in LT-T Mode

In the LT-T position, the MTC-20172 SIC will lock to the 192 kbit/s received AMI data, as in the TE case.

The frame transmitted at terminal-side is delayed for a period of two bits with respect to the received frame. This is deterministic, see 5.4.1, adjustable according to 5.4.3.
The main difference with the TE case

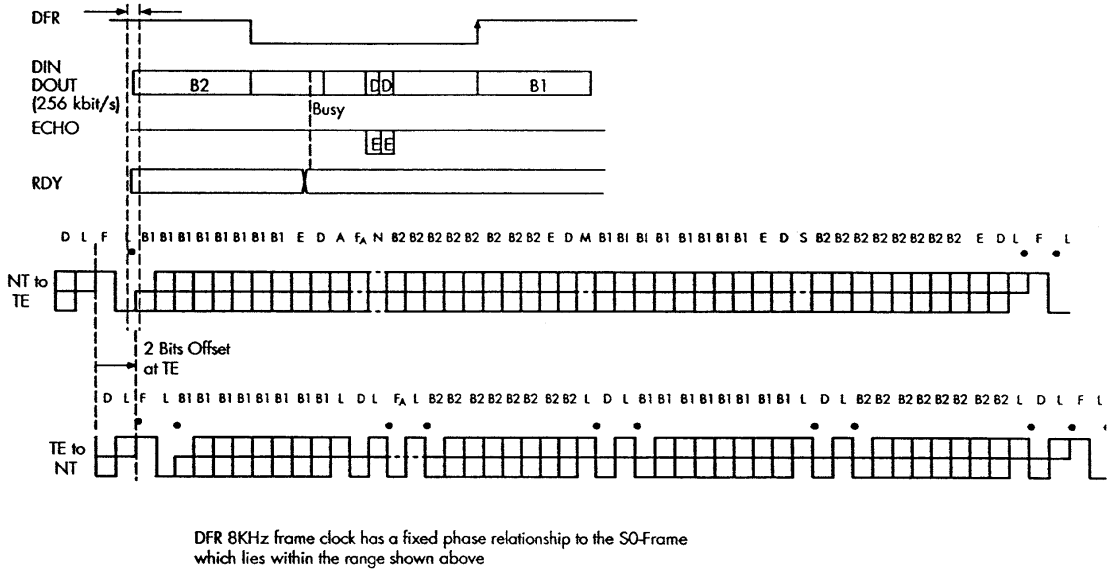


Fig. 5.5 : GCI S-bus Phase Relation TE Mode, RDY & ECHO pin

is the absence of synchronization of the S-bus and GCI bus. In LT-T mode the both the GCI and S-bus clock and frame signals are received. The MTC-20172 SIC must accept any phase relation between both frames. After GCI activation and S-bus synchronization, it presets the pointers in the RAM buffer between between both interfaces to allow a wander of 18 µs.

If, in spite of the 18 µs distance, the pointers in the RAM buffer are crossing over, the RAM pointers are shifted with 125 µs. This causes the repetition or deletion of a B-channel byte and of 2 bits on the HDLC D-channel.

LT-T-mode exception: The relation between transmitted bits and received bits at the S-bus is not applicable in LT-T-mode when the transmitter signal is looped back to the receiver. During this non-transparent analog loop, the MTC-20172 SIC uses the GCI clock as master clock, and locks its crystal to the GCI timing. (This behaviour is more NT/LT-S like, except that the loop is not transparent on the bus!). Note also that activation via the S-bus is possible during the loop mode.

5.6 E-Channel Generation in NT/LT-S

At the NT/LT-S, the MTC-20172 SIC mirrors the uplink D-bits in the downlink E-channel. The purpose of the E-channel is to control the D-channel access from multiple TEs on the S-bus.

In INFO2, the E-bits are zero; in INFO4, the E-channel mirrors the preceding D-channel bit received in the S-bus receiver.

5.6.1 E-Channel Generation In NT in STAR Configuration

In the STAR configuration, two or more MTC-20172 SIC devices drive separate physical S-buses, which are logically combined.

This STAR configuration allows the construction of a special NT1 where multiple point-to-point S-buses are tied to one U0-line, working logically as a single short passive bus.

The STAR configuration requires a logical combination of D and E-channels, and of the C/I and M-channels at the NT/LT-S. B-channels remain point-to-point links, assigned via the LAPD.

The MTC-20172 SIC restricts the STAR configuration to the D-channel, using a special Echo bus, explained in 5.6.3. The C/I channels of each MTC-20172 SIC are not combined. The C/I channel considerations are explained in 6.5.6.

5.6.2 E-Channel Generation In LT-S For HDLC Pooling

Theoretically, the same STAR configuration is possible in the LT-S position also. However, if the logical combination of S-buses is limited to the D-channel, it becomes possible to handle multiple S-buses with a limited pool of HDLC transceivers, without restricting B-channel connections, and without any C/I channel problems.

Each MTC-20172 SIC has its own GCI channel. The D-channels are merged via a special Echo bus, explained in 5.6.3. As long as MTC-20172 SIC devices are tied to the Echo bus they can be handled by a single HDLC D-channel device. All individual D-channels contain the same LAPD signals. The pooled HDLC device must be connected to only one of them. If the load on a shared D-channel is too large, individual D-channels can be disconnected from the shared HDLC receiver. Each MTC-20172 SIC can be programmed via an enable pin or via the M-channel to leave the Echo bus.

5.6.3 E-Channel Generation: Operational

Without STAR, the E bit is simply the echo of the downlink D-bit. There is an exception in the extended Mode, when the TIC protocol is used, see 5.8, but the TIC protocol is NOT implemented.

The SICs in STAR or HDLC-pooling configuration use a common bus line to combine all accesses to the uplink D-channel. It is called D-channel Echo (DE) bus in Basic Mode, and the Common Echo Bit (CEB) bus in extended Mode. The bus pin has an internal 50 kΩ pull-up resistor (pin XTR0 in NT mode, pin AUX4 in LT-S mode). Each MTC-20172 SIC can pull the bus low with an open drain output.

When a group of SICs is tied to a DE/CEB bus, each SIC can individually participate or not. Participating SICs drive the received D-channel bits via the open drain output, and sense the common E-bit. The common E-bit is also the D-channel bit which is sent on the GCI channel. Non-participating SICs do not pull the bus low and

ignore the content.
Participation on the DE/CEB bus can be forced via a pin (DEX) and via an internal register bit. The participation is a logical function of the DEX pin (see 4.11 and 4.12) and the DEX bits (control via the M-channel, see 7.7.3).

Implementation issue:

Note that each individual MTC-20172 SIC tied to the DE/CEB bus must work with the same GCI frame indication, but not necessarily the same GCI channel. Each MTC-20172 SIC drives the S-bus with frames strictly synchronized to the GCI interface frame, see 5.5.1, and Figure 5.5.

This means that driving and sensing the DE/CEB bus can be done in a distributed way. Each MTC-20172 SIC drives the DE/CEB bus when the uplink D-bit is sampled, and senses the DE/CEB bus when E-bit must leave, without possible discrepancy in each E-channel. Note that DE/CEB could work incorrectly when the uplink signals have a delay of zero bits, i.e. in loop condition. The timing diagram is included in Figure 5.5.

5.7 D-Channel Access in TE/LT-T

In the uplink direction, the D-channel is organized in a multipoint manner on the S-bus.

To allow only one TE on the D-channel, a collision detection and a strictly fair access protocol is defined by the CCITT I.430. To detect the availability and collision at the TE, the E-bit echo channel is used. The downlink E-channel contains the reflection of actual uplink D-bits which are seen at the NT/LT-S, see 5.6. When an electrical collision happens on the S-bus, the binary zero wins.

The messages sent on the D-channel are HDLC messages, containing a start flag, message bodies and end flag. In between the messages the channel returns to idle (all binary ones). The idle on the D-channel allows the different TEs to detect the availability of the D-channel. The TEs do not monitor idle on the uplink D-channel directly, but monitor this via the E-channel.

When the TEs see the idle on the E-channel they can start a message. The TE which start first gains the access, because the start flag begins with a zero. When many TEs start a message simultaneously at the same bit position, the flags will coincide. However, the message body will differ somewhere. The collision detection is based on E-channel observation. The TE which sends D = binary one which is overwritten by a zero on the S-bus, loses the access, because the E-channel reflects the zero. The TE which detects a collision releases the D-channel by sending idle on the bus. The TE which won the collision, continues without even knowing it occurred.

After a TE has transmitted a complete message, or lost the D-channel in a collision, it must detect a number of idle bits X before it can start another transmission. The number X is defined for 2 priority classes: X=8 and X=10. When a TE has successfully transmitted a message it increases X by 1 (to 9 or 11). If X is at 9 (or 11) and this exact number of ones for an idle is seen on the bus, then it resets the X to 8 or 10.

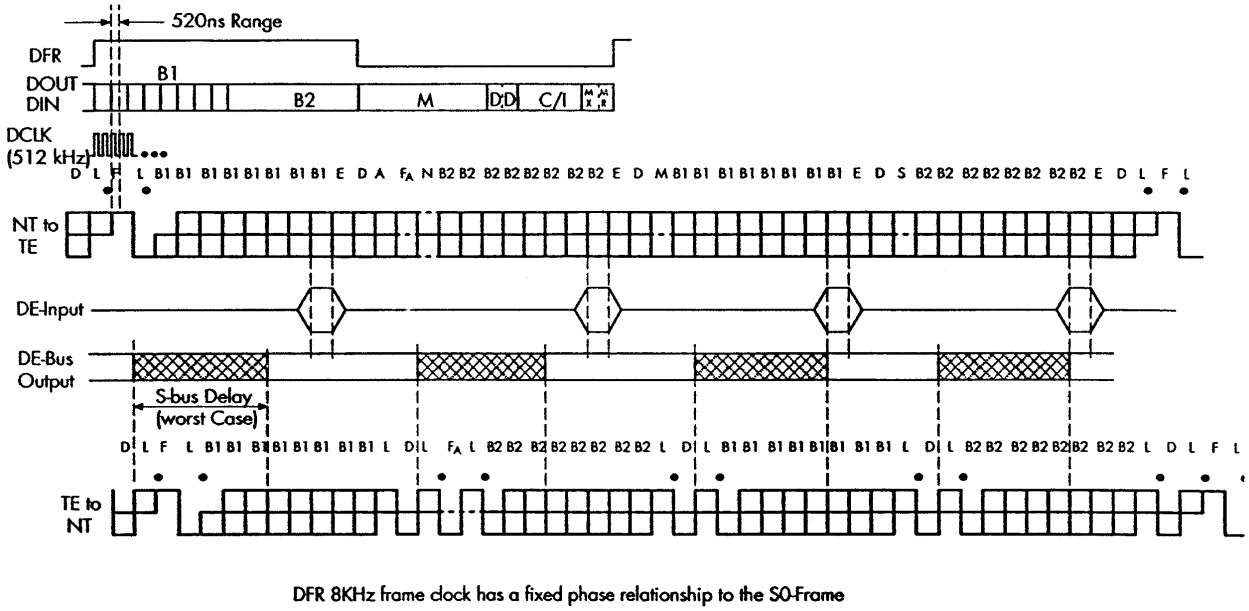


Fig. 5.6 : GCI S-bus Phase Relation NT/LT-S Mode, DE/CEB timing

HDLC message properties:

The HDLC flag is 01111110 in binary, or 7E hex. The message bodies never look like idle or flags, because a bit stuffing mechanism forces extra zeros when 5 consecutive ones are seen, see CCITT I.430. In some cases the message body is not terminated correctly with a flag but with idle; this is an abort. When aborting a message, the TE must release the D-channel also

5.7.1 D-Channel Access Working Principles for the MTC-20172 SIC

The TE/LT-T access on the D-channel is the combined operation of the MTC-20172 SIC working together with an intelligent HDLC device. The D-channel coming from the HDLC device is not transparently transmitted from GCI bus to the S-bus. Inside MTC-20172 SIC, there is a D-channel Access Controller (D-AC), which limits the access according to the S-bus rules.

The D-AC knows about the general principles of the HDLC LAPD channel and of the echo channel. It must recognize the idle via the E-channel, it must know about the priority classes when trying to access, it must track the HDLC messages of its local HDLC transmitter: It recognizes the (single) start flag of a message and the end flag or abort of the message. When it sends a message it must recognize the collision of the message on the S-bus.

5.7.2 The D-Channel Access Controller (D-AC) - Functional description

The D-AC can only handle one priority class simultaneously. The priority is indicated via the C/I nibble in the GCI B1*-channel, see 6.5.10.

The D-AC can be in the READY or BUSY state. The D-AC changes states at each observation of the (downlink) E-channel. When it is in the READY state, it allows the GCI D-channel transparently on the S-bus. When it is BUSY it forces idle on the S-bus. The detailed state diagram described in Figure 5.7, with a number of control variables:

- The variable C: the count of consecutive ones on the E-channel;
- The variable P: indicates the priority class (8 or 10);
- The variable R: 0 or 1, indicates the priority reduction; simply added to P, changing priority to 9 or 11;
- The variable V: indicates a violation between D and E when 1.

The D-AC can only go from BUSY to READY when the E-channel contains a number of idle bits equal to or larger than X, the priority class. This is when C= P + R. The condition C>= P + R is used, to allow changes in P.

The D-AC goes from READY to BUSY when:
1) a violation is seen, (from states RDY1, RDY2, RDY3 to BUSY);
2) OR the start flag + message body, is eventually followed by an end flag; message can be empty;
3) OR the start flag + message body, is eventually aborted (forced to idle without end flag); message can be empty;
4) OR a starting flag degenerates to idle;
5) OR a message without correct starting flag is followed by an end flag + idle or is aborted;

The D-AC will allow D-bits transparently on the S-bus when it is in the RDY1 to RDY4 states. The RDY4 state is added to the Basic Mode state diagram, to allow the last zero of the tail flag to leave. The MTC-20172 SIC has only a limited control on the content of the D-channel after it goes to the READY state. See 5.7.7.

The BUSY2 state is added to send an anticipated READY via the RDY pin and via the GCI bus, see 5.7.3 and 5.7.4.

The Variables and how they Change :

Variable R goes to 1 when a successful end flag is transmitted or when a message is aborted, i.e. in the RDY4 state. The variable R goes to 0 when C>= P + R, i.e. in the RDY1 state. CCITT I.430 states: The priority count X (=P+R) can be reduced, i.e. R := 0, when the priority count X is at P + 1 (9 or 11) and this exact number of ones for an idle is seen on the bus.

Count C is updated for each received E-bit. In the RDY4 state, C will be at 0, because then the last (zero) bit of the end flag is seen. We force C = 0 in the RDY4. This happens when the local HDLC message was aborted, and it keeps the local HDLC transmitter from restarting a new message too soon.

Variable V is the Violation detection. To change states, the D-access controller compares the D-channel bits with the E-channel bits. This comparison is done bit by bit. The variable V is the EXOR of the E-bit and the D-channel bit sent on the S-bus.

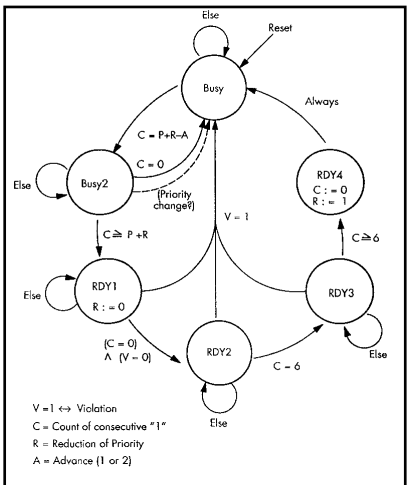


Fig. 5.7 : State Diagram of D-Channel Access Procedure

Normally, a violation is E=0 and D=1, however the opposite case is also considered a violation. This stops the message when a bit-error is seen.

Variable P contains the priority class, 8 or 10. This variable can change via the command interface, see 6.5.10. When P is changed in the RDYi states, the ongoing transmission will not be affected.

5.7.3 READY Signal

The external HDLC controller can monitor the READY/BUSY via a pin and via a bit on the GCI bus, in the TE and the LT-T modes.

The RDY pin is available in the TE and the LT-T position in Basic Mode and in extended Mode, see 4.11 and 4.12. The polarity is normal. RDY = 1 means D-channel available. RDY = 0 means D-channel NOT available.

The MTC-20172 SIC has a BUSY bit in the GCI M-channel at the 5th position (numbering 1 to 8), in TE and LT-T position, for both modes. The polarity is normal. BUSY = 1 means D-channel NOT available. BUSY = 0 means
D-channel available.

The MTC-20172 SIC in the extended TE mode has an extra RDY bit in the B*-channel of the GCI channel 2, position 3 (numbering 1 to 8). The normal GCI information is in the GCI channel 0. The name RDY is confusing, because the polarity of this RDY bit is INVERTED. RDY = 0 means D-channel available. RDY = 1 means D-channel NOT available.

The MTC-20172 SIC always offers both the BUSY bit in the M-channel and the RDY pin.

5.7.4 Anticipation and LAPD Fairness

Anticipation

The RDY pin and the RDY bit must anticipate the READY state, because the uplink D-channel is sent with two bits grouped, because the E-channel has an extra roundtrip delay, and because the RDY pin and the BUSY signal are sampled at a fixed position in the 8 kHz GCI frame.
The BUSY2 state anticipates the RDY pin and bit indication.

Lapd Fairness

In spite of the anticipation of the RDY signals, the LAPD fairness is not optimal. Indeed, the relation between the MTC-20172 SIC and the HDLC transmitter via the GCI bus limits the reaction time. Even in the best situation, the uplink messages will be one bit late in 50 % of the time. Giving more anticipation is impossible, because then it could happen that the ready indication arrives too soon at the HDLC controller. The opening flag would then be mutilated, which causes useless retransmission delays and even deadlock situations.
In the LT-T position, the fairness is worse, because the delay of the D-channel is larger, caused by the asynchronism between the GCI bus and the S-bus. Luckily, in LT-T mode, the MTC-20172 SIC is normally the only TE on the T-bus, and fairness is not an issue.

Fairness Enforced ?

If the HDLC controller wants a fair access in TE or LT-T mode against some other terminal on the S/T-bus, it can force the D-channel in all zero state. The D-AC will dump the zeros in the D-channel, which blocks the access of all other TEs. The leading zeros can be followed by a normal start flag + message + tail flag and idle. Also see 5.7.7.

Note that the priority change X to X+1 will still allow all other terminals an access on the D-channel.

5.7.5 RDY Pin and Bit Operation in Basic Modes;

Anticipation in the Basic TE mode is 2 bits.
Anticipation in the Basic LT-T mode is 1 bit.
Timing (see Figure 5.6)

5.7.6 Timing and Operation in extended Modes;

Anticipation in the TE and LT-T mode is 1 bit.

Timing (see Figure 5.6)

In the extended mode of the MTC-20172 SIC, the RDY pin and the BUSY bit in the M-channel change simultaneously.

5.7.7 Illegal Messages from the HDLC:

Multiple Leading Flags:

MTC-20172 SIC will not handle messages with too many leading flags. It will consider any second flag a terminating one and go to BUSY.

Messages preceded with non-idle preceding the start flag.

If the start flag is not preceded by a normal idle but by some header containing zeros, different from a flag or idle, the D-AC remains in the RDY2 sub-state. It will wait for the start flag + message + tail. It was decided to allow this incorrect behaviour of the HDLC transmitter to avoid some problems in the LT-T situation, see 5.7.4 above.

Messages started without a start flag.

The D-AC does not block messages without a legal start flag from the local HDLC transmitter.

When the HDLC is not synchronized with the READY signal, it could happen that the D-AC opens the D-channel to the HDLC transmitter while it is not sending idle. Then a message without opening flag is sent on the D-channel of the S-bus.

The D-AC can not detect this behaviour. The D-AC reaches the different ready states. It goes only to BUSY when the end flag arrives followed by idle, or if the message is aborted (forced to idle without end flag). The HDLC receiver in the NT position will normally ignore the message. It will only react on the end flag followed by the idle.

5.7.8 E-Channel To External-HDLC Device at TE Position.

The D-channel access can also be controlled outside the MTC-20172 SIC, by supplying the E-channel to the external HDLC device.

In Basic Mode, the E-channel is put on the ECHO pin, see 4.11 and 4.12. The ECHO pin contains the downlink E-bits synchronized with the GCI D-bits. All other bits are at 1. Timing as in Figure 5.6.

In the extended (GCI) TE mode, the actual E-channel is not available on a separate pin, but present on the GCI bus. The normal GCI information is in the GCI channel 0. The extra E bits are put in B*-channel of the GCI channel 2, position 1 and 2, numbering from 1 to 8. Timing in Figure 5.6. (NOTE: The 3rd bit is the RDY indication).

5.8 D-Channel Access in NT/LT-S: TIC Protocol

This feature is NOT included in the MTC-20172 SIC.

If necessary an intelligent HDLC device can use the DE/CEB bus to monitor the E-bits and to drive the GCI D-channel, see 5.6. Only the 16 kHz clock must be provided externally, synchronized with the GCI framing.

5.9 Multiframing; S and Q Channel Functions

The MTC-20172 SIC supports multiframing according to I.430.

The MTC-20172 SIC can transmit a Q-channel at 800 bit/s uplink, synchronized with a multiframing indication. In the downlink direction, the MTC-20172 SIC can send a multiframe indication and the S-channel at 800 bit/s.

The S and Q bits can be accessed via the M-channel, see 7.5. During system reset condition, the internal MTC-20172 SIC S and Q-bit registers are set to logical '0' at the NT/LT-S and set to logical '1' at the TE/LT-T.

5.9.1 Compatibility With the MTC-2072 SIC

In the MTC-2072 SIC, a bit called “E-bit” in the B1* channels was used to enable and synchronize the multiframing. This operation is not supported anymore. It was not supported by any other component.

5.9.2 Multiframing Enabling

The enabling of multiframing is the OR function of 3 inputs:

1) a PIN (MFD),
2) a register bit, and
3) a special GCI framing.

1) In the NT modes (Basic and extended modes) there is a MFD MultiFrame Disable pin, with an internal weak pull-up, see 4.12.

2) In ALL modes, multiframing can be enabled via the M-channel on the GCI bus. At RESET the multiframing is disabled.
3) In ALL modes, except in the inverted mode multiframing can be enabled via the width modulation of the GCI frame signal, see next section.

5.9.3 Functional Behaviour at The NT/LT-S

When multiframing is disabled, the MTC-20172 SIC will send the FA and the M bits and also the S-channel as binary zero, in downlink direction.

When multiframing is active, the MTC-20172 SIC transceiver will send FA='1' as "Q-frame identifier" in every fifth S-bus frame, and M='1' as multiframe identifier in every 20th S-bus frame (5 ms), as required in the CCITT I.430. The coding of the corresponding N-bit remains always N = .NOT. FA.

The S-channel is a 4 kbit/s channel, transmitted in frames of 20 bits, subdivided in 5 groups of 4 bits, for i = 1 to 5, Si1, Si2, Si3, Si4. Only the S1j bits can be accessed, or 400 bit/s. The other S bits are forced to 0. See TABLE 5.1.

Synchronous with the M=1, FA=1, the S11 bit is sent. The S-bits are taken from the S registers, writable via the M-channel. In the uplink direction, the Q1, Q2, Q3, Q4 bits are found at the FA position of the received S-bus frames and stored in the Q register, accessible via the M-channel.

When the width of the frame pulse is reduced to one clock period of the data clock, the MTC-20172 SIC will enable multiframing. The width modulation must be done with a cadence of once per 5 ms, and the MTC-20172 SIC will synchronize the multiframe start (S and M bits at binary ONE) with this event. Frame width modulation is impossible in the inverted mode, because the frame pulse is always 1 clock period long.

5.9.4 Functional Behaviour at TE/LT-T Side

If the MTC-20172 SIC has multiframing disabled at the TE/LT-T position, it sends an uplink frame having FA = 1, in response to each downlink frame with FA = 1.

If the MTC-20172 SIC has multiframing enabled at the TE/LT-T position it tries to synchronize. As long as MTC-20172 SIC is not synchronized, it sends an uplink frame having
FA = 1, in response to each downlink frame with FA = 1.

Synchronization at the TE/LT-T: When the MTC-20172 SIC sees M = 1, and FA = 1 in a received S-bus frame, followed by a complete 5 ms multiframe with the correct values for M and FA, then it assumes multiframe synchronization. See TABLE 5.1, or CCITT TABLE 7/I.430. As soon as one value of FA or M is incorrect, synchronization is lost.

Once it is synchronized, the MTC-20172 SIC starts transmitting the Q channel in the next 5ms multiframe. The Qi bits positions are shown in TABLE 5.1, or CCITT TABLE 7/I.430.

5.9.5 Automatic S and Q Bit Interpretation

Automatic power loss indication is not implemented in MTC-20172 SIC.

5.9.6 Multiframing and S-bus Synchronization

Multiframing affects the S-bus synchronization, see 5.1.7.

5.10 BER PIN

The BER pin signals errors in the RX data, when synchronization is reached. If too many errors force the MTC-20172 SIC out-of-sync, it indicates this via the C/I channel.

BER = Bit Error Rate: each excessive violation seen during the S-bus frame between position 14 and 48 indicates a link transmission problem, except in uplink frames during multiframing (see 5.1.7). Each error forces this BER output low for one S-bus bit period. All BER outputs can be tied to a single bus.

Table 5.1 : Multiframing Sequence *(with i = 2, 3, 4 or 5)*

frame number	FA downl.	FA uplink	M downl.	S downl.
1	ONE	Q1	ONE	S11
2 - 5	ZERO	ZERO	ZERO	Si1 = ZERO
6	ONE	Q2	ZERO	S12
7 - 10	ZERO	ZERO	ZERO	Si2 = ZERO
11	ONE	Q3	ZERO	S13
12 - 15	ZERO	ZERO	ZERO	Si3 = ZERO
16	ONE	Q4	ZERO	S14
17 - 20	ZERO	ZERO	ZERO	Si4 = ZERO

6. The GCI Interface

6.1 The GCI Interface

At the digital control interface, the MTC-20172 SIC is connected via a bidirectional serial interface, a digital bus called the General Circuit Interface (GCI). Data (in B+D channels) and control information are passed on a 256 kbit/s channel of the GCI bus. In PABX systems, many SICs may be connected to a single multipoint bus. In this case, there is a "burst" transmission. The MTC-20172 SIC adapts its speed automatically to the available speed on the bus. Moreover, the MTC-20172 SIC can use one of 8 consecutive GCI channels, numbered 0 to 7. The maximal speed of the bus is 4096 kbit/s.
The description of the GCI standard is also available as a separate document.

6.1.1 General Content of the GCI Bus For MTC-20172 SIC

The GCI interface contains: B1, B2, M-channel, B1* channel.
In ISDN applications, the B1* channel contains two D-channel bits, 4 C/I bits with the commands (towards the MTC-20172 SIC) or the status indications (from MTC-20172 SIC), and two extra bits to control the maintenance channel, MX and MR.

A general overview can be found in 4.6.2. For details see paragraphs:-

Physical Organization :	6.2
B-channels :	6.3
D-channel :	6.4
C/I channel :	6.5
M-channel, MX and MR :	6.6

6.2 The Physical Organization of the GCI bus

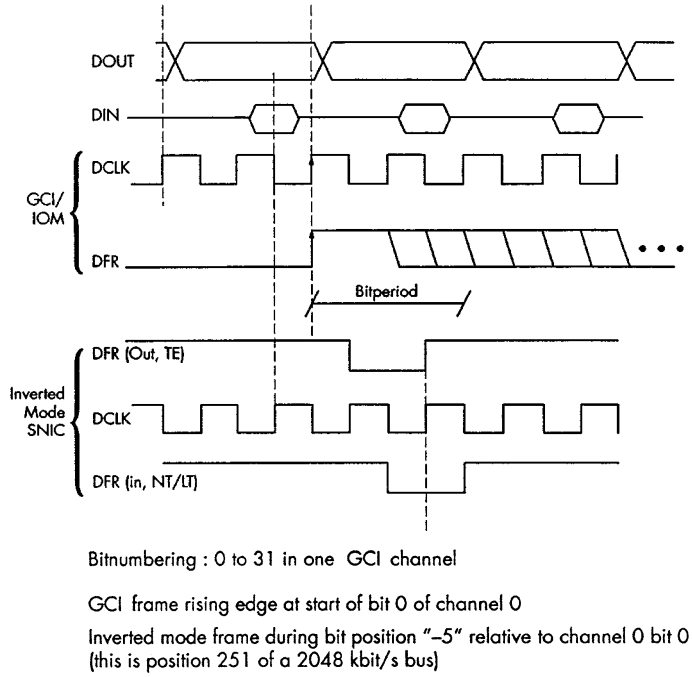
The bus has a clock and frame signal as timing, and two data lines, one for each direction.

The actual timing and speed of these 4 signals exists in several flavors and variants. The MTC-20172 SIC provides all the different variants of the prevailing standards :
See TABLE 4.1:
- V* master mode, with clock at 512 kHz;
- V* slave mode, defined at 4096 kHz, but accepting any CGI clock;
- Inverted mode at 512 kHz, clock inv., frame neg. & advanced;
- Inverted MUX mode at 4096 kHz, clock inv., frame neg. & advanced;
- CGI master mode, with clock at 1536 kHz;
- CGI slave mode, clock recognition, 512 kHz - 8192 kHz.

The clock, frame and data relation is shown in Figure 6.1; the timing and electrical details in chapter 9.

6.2.1 Clock and Frame Signals (see Figure 6.1)

In the TE mode, the clock and frame are generated by the MTC-20172 SIC. Here, the timing is slaved to the S-bus and the network.
In the LT-T, the LT-S or the NT mode, the MTC-20172 SIC receives the GCI timing. In the LT-T the MTC-20172 SIC must handle slip between the GCI timing and the received S-bus clock.



Bitnumbering : 0 to 31 in one GCI channel

GCI frame rising edge at start of bit 0 of channel 0

Inverted mode frame during bit position "–5" relative to channel 0 bit 0 (this is position 251 of a 2048 kbit/s bus)

Fig. 6.1 : Relation of Clock, Frame and Data on the GCI bus; Normal and Inverted (or V*) bus

The clock signal is twice the bit-rate of the serial data lines. The clock entering the MTC-20172 SIC can be ANY multiple of 16 kHz between 512 kHz and 8192 kHz.
The frame signal has two possible polarities: GCI style or Inverted.

The MTC-20172 GCI selects automatically between mode and inverted mode based on the frame width.
The GCI frame signal is often a 50% duty-cycle signal, but only the rising edge is important. The frame indicates the bit 0 of channel 0, the first bit of the frame. If the width of the HIGH part of the frame signal is narrowed to only one clock cycle, this indicates a multiframing request, see 5.9. The narrowing must run at a cadence of once per 40, 8-kHz frames.

In the inverted mode (see TABLE 4.1 and Figure 6.1), the descending edge of the frame is used; it indicates the bit position -5 before the bit 0 of channel 0. The frame signal is low for only one cycle of the clock signal. This allows the automatic recognition of this mode. The inverted frame sent to the MTC-20172 SIC is displaced by half a period of the clock. Note that the inverted mode will not support multiframing indication or synchronization. Extra clock signals are present on the MTC-20172 SIC to support other bus related functions (e.g. CODECs), see tables 4.1a and 4.1b. All clock outputs of the MTC-20172 SIC are normally derived from the crystal. However, in the TE and LT-T modes some clock outputs, marked with "*" in TABLES 4.1.a & b, are synchronized with the downlink S-bus interface.

Details on the timing can be found in chapter 9.

6.2.2 Channel Selection

The MTC-20172 SIC will access the first GCI channel group after the frame pulse, in all non-multiplexed modes.
In the multiplexed modes, the MTC-20172 SIC will access a GCI channel group at the position indicated by the TSi input pins. (See 4.11 and 4.12).
The MTC-20172 SIC does not allow some channels to be displaced to other position in the frame.

6.2.3 DATA Pin Tristate or Open Drain Operation

The I/O type of the DOUT pin of the MTC-20172 SIC is found in TABLE 3.3, in function of the configuration modes of TABLE 4.1; for electrical and timing properties, please see chapter 9.

6.2.4 Power-down and Power-up On The GCI Bus

For maximum power saving, the GCI bus can be halted completely in the TE and NT modes.

POWER-DOWN

The principles of the shut down procedure are shown in Figure 6.1a. The upstream device is the master of the bus, and will shut it down by halting the clock and frame in a low voltage, low impedance state. The data lines are in a high voltage and high resistance state (with a pull-up device).

Before shut-down, all device must prepare to reactivate the bus or to recognize the reactivation via the bus.

The time of the shutdown is related to the C/I channel and the actual commands and indications. The upstream master device sends the deactivate request (DR="0000"), the downstream device answers with the Deactivate Indication upstream (Dlu="1111"). The "all one" Dlu is compatible with the idle state of the upstream data line in an "all one" state. The bus master waits until it sees the Dlu, and changes the downstream C/I to "1111" = Dld (basic) = DC (extended). This is the deactivation confirmation. The master sends DC exactly 4 times, and shuts the clock down after the last bit of the fourth occurrence of the C/I = "1111".

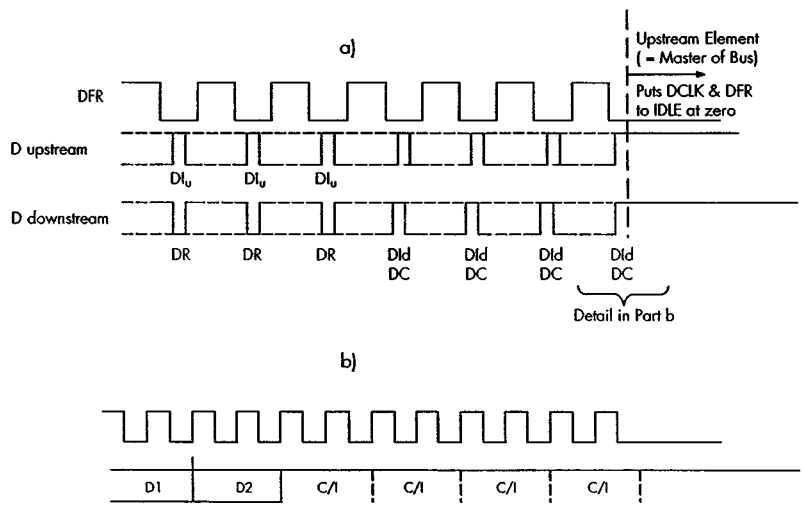


Fig. 6.1a : Deactivation of the GCI Interface

The upstream device can then enter the complete internal power-down state.

After validating the DC or DId, the downstream device goes to the idle state, it will release the upstream data line completely, which will be held high by a pull-up resistor.

The downstream device can enter the power-down state earlier than the upstream master, only the GCI bus part must count frame activity and recognize activity beyond the shut-down instant. (Indeed, this is recognition of bus reactivation by the upstream device).

Asynchronous Power-Up Request from the Downstream Device

If the downstream device wants to activate the bus, it pulls the upstream data line low (against the pull-up resistor).

The upstream bus master recognizes this as an activation and starts the bus, as described in the next paragraph.

The downstream device can keep the data line low until it has recognized the activity on the GCI bus and it is synchronized on clock and frame. As long as the downstream device pulls down the data line the C/I is "TIM" ("0000" or timing request).

POWER-UP from the Upstream device

The upstream device is awakened by the network or by the asynchronous power-up request from the downstream device, see previous paragraph.

In both cases, the upstream device simply starts the clock, frame and data of the bus.

If the downstream device is still in power-down, the frame signal is recognized by its GCI bus part. Indeed, it is awakened by a frame signal edge after the shut-down instant.

6.2.4.1 MTC-20172 SIC Power-down and Power-up in NT Mode

Here, the MTC-20172 SIC is a slave on the GCI bus.
POWER-DOWN of the MTC-20172 SIC in NT mode

The general procedure to shut down the GCI bus (see above) forces the MTC-20172 SIC into the maximum power-saving state (3) "Deactivated", see 6.5.2 and Figure 6.1a.

The DC command deactivates the S-bus transceiver, the internal clock distribution and the XTLO output pin (i.e. the 7 MHz crystal oscillator). If no crystal is used, the 7 MHz clock on the XTLI pin can be shut down.

The asynchronous signal detector is the only active part in the S-bus transceiver, the GCI part runs no activity internally, it will only react on a rising edge of the frame signal, to start again.

POWER-UP of the MTC-20172 SIC in NT mode

a) Activation through the S-bus will be seen by the activity detector.

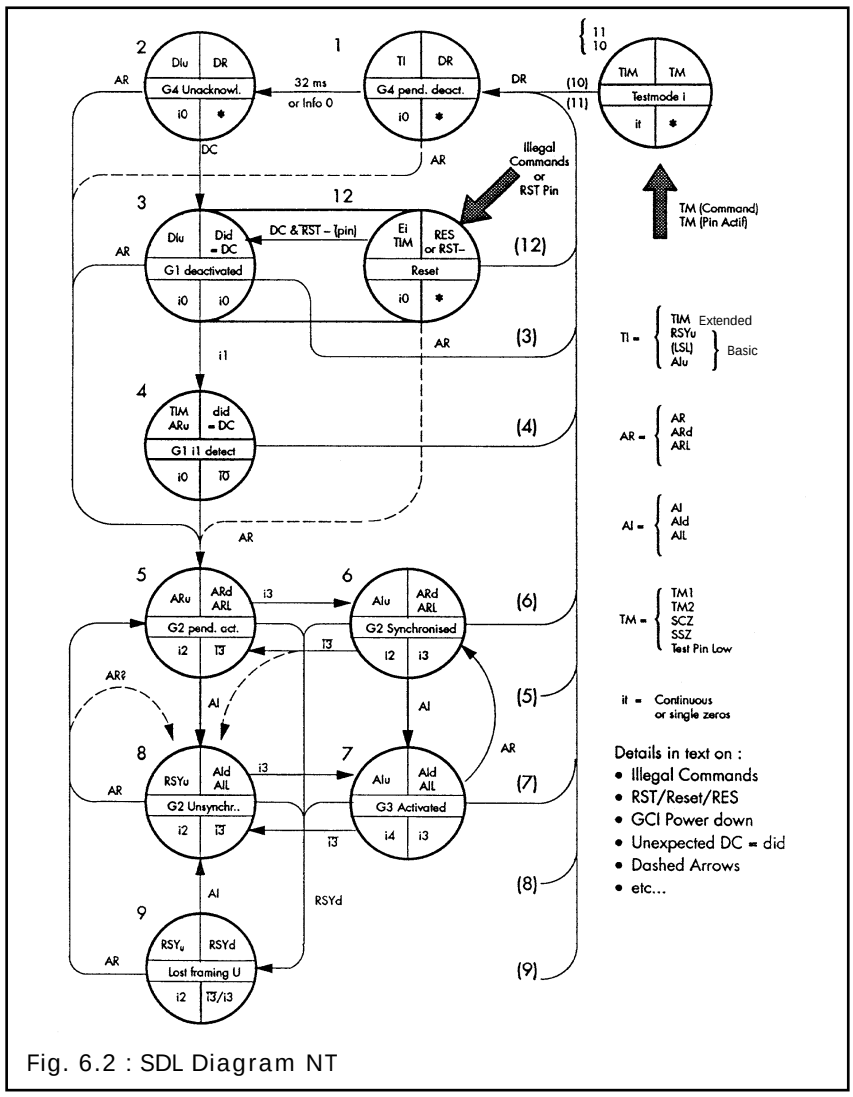


Fig. 6.2 : SDL Diagram NT

The MTC-20172 SIC does not need a crystal input or GCI clock to activate the GCI interface, which it does by asynchronously pulling the GCI data line low. The bus master activates the bus and it must also deliver the 7 MHz master clock if it is generated externally of MTC-20172 SIC. If an crystal is used for the master clock signal, the MTC-20172 SIC will enable the crystal oscillator when it sends the asynchronous activation request on the GCI bus.

b) Activation through the GCI bus consists of clock and frame delivery, followed by commands via the C/I channel. MTC-20172 SIC will activate the S-bus transceiver according to the commands; it also starts the crystal oscillator. If the master clock is generated externally it must be delivered to MTC-20172 SIC.

In both cases a) and b), a delay of 2ms is needed by the crystal oscillator to start running.

6.2.4.2 Power-down and Power-up in TE Mode

In the TE mode, the MTC-20172 SIC is master of the GCI timing.

POWER-down of the MTC-20172 SIC in TE mode

The procedure to shut down the GCI bus (see above) brings the MTC-20172 SIC into the maximum power-saving state (1) "Power Down", see 6.5.4 and Figure 6.4.

The Dlu command deactivates the S-bus transceiver, except the activity detector.

If the ENCK input of MTC-20172 SIC (see under 4.11 and 4.12) is off, the MTC-20172 SIC shuts down the GCI bus, the internal clock distribution, the XTLO output pin (i.e. the 7 MHz crystal oscillator), and the extra clock outputs, shown in TABLES 4.1a & b. The asynchronous signal detector is the only active part in the S-bus transceiver, the GCI part runs no activity internally, it will only react on a falling edge of the data input signal.

If ENCK stays active, the crystal, the GCI bus, and all clock outputs stay active. The power saving is not optimal.

POWER-UP of the MTC-20172 SIC in TE mode

Activation through the S-bus is possible. The signal detector enables the crystal, the GCI clock and frame is activated, the receiver hunts for synchronization, indications and commands are exchanged via the C/I channel and the MTC-20172 SIC awaits further commands.

On activation through the GCI bus, the controller pulls the data line low (timing request). The MTC-20172 SIC enables clock and frame, and C/I codes are exchanged between the MTC-20172 SIC and the controller.

The controller has an alternative way to activate the GCI bus in TE mode: It pulls the ENCK pin active in power-down, and the MTC-20172 SIC starts the crystal and delivers the GCI timing signals and all other clock signals.

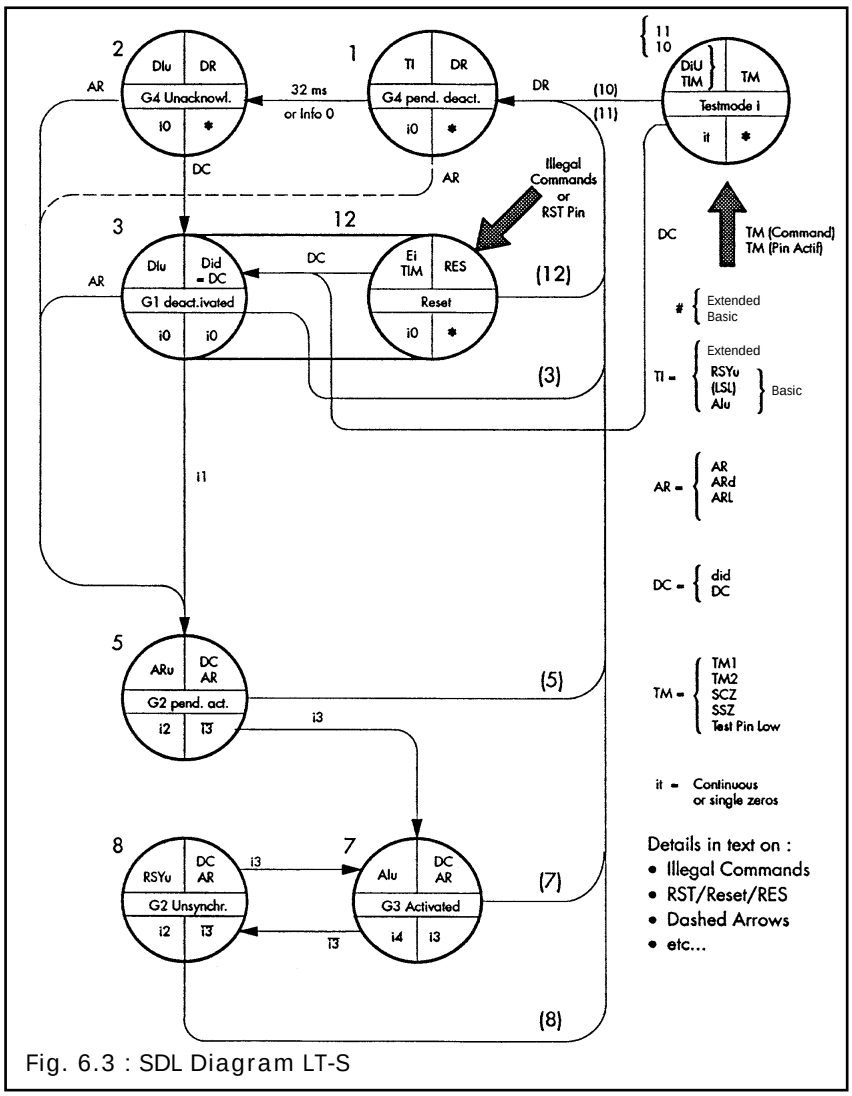


Fig. 6.3 : SDL Diagram LT-S

One major difficulty exists:
Once the MTC-20172 SIC has acquired synchronization on the downlink data, the GCI frame must be adjusted to the received frames.
This is needed to minimize transport delays of the B-channels. There is an optimal fixed relation between the received S-bus frame and the GCI frame, see 5.5.2.

The locking of the GCI frame to the S-bus frame causes a jump of the GCI frame pulse. To limit the number of phase jumps, the free-running GCI pulse is only adjusted when the full synchronization on the
S-bus frames is acquired.

6.2.4.3 MTC-20172 SIC Power-down and Power-up in The LT-S/LT-T

In the LT-S/LT-T modes the GCI bus is not put in power-down. The GCI clock and frame run continuously.

However, the MTC-20172 SIC can be forced in a low power state via the dedicated "1111" command. This is the "did" or DC command in LT-S and the Dlu command in LT-T, see 6.5.9 and 6.5.10.
The MTC-20172 SIC in LT-S mode goes to the state (3) "Deactivated", see 6.5.3 and Figure 6.3.
The MTC-20172 SIC in LT-T mode goes to the state (1) "Power Down", see 6.5.4 and Figure 6.4.

This command deactivates the analog part of the S-bus transceiver, and partly the internal clock distribution. The asynchronous signal detector is the only active part in the S-bus transceiver, the GCI part will react on new C/I channel commands and on M-channel activity, but runs no other activity internally.
The 7 MHz master clock stays active if a crystal is used between the pins XTLO and XTLI.

Special clock pins for the LT-T mode:
As long as the XTLI pin receives a 7 Mhz signal (with crystal or other clock source), the SCLK 512 kHz* output (in the LT-T normal mode) or the XTR3 1536 kHz* output (in the LT-T extended mode) will stay active.

These pins contain a clock signal, which is normally synchronized on the S-bus downlink bit-stream, but which can not be adjusted when the S-bus is idle.
The SCLK or XTR3 clock will have the same frequency error as the XTLI clock signal.

If the clock signal XTLI is shut down, the SCLK or XTR3 pin will go to an (undefined high or low) permanent DC state.

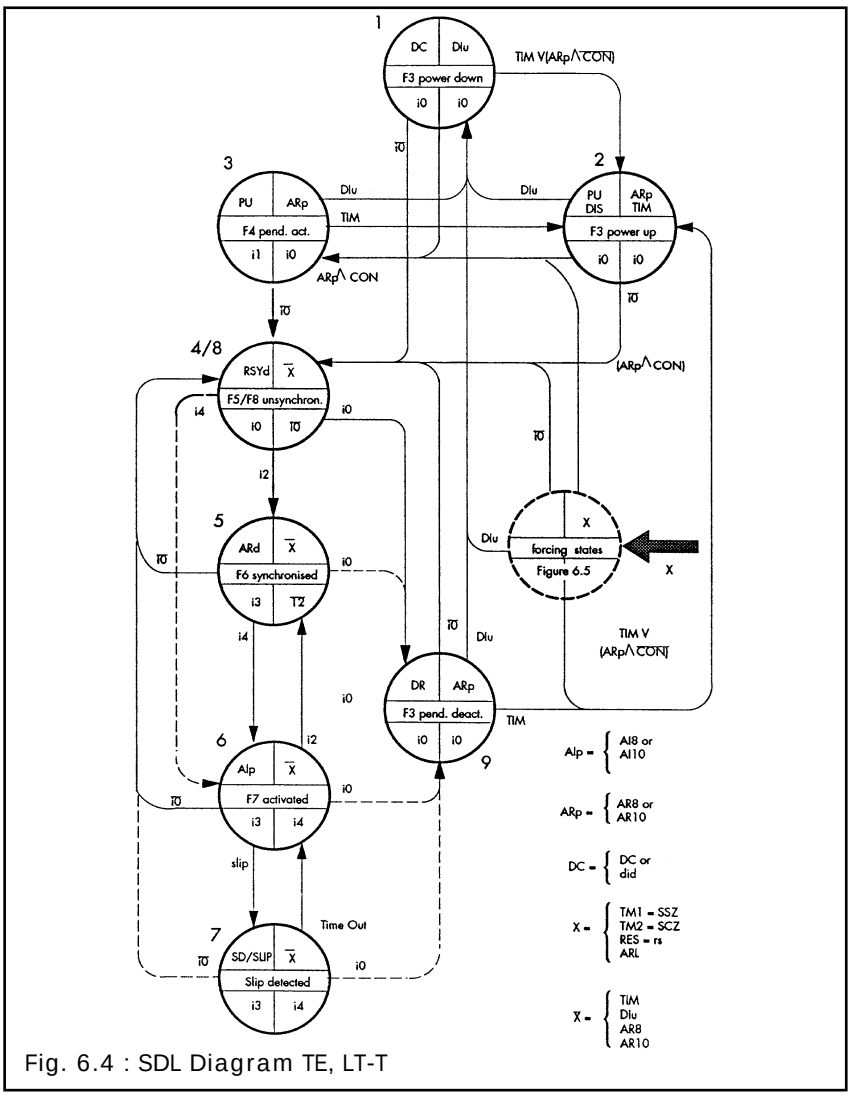


Fig. 6.4 : SDL Diagram TE, LT-T

6.3 The B-Channels on the GCI bus

The B-channels are 64 kbit/s. They are transparent channels used for a point-to-point switched connection. Idle B-channels are often forced at all binary 1.

In other interface devices, the direction of the B-channels can be reversed on the GCI data pins. This is not possible in the MTC-20172 SIC.
Also, the position of the GCI B-channels can be moved to alternative positions. This is not possible with MTC-20172 SIC.

6.4 The D-Channels on the GCI bus

The D-channel contains HDLC messages.

In NT/LT-S mode the D-channel is exchanged transparently with the S-bus.

In TE/LT-T mode there is a D-channel access protocol on the S-bus, which limits the transport of the D-channel to the S-bus, see 5.7.

The TIC bus protocol used by other divices for D-channel Access control in an intelligent NT is NOT supported, see 5.8.

6.5 The Command/ Indication (C/I) Channel

The S-bus transceiver must be put in a defined state according to CCITT I.430. This happens partially under its own control and under supervision of an external controller.

In the C/I channel, commands to and state indications from the MTC-20172 SIC are exchanged with a control element (µ-controller) or with an other uplink or downlink ISDN circuit.

The state diagram of the C/I channel, the possible commands and indications, and the internal reaction of the S-transceiver are all defined in the GCI standards, which allow a simple interconnection of uplink and downlink ISDN elements. Unfortunately, a few dialects of the C/I exist.

Moreover, some unused commands and indications can be used for other purposes (e.g.maintenance/monitoring) and can be chosen according to the component manufacturer.

In MTC-20172 SIC, two version of the C/I command channel are implemented:

1) The V* version
The C/I channel works according to the Mietec MTC-2072 SIC. It can be linked to the MTC-2071 UIC (4B3T) of MIETEC and the IEC of Siemens at the NT. The MTC-20172 SIC is fully compatible, with a few extra commands available.

2) The GCI version
The C/I channel is compatible with many other devices. It can be linked to the UID of ST/NSC and to the 2B1Q U-device of Siemens.

Compared to the V* version, GCI incorporates minor changes and additions. Some commands are coded with binary numbers differently from

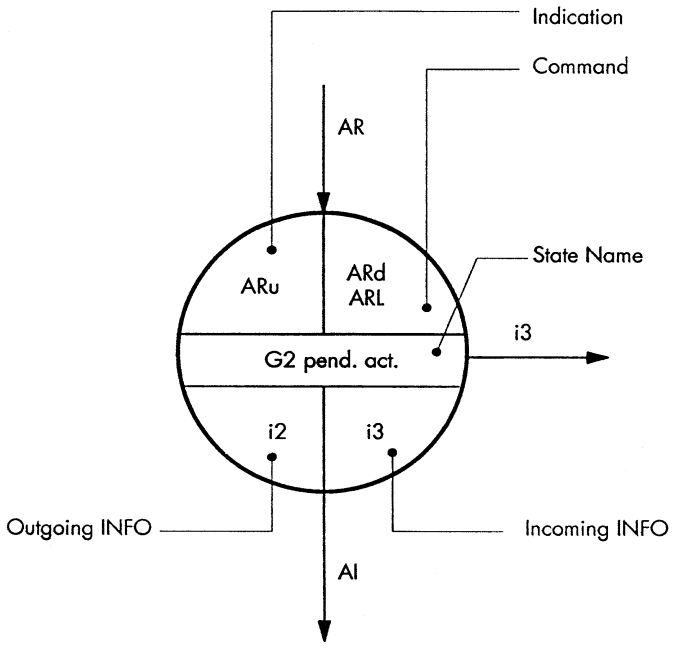


Fig. 6.5 : Explanation of Notation of the SDL Diagrams

the V*, some indications were split or added.

For information, the remainder of this section 6.5 contains:

- 6.5.1 General information of the C/I state diagrams
- 6.5.2 State Diagram for the NT position
- 6.5.3 State Diagram for the LT-S position
- 6.5.4 State Diagram for the LT-T position
- 6.5.5 The Commands and Indications of the Basic Mode
- 6.5.6 The Commands and Indications of the extended Mode
- 6.5.7 C/I Equivalence TABLE basic/extended modes
- 6.5.8 Commands and Indications For the NT Applications
- 6.5.9 Commands and Indications For the LT-S Applications
- 6.5.10 Commands and Indications For the TE/LT-T Applications

6.5.1 General Information of the C/I State Diagrams

The state diagrams exist for NT, LT-S, and the combination TE/LT-T, as explained in 6.5.2 to 6.5.4.

The STATE DIAGRAMS are shown in the Figures 6.1 to 6.5. Three examples of activation and deactivation are shown in Figures 6.7 to 6.9.

The state names use the names F1 to F8 and G1 to G4, as used by the CCITT. However, for a full functional description, the states need to be expanded into sub-states. The state diagrams are almost identical for Basic and extended Modes, the differences are minor for NT and LT-T, and mostly related to the Command/Indication use. In some cases, hidden sub-states of the Basic Mode are expanded to the improved extended Mode version.

The LT-S diagram is a simplified version of the NT state diagram. One will notice that the state numbering of the LT-S is just a sparser version of the NT-T case. The TE and LT-T diagrams are identical.

In the state diagrams, each state is represented by a circle. It contains the name, the command and indication, the incoming and outgoing INFO on the S-bus, as explained in Figure 6.1. For convenience the states are also numbered.

The commands and indications are commented in 6.5.5 to 6.5.10.

The arrows indicate events and conditions which cause state changes. The diagrams are functionally complete, but some arrows are omitted (unexpected or illegal commands), and some arrows are dashed and commented in the text for clarity.

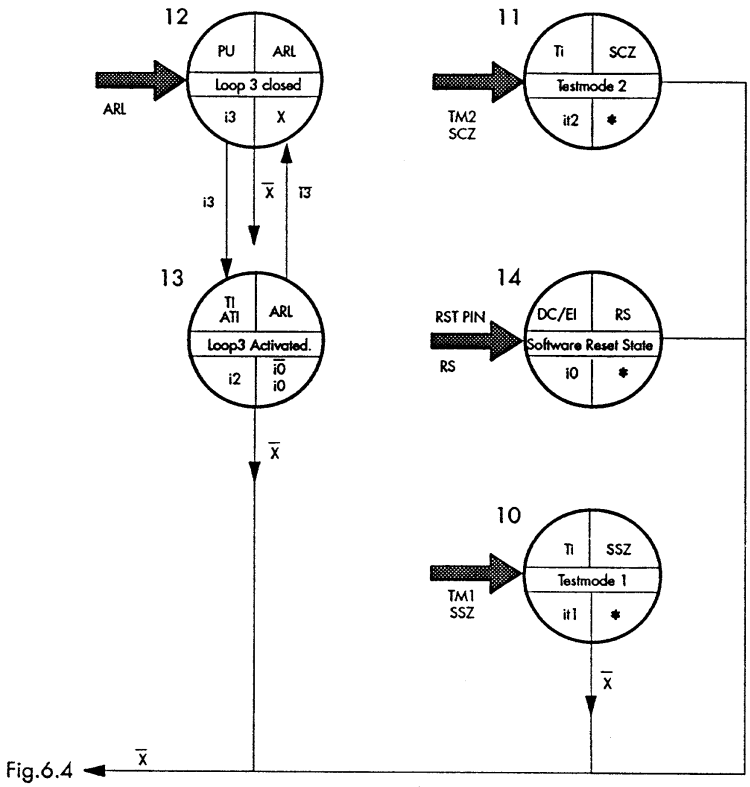


Fig. 6.6 : SDL Diagram TE/LT-T, Unconditional states, Basic Mode

Debouncing
The C/I codes are debounced to prevent accidental errors. The MTC-20172 SIC accepts a command only after it is present for 2 consecutive GCI frames. Normally, the indications from the MTC-20172 SIC should be debounced also by the receiving control unit.

Illegal Commands
The reaction of MTC-20172 SIC to illegal commands (unknown values of the command nibble) is No-Operation

Not-Logical C/I Transitions
The MTC-20172 SIC will follow the C/I-channel commands, even if they are out of sequence according to the CCITT.

6.5.2 State Diagram for the NT Position

STATE NAMES and NUMBERS

(1) G4 Pending Deactivation
This state is reached by the the unconditional "DR" deactivation request command. After a timeout of 32 ms, or 16 ms of INFO0 reception the MTC-20172 SIC goes to state (2).

(2) G4 Unacknowledged
The MTC-20172 SIC is ready to deactivate, signals "Dlu", and waits for the acknowledgement with "did"="DC", and prepares the idle state (see 6.2.4) of the GCI bus.

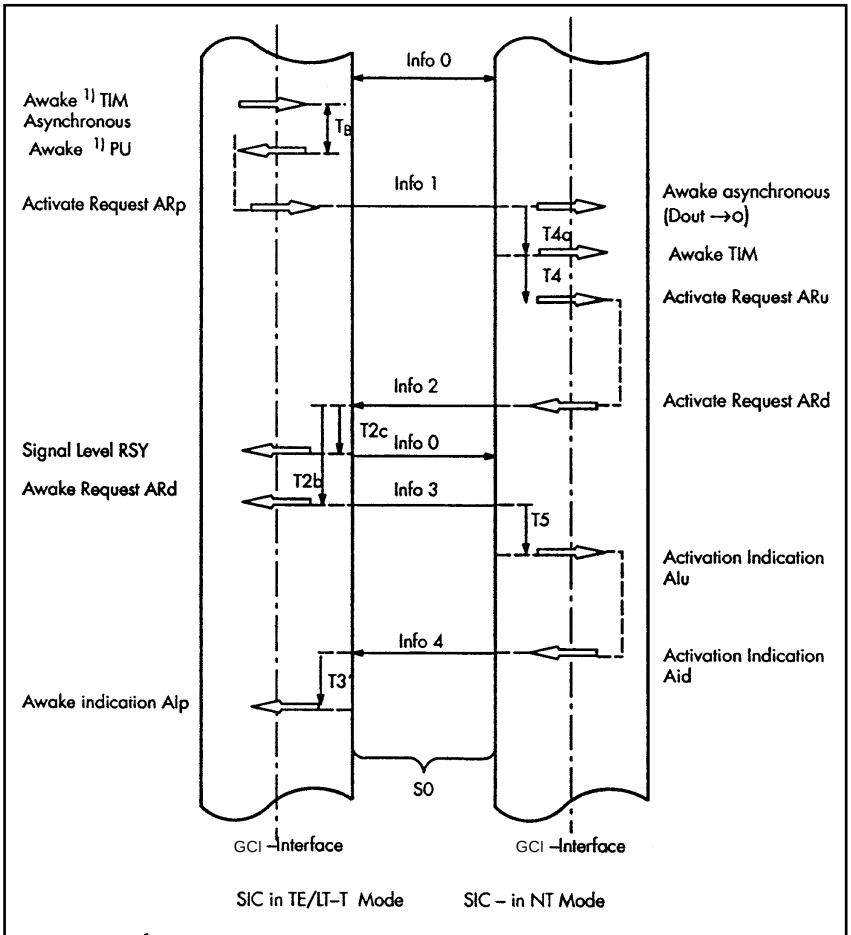
(3) G1 Deactivated
The MTC-20172 SIC is not transmitting. No signal is detected, no activation is commanded. This state is closely linked with the state 12.

(4) G1 INFO1 Detected
INFO1 detected (actually, any AMI signal). MTC-20172 SIC goes through the GCI bus activation, requesting timing signals with the "TIM" indication (see 6.2.5), then indicates "ARu". The MTC-20172 SIC waits for the the "ARd" command from uplink device (e.g. U interface) once the U-link synchronizes.

(5) G2 Pending Activation
"ARd" forces the MTC-20172 SIC to send INFO2, and to try to detect and sync on INFO3. "ARL" also activates the analog loop from TX to RX on the S-bus transceiver.

(6) G2 Synchronized
MTC-20172 SIC achieved INFO3 synchronization, MTC-20172 SIC signals "Alu" and waits for "Ald" (or AIL) to go to the G3 state. The MTC-20172 SIC signals "Alu". ARL (the loop 2 case) forces the analog loop and the receiver synchronizes on INFO2.

(7) G3 Activated (with or without loop 2)
Receiving "Ald" (or AIL) MTC-20172 SIC switches INFO2 to INFO4, provided the receiver synchronizes on INFO3: cut through of the B and D



1) Only TE, TE1, TE2, Modes

Response Times :

T_B < 4 ms
T2c = 0.2 ...0.45 ms
T2b = 4.37...5.8 ms
T3 = 0.5 ...0.75 ms
T4a < 4 ms
T4 ≤ 4 ± 0.125 ms
T5 = 0.5...1.5 ms

Fig. 6.7 : Activation Sequence Outgoing Call

channels. The MTC-20172 SIC signals "AIu". AIL (the loop 2 case) forces the analog loop and the receiver synchronizes on INFO4.

(8) G2 Unsynchronized
If the S-bus receiver loses synchronization on the incoming INFO3, it switches to INFO2 downlink transmission, and signals "RSYu". In the Basic Mode, this state is hidden in the previous state (7).

(9) Lost Framing at U-side
If the U-link loses synchronization, it indicates this with the RSYd command. Here, some fundamental difference exists between Basic and extended Modes, discussed further down under remark 11.

(10)-(11) Test-mode 1 and Test-mode 2
The unconditional commands TM1, TM2, SSZ and SCZ (or the equivalent pins TM1-, TM2-, SSZ- and SCZ-, see 4.11, 4.12) force the MTC-20172 SIC into test-mode 1 (Send Single Zeros) and test-mode 2 (Send Continuous Zeros)

(12) Reset
In the state diagrams of the Basic and extended Modes, the reset is shown differently. However, for the Basic mode, the reset state (12) is a sub-state hidden in state (3). In the MTC-20172 SIC, the split states (3) and (12) are implemented for the Basic and extended modes. INFO0 is sent and the incoming INFO is ignored.

6.5.2.1 NT State Diagram: Remarks and Implementation

Remark 1 : During the test-modes, the MTC-20172 SIC request timing with "TIM". This also applies if the test-modes are commanded via pins (see 4.11, 4.12). Indeed, without TIM the NT clocks are not activated and MTC-20172 SIC would not receive the Xtal clock.

Remark 2 : a number of non-logical commands could be received at various states of the diagram. The unexpected RSYd, AId, AIL, etc... will force the correct states, with the appropriate indications. The incorrect issuing of the deactivate confirmation command "did"="DC" will force the state (1). However, the power down of the GCI bus (clocks, frame etc, ...) can only be guaranteed if the correct "DR" is used. See 6.2.4.

Remark 3 : There are some dashed arrows in the state diagram: The device will not return to state (5) when an unexpected AR is given during state (9). The latest GCI state diagram appears to pass through the state (5) only once, all subsequent loss-of-sync events are indicated with RSYu from state (8). To simplify the MTC-20172 SIC there will be no difference between basic and extended modes, and the dashed arrows are NOT implemented.

Remark 4 : During the G4 pending deactivation state, the basic mode indicates RSYu, LSL or AIu, the extended mode indicates TIM. This difference is implemented.

Remark 5 : The "lsl" indication is deleted from the basic states. If the device receives no signal, it will go out of synchronization after only 2 missing frames. LSL is replaced by RSYu, as is done for the extended mode.

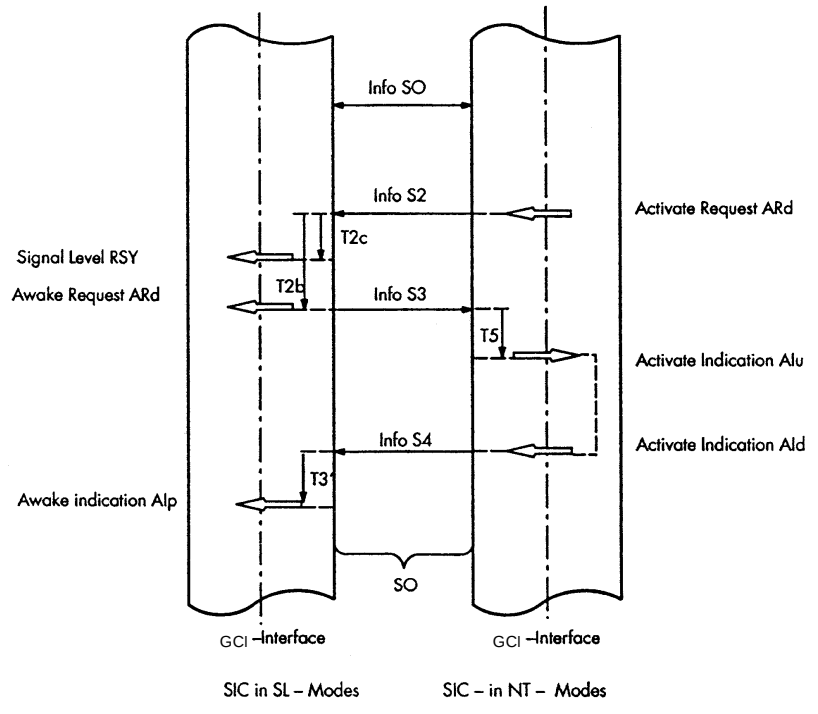


Fig. 6.8 : Activation Sequence Incoming Call

Remark 6 : The reaction of MTC-20172 SIC on the AR command is not required. However, the MTC-20172 SIC reacts on AR in state (1) as indicated.

Remark 7 : If an accidental signal on the S-bus (spike, EMC, ...) awakens the MTC-20172 SIC, which goes to state (4), the only way to return to idle, state (3), is via the normal activation and deactivation procedure.

Remark 8 : In the state (9), the extended mode always answers with RSYu; the basic mode can also signal LSL and Alu, depending of the receiver state. However, the MTC-20172 SIC suppresses the LSL and Alu indication during state (9).

Remark 9 : The command TM2 (test-mode 2) exists only for the extended mode. It could be considered illegal for the basic mode and result in NO-Operation. However, the implementation extends the TM2 command to the basic mode.

Remark 10 : The "ei" indication, i.e. both RSTB and SCZ- pin active, is valid for the extended mode. The indication during active RSTB pin is TIM.

Remark 11: In state (9), the MTC-20172 SIC sends INFO2 for ALL NT modes. This is the most logical response. It keeps the S-bus active and synchronous, with the B and D-channels downlink idle at all zero. Uplink the B-channels are transparent, but the D-channel will be idle, because the E-channel downlink is forced to all zero. Note that the multiframing S/Q-channel will work also during INFO2!.

Remark 12 : In the loop modes under command of ARL and AIL the receiver sees the INFO2/4 of its own transmitter as uplink signal instead of actual INFO3. It ignores activity detection on the real S-bus. This bus will activate normally, because the loop is a transparent loop 2. The TEs could even try to send LAPD messages, but they are not terminated correctly.

6.5.3 State Diagram for the LT-S Position

The state diagram of the LT-S is a sparse version of the NT. The same numbers and names are used. The Figure of the state diagram is organized with identical states on the same position, with deletion of missing states. The states (4), (6) and (9) do not exist in the LT-S case.

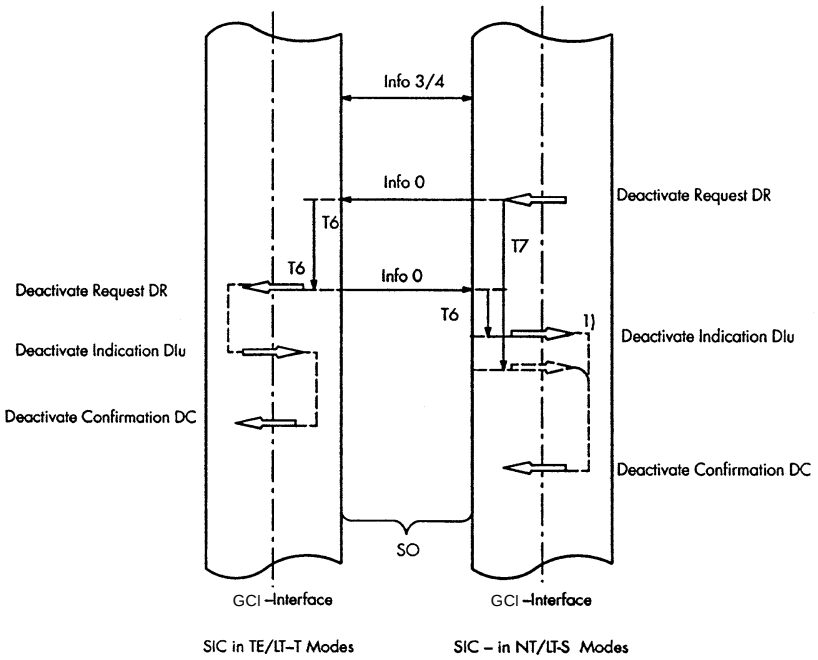
State Names and Numbers

(1) G4 Pending Deactivation
This state is reached by the the unconditional "DR" deactivation request command. After a timeout of 32 ms, or 16 ms of INFO0 reception, the MTC-20172 SIC goes to state (2).

(2) G4 Unacknowledged
The MTC-20172 SIC is ready to deactivate, signals "Dlu", and waits for the acknowledgement with "did"="DC", and prepares the internal idle state (see 6.2.4). However, the GCI bus will not go to idle.

(3) G1 Deactivated
The MTC-20172 SIC is not transmitting. No signal is detected, no activation is requested. This state is closely linked with the state 12, which is only defined for the extended mode.

(5) G2 Pending Activation
There are two ways to arrive in this state:



Response Times :
T6 = 16 ± 1 ms
T7 = 32 ± 2 ms
1) These events are alternative

Fig. 6.9 : Desactivation Sequence

Either :
a) INFO1 is detected (actually any AMI signal). MTC-20172 SIC indicates "ARu". Without waiting for the "ARd" command, the MTC-20172 SIC activates the S-bus (INFO2).

Or :
b) "ARd" forces the MTC-20172 SIC to send INFO2. "ARL" also activates the analog loop from TX to RX on the S-bus transceiver.

In both cases a) and b), the INFO2 forces the TEs to respond with INFO3. The MTC-20172 SIC tries to synchronize and goes to state (7) when this happens. In loop case the receiver sees INFO2/4.

(7) G3 Activated (with or without loop 2)
MTC-20172 SIC achieved INFO3 synchronization, MTC-20172 SIC signals "AIu" and goes to "cut-through" by sending INFO4. ARL (the loop 2 case) forces the analog loop and the receiver synchronizes on INFO2/4.

(8) G2 Unsynchronized
If the S-bus receiver loses synchronization on the incoming INFO2/3/4 in state (7), it switches to INFO2 downlink transmission and signals "RSYu". In the basic mode, this state is hidden in the previous state (7).

(10)-(11) Test-mode 1 and Test-mode 2
The unconditional commands TM1, TM2, SSZ and SCZ force the MTC-20172 SIC in test-mode 1 (Send Single Zeros) and test-mode 2 (Send Continuous Zeros)

(12) Reset
In the state diagrams of the reset is shown differently. However, for the basic mode, the reset state (12) is a substate hidden in state (3). In the MTC-20172 SIC, the split states (3) and (12) are implemented.
INFO0 is sent and the incoming INFO is ignored.

6.5.3.1 LT-S State Diagram: Remarks and Implementation

Some remarks are the same as those listed under the NT description.

Remark 1 : During test-modes, the MTC-20172 SIC indicates "TIM", see Remark 1, NT case.

Remark 2 : In all states, all listed LT-S commands can be issued. Even the DC command without the normally preceding DR is allowed. Indeed, the strict power-down of the bus is not needed. The MTC-20172 SIC simply goes to an internal low-power state. See also 6.2.4.

Remark 3 : During the G4 pending deactivation state, the basic mode indicates RSYu, LSL or AIu, the extended mode indicates TIM. This difference is implemented in the SIC.

Remark 4 : The "lsl" indication is deleted from the basic mode states. If the device receives no signal it will go out of synchronization after only 2 missing frames. LSL is replaced by RSYu, as is done for the extended mode.

Remark 5 : The command RES (soft reset) exists only for the extended mode.

Remark 6 : The command TM2 (test-mode 2, binary "0011") exists only for the extended mode. It could be considered illegal for the basic mode, and result in NO-Operation. However, the implementation extends the TM2 command to the basic mode.

Remark 7 : In the loop modes under command of ARL and AIL, the receiver sees the INFO2/4 of its own transmitter as an uplink signal instead of the actual INFO3. It ignores activity detection on the real S-bus. This bus will activate normally, because the loop is a transparent loop 2. The TEs could even try to send LAPD messages, but they are not terminated correctly.

Remark 8 : The reaction of MTC-20172 SIC on the AR command from state (1) is not required. However, MTC-20172 SIC reacts on AR in state (1) as indicated.

6.5.4 State Diagram for the TE/LT-T Position

(See also fig. 6.6).

State Names and Numbers

(1) F3 Power Down
The MTC-20172 SIC is not transmitting. The receiver activity detector is on, but no signal is detected; no activation is commanded.

Clock outputs (TE case only) are inactive, unless the ENCK- pin is forced low. In TE, the power-down is maximum.

(2) F3 Power Up
The TIM command request is given and MTC-20172 SIC answers with PU, unless the CON pin is inactive, see 4.11, 4.12. Then DIS is indicated.

If the ARp command is given with the CON pin inactive this state is also reached.

(3) F4 Pending Activation
The command AR8 or AR10 force MTC-20172 SIC to send INFO1, as long as INFO0 is received in return. Software must implement the INFO1 timeout, i.e. timer T3 of CCITT I.430.

Any AMI downlink signal (=not INFO0) stops the INFO1 uplink. The detection time is 50 µs when INFO2 comes in. MTC-20172 SIC goes to state (4).

If the ARp command is given with the CON pin inactive, the MTC-20172 SIC goes to state (2).

(4)/(8) F5/F8 unsynchronized
This state can be reached from all other states, when some activity is detected downlink after idle, or when synchronization is suddenly lost but with signal still assumed present. MTC-20172 SIC tries to synchronize. MTC-20172 SIC sends INFO0. If it was sending INFO1 in state (3), it will cease doing so.

(5) F6 Synchronized
MTC-20172 SIC achieved INFO2 synchronization. Automatically it responds with INFO3. It waits for INFO4. Reaching this state from the power down state (1) takes less than 6 ms, when MTC-20172 SIC is activated by INFO 2/4 from an uplink NT or LT-S.

(6) F7 Activated
MTC-20172 SIC achieved INFO4 synchronization. Automatically it responds with INFO3. It is now in cut-through. The transition from (5) to (6), or from INFO2 to INFO4, takes less than 0.5 ms.

7) Slip detected
This state is hidden in the basic mode. The Slip detection is normally send for 0.5 ms (i.e 4 times) on the C/I channel. The internal elastic buffer is adjusted, which causes a number of bytes to be lost or repeated in the B-channels, and bit errors on the D-channel.

(8) F8 lost framing
This state (basic mode) is now merged with the state (4).

(9) F3 Pending Deactivation
When the MTC-20172 SIC sees INFO0 (after 16 ms) it signals "DR", deactivation request. When receiving INFO again it reactivates to state (4). To reactivate the S-bus from the TE side, MTC-20172 SIC must first be put in state (1) or (2) with Dlu or TIM.

(10)-(11) Test-mode 1 and Test-mode 2
The unconditional commands TM1, TM2, SSZ and SCZ force the MTC-20172 SIC in test-mode 1 (Send Single Zeros) and test-mode 2 (Send Continuous Zeros)

(12)-(13) Loops
The loops are a special case: It is a loop 3 type. It links the transmitter output to the receiver, but only internally, without transmitting signal on the uplink S-bus.

The ARL command forces the transmitter to send INFO3. The receiver activity detector stays linked to the downlink signals. The rest of the receiver sees the looped signal. If the receiver is NOT synchronous yet the MTC-20172 SIC is in state (12). Once the receiver is synchronous MTC-20172 SIC will be in state (13). B and D-channels are now looped with a fixed delay.
The indications differ between basic and extended modes, and are shown on Figures 6.5 and 6.6.

If the activity detector sees a downlink signal, it warns with a special indication "ATI" (basic mode) or "RSY" (extended mode).

(14) Reset
The RESET state is an idle state. Analog parts of the S-bus transceiver are off. Incoming INFO2/4 is ignored. Clocks are supplied. Digital outputs are active.

MTC-20172 SIC will reach the RESET state when forced via the RST- pin or the reset C/I command.

6.5.4.1 TE/LT-T State Diagram: Remarks and Implementation

Remark 1: RST- pin effect and implementation. The RST- pin force the device in state (1) (F3 Power Down). It forces the device in state (14) (RESET). Both devices go to the RESET state when commanded via the C/I RESET command.

The RST- pin and the RESET command always force the MTC-20172 SIC to the RESET state.

Remark 2: The CON pin must only be tested to send INFO1 on the S-bus. If INFO2 or INOF4 is received downlink, INFO3 is sent without checking the CON condition.

Remark 3: Some of the transitions in the state diagram will never occur. They are marked with dashed lines. Implementation is simplified. Indeed, loss of synchronization will be seen first, long before the confirmation of the loss of signal (i.e. INFO0) is valid. However, a long timeout for INFO0 validation is implemented.

6.5.5 The Commands and Indications of the Basic Mode

The MTC-20172 SIC implements the full list of C/I codes of the basic mode as indicated below:

Table 6.1: The Original Basic Mode Commands and Indications

mode	Terminal equipm. TE/LT-T		network termin. NT		line termination LT-S	
C/I code	Downstr Indicat.	Upstr. Command	Downstr Command	Upstr. Indicat.	Downstr Command	Upstr. Indicat.
0000	DR	TIM	DR	TIM	DR	-
0001	-	RS	[RES]+	(lsl)!	scz	(lsl)!
0010	sd	SSZ	SSZ	-	SSZ	-
0011	dis	[TM2]+	[TM2]+	-	[TM2]+	-
0100	RSY	scz	RSYd	RSYu	-	RSYu
0101	-	-	-	-	-	-
0110	ei	-	-	ei	-	-
0111	PU	-	-	-	-	-
1000	ARd	AR8	ARd	ARu	ARd	ARu
1001	-	AR10	-	-	-	-
1010	ti	ARL	ARL	-	ARL	-
1001	ati	-	-	-	-	-
1100	AI8	-	AId	AIu	-	AIu
1101	AI10	-	-	-	-	-
1110	-	-	AIL	-	-	-
1111	DID	DIu	DID	DIu	DID	DIu

Comments:

[]+: The command "testmode2" = TM2 (=scz) and "soft reset" = RES (=RS) are added at unused positions to remove differences between modes.

!: The lsl indication was deleted, because its effect is equivalent with the RSYu indication.

The C/I of the basic mode are not according to the final GCI standard. The commands which differ functionally from the final GCI are put in lower case.

For C/I names which differ only for the upstream and downstream indication, are added lower case "d" and "u".

The detailed explanation of each command is given below in 6.5.8 to 6.5.10.

6.5.6 Extended Mode Commands and Indications

The MTC-20172 SIC implements the full list of C/I codes of the extended mode as indicated below:

Table 6.2: Extended mode commands and indications

mode	Terminal equipm. TE/LT-T		network termin. NT		line termination LT-S	
C/I code	Downstr Indicat.	Upstr. Command	Downstr Command	Upstr. Indicat.	Downstr Command	Upstr. Indicat.
0000	DR	TIM	DR	TIM	DR	TIM
0001	RES	RES	RES	-	RES	-
0010	TM	TM1	TM1	-	TM1	-
0011	SLIP	TM2	TM2	-	TM2	-
0100	RSY	[scz]+	RSY	RSY	-	RSY
0101	-	-	-	-	-	-
0110	-	-	-	[ei]+	-	-
0111	PU	-	-	-	-	-
1000	AR	AR8	AR	AR	AR	AR
1001	-	AR10	-	-	-	-
1010	ARL	ARL	ARL	-	ARL	-
1001	-	-	-	-	-	-
1100	AI8	-	AI	AI	-	AI
1101	AI10	-	-	-	-	-
1110	AIL	-	AIL	-	-	-
1111	DC	DI	DC	DI	DC	DI

[]+: The commands "scz" (=TM2) and "ei" were added to remove differences between modes.

This list follows the stable GCI version of the names, abbreviations and positions of the C/I codes.

The detailed explanation of each command is given below in the 6.5.8 to 6.5.10.

The NT-STAR C/I channel issue:
The MTC-20172 sic does not support the functional combination of the c/i codes in the nt-star configuration.
If two SICs in an NT are put in STAR configuration, see 5.6.1, the C/I channels will coincide on the GCI bus.

The DOUT pin is configured as open drain (see TABLE 3.3), thus no electrical problems exist. However, the indications of both SICs will be wired-ANDed on the bus, bit by bit, and the result is incorrect. E.g., when one branch of the STAR has no TE, then it is not synchronous and it signals "RSY", while the other branches try to indicate "AI". The combination is still "0100", which is "RSY".

NOTE: Some devices use the CEB pin, which links all devices in the NT-STAR, to allow the AI uplink indications in the C/I channel, when at least one device reaches the G3 Activated state (5). The MTC-20172 SIC does not support this.

6.5.7 C/I Equivalence Table

The C/I codes are identical for all functional modes. The C/I codes for the extended mode (GCI) are more logically organized and kept identical over the different modes.

IDENTICAL commands and indications which use the same abbreviation are marked as a single C/I in UPPER CASE. IDENTICAL C/I have sometimes the same abbreviation except for the letters "u" and "d" (uplink an downlink). Those are marked as single C/I in Mixed Case.

All commands and indications which have different abbreviation but same meaning and on the same position have the equal sign "=".

The basic command in lower case, the extended command in upper case.

All commands and indication which are different but on the same position are marked with the star sign "*", C/I for basic mode at the left.

Unused positions are marked "-". Some positions are NOT USED BY ONE DEVICE ONLY; then they are marked with both "-" and "*".

Some of the mixed command and indication codes (i.e. used * unused) are merged in the MTC-20172 SIC. This is marked with "&". The command used in one device is allowed in the unused position of the other device. Some mixed indication (i.e. used * unused) can also be merged: The lsl indication is deleted, the ei indication will also appear in the NT extended mode.

** Marks functional differences (17 in total).*

& Marks functional differences which can be merged for both modes.

Table 6.3: Equivalence table, Basic versus Extended Mode

mode	Terminal equipm. TE/LT-T		network termin. NT		line termination LT-S	
C/I code	Downstr Indicat.	Upstr. Command	Downstr Command	Upstr. Indicat.	Downstr Command	Upstr. Indicat.
0000	DR	TIM	DR	TIM	DR	- *TIM
0001	- * RES	rs=RES	-& *RES	(lsl)*&-	scz*RES	(lsl)*&-
0010	sd * TM	ssz=TM1	ssz=TM1	-	ssz=TM1	-
0011	dis*SLIP	-& *TM2	-& *TM2	-	-& *TM2	-
0100	RSY	scz* &-	RSYd	RSYu	-	RSYu
0101	-	-	-	-	-	-
0110	ei * -	-	-	ei * &-	-	-
0111	PU	-	-	-	-	-
1000	ARd	AR8	ARd	ARu	ARd	ARu
1001	-	AR10	-	-	-	-
1010	ti * ARL	ARL	ARL	-	ARL	-
1001	ati * -	-	-	-	-	-
1100	AI8	-	AId	AIu	-	AIu
1101	AI10	-	-	-	-	-
1110	- * AIL	-	AIL	-	-	-
1111	did=DC	Dlu	did=DC	Dlu	did=DC	Dlu

6.5.8 Command and Indications for NT Applications

Table 6.4.a : MTC-20172 SIC C/I : NT overview

NT	Downstr Command	Upstr. Indicat.		Downstr Command	Upstr. Indicat
0000	DR	TIM	1000	ARd	ARu
0001	-& * RES	(lsl)*&-	1001	-	-
0010	ssz=TM1	-	1010	ARL	-
0011	-& * TM2	-	1001	-	-
0100	RSYd	RSYu	1100	AId	Alu
0101	-	- ++	1101	-	-
0110	-	ei * &-	1110	AIL	-
0111	-	-	1111	did=DC	Dlu

++ MAIC is NOT implemented.
** Marks functional differences (4 in total).*
& Marks functional differences which are merged for both devices.

6.5.8.1 Commands (Downstream) in NT Mode

Table 6.4.b : MTC-20172 SIC commands (DS) NT

0000	DR #	Deactivate Request	Forces MTC-20172 SIC to deactiv. the S-bus (=INFO0) followed by Dlu and did=DC
0001	*RES # &	RESET	Forces MTC-20172 SIC to soft reset, extended mode only, MTC-20172 SIC accepts it in basic mode (merged)
0010	ssz # = TM1	TEST-MODE 1	Forces MTC-20172 SIC to test-mode 1, sending single zeros
0011	*TM2 # &	TEST-MODE 2	Forces MTC-20172 SIC to test-mode 2, extended mode only, sending continuous zeros, command is extended to the basic mode of the MTC-20172 SIC
0100	RSYd	Resynchon-izing down	The U-interface is not synchronous, MTC-20172 SIC sends INFO2 {or SCZ}, see remark 1 below
1000	ARd	Activation Request down	MTC-20172 SIC forced to INFO2 transmission, receiver indicates the S-bus reaction
1010	ARL	Activat. req with S-loop	INFO2 transmission on the S-bus test loop2 switched (transparent loop)
1010	AId	Activation Indication	INFO4 transmission, normally only after Alu indication is received
1010	AIL	Activ. Indic. with S-loop	INFO4 transmission test loop2 switched (transparent loop)
1111	did= DC	Deactivate Confirmation	Deactivation confirmation, entering the power down state, INFO0 sent, critical timing to halt the clocks, see 6.2.4

** Marks functional difference;*
& Marks differences that are merged.
 # Unconditional commands, which force an unambiguous state.

Remark 1: When the U-interface is resynchronizing, the basic mode sends Continuous Zeros, the extended mode sends INFO2. MTC-20172 SIC will send INFO2.

Remark 2: During loops, the MTC-20172 SIC simply ignores the incoming INFO3 from the S-bus. The receiver synchronizes on looped INFO2/4.

6.5.8.2 Indications (Upstream) in NT Mode

Table 6.4.c : MTC-20172 SIC indications (US) NT

0000	TIM	Timing Request	The MTC-20172 SIC requires GCI clocks and also Master clock input, if no crystal is used.
0001	*lsl &	Lost Signal Level	No receive level, indication deleted, replaced by RSYu
0100	RSYu	Resynchron-izing	The S-bus receiver tries to synchronize
0101	---------	---------	---------
0110	* ei &	Error Indication	RSTB and SCZ- pin both low simultaneously Only in basic mode, but is extended to theextended mode
1000	ARu	Activation Request up	INFO1 received (actually any AMI signal)
1100	Alu	Activation Indication up	Receiver synchronized on INFO2/3/4 (INFO3 normally, INFO2/4 in loop)
1111	Dlu	Deactivation Indication	Timer (32 ms) expired, or INFO0 received (16 ms) after DR (deactiv. request)

** Marks functional difference;*

& Marks differences that are merged.

"lsl" and "ei" are NOT implemented.

Remark 1: The "lsl" indication is deleted from the command list and replaced by RSYu. If the devicedoes not receive a valid signal, e.g. no signal, it will go to the loss of sync state, and it signals loss of sync.

Remark 2: The "ei" indication is extended to the the extended mode, without any problems.

Note also comments in REMARK [10] in 6.5.2.1.

6.5.9 Commands and Indications LT-S

Table 6.5.a : MTC-20172 SIC C/I LT-S

LT-S	Downstr Command	Upstr. Indicat.		Downstr Command	Upstr. Indicat
0000	DR	- *TIM	1000	ARd	ARu
0001	scz*RES	(lsl)*-&	1001	-	-
0010	ssz=TM1	- -	1010	ARL	-
0011	-& *TM2	- -	1001	-	-
0100	-	RSYu	1100	-	Alu
0101	-	-	1101	-	-
0110	-	-	1110	-	-
0111	-	-	1111	did=DC	Dlu

** Marks functional differences (3 in total).*

& Marks functional differences which are merged for both devices.

6.5.9.1 Commands (Downstream) In LT-S Mode

Table 6.5.b : MTC-20172 SIC commands (DS) LT-S

0000	DR #	Deactivate Request	Forces MTC-20172 SIC to deactiv. the S-bus (=INFO0) followed by Dlu and did=DC
0001	*RES #	RESET	Forces MTC-20172 SIC to soft reset, extended mode has "scz" meaning for basic mode
	*scz #	Send Continu-ous Zeros	Forces MTC-20172 SIC to test-mode 2, extended mode has RESET meaning for extended mode
0010	ssz # = TM1	TEST-MODE 1	Forces MTC-20172 SIC to test-mode 1, sending single zeros
0011	*TM2 #	TEST-MODE 2	Forces MTC-20172 SIC to test-mode 2
1000	ARd	Activation Request down	INFO transmission, first INFO2, then INFO4 once receiver is synchronous
1010	ARL	Activat. req	INFO transmission on the S-bus with S-loop test loop2 switched (transparent loop)
1111	did= DC	Deactivate Confirmation	Deactivation confirmation, entering the power down state, INFO0 sent

** Marks functional difference;*
& Marks difference that can be merged.
 # Unconditional commands, which force an unambiguous state.

Remark 1: During loops the MTC-20172 SIC simply ignores the incoming INFO3 from the S-bus. The receiver synchronizes on looped INFO2/4.

Remark 2: The TM2 command could be extended to the basic mode.

Remark 3: RES and scz commands cannot be merged

6.5.9.2 Indications (Upstream) In LT-S Mode

Table 6.5.c : MTC-20172 SIC indications (US) LT-S

0000	*TIM	Timing Request	The MTC-20172 SIC requires GCI clocks and Master clock input, extended mode only (Extention to basic mode impossible)
0001	*lsl &	Lost Signal Level	No receive level, indic. Basic mode only, indication deleted, replaced by RSYu
0100	RSYu	Resynchron-izing	The S-bus receiver tries to synchronize on incoming INFOx
0101	---------	---------	---------
1000	ARu	Activation Request up	INFO1 received (actually any AMI signal)
1100	Alu	Activation Indication up	Receiver synchronized on INFO2/3/4 (INFO3 normally, INFO2/4 in loop)
1111	Dlu	Deactivation Indication	Timer (32 ms) expired, or INFO0 received (16 ms) after DR (deactiv. request)

** Marks functional difference;* *& Marks difference that can be merged.*

Note that this list is identical to the NT indication list, except for the "ei" indication, which is not present here.

Remark 1: The "lsl" indication is deleted from the basic command list and replaced by RSYu. If the device does not receive a valid signal, e.g. no signal, it will go to the loss of sync state, and it signals loss of sync.

Remark 2: The TIM indication is used in the NT modes. However, in the LT-S modes here it is only listed for the extended mode. Because the "TIM" indication is not expected from the basic mode, it cannot be allowed it to appear in the C/I channel in LT-S modes of the MTC-20172 SIC. As the GCI bus is never shut down in LT-S modes, the timing request "TIM" is not needed.

6.5.10 Commands and indications TE/LT-T

Table 6.6.a : MTC-20172 SIC C/I TE/LT-T

TE/ LT-T	Downstr Indicat.	Upstr. Command		Downstr Indicat.	Upstr. Command
0000	DR	TIM	1000	ARd	AR8
0001	- *RES	rs=RES	1001	-	AR10
0010	sd * TM	ssz=TM1	1010	ti * ARL	ARL
0011	dis*SLIP	-& *TM2	1001	ati * -	-
0100	RSY	scz* &-	1100	AI8	-
0101	-	-	1101	AI10	-
0110	ei * -	-	1110	- *AIL	-
0111	PU	-	1111	did=DC	Dlu

General comments:

The difference between the TE and LT-T modes will be the absence of the SLIP or "sd" indications. In TE the MTC-20172 SIC generates its own clocks.

6.5.10.1 Commands (Upstream) in TE/LT-T Mode

Table 6.6.b : MTC-20172 SIC commands (US) TE/LT-T

0000	TIM #	TIMING	MTC-20172 SIC receives clocks (GCI ..)in LT-T, it must activate the clocks in TE mode
0001	rs= #	RESET = RES	Forces MTC-20172 SIC to soft reset
0010	ssz #	TEST-MODE 1 = TM1	Forces MTC-20172 SIC to test-mode 1, sending single zeros
0011	*TM2 # &	TEST-MODE 2	Forces test-mode 2, sending continu. zeros
0100	*scz # &	Send Continu. Zeros	Forces test-mode 2, sending continu. zeros
1000	AR8	Activation Request 8	Activation command, D channel priority 8/9 INFO1, unless the CON pin is not high followed by INFO3, without CON condition
1001	AR10	Activation Request 10	Activat. command, D channel priority 10/11 INFO1, unless the CON pin is not high followed by INFO3, without CON condition
1001	AR10	Activation Request 10	Activation command, D channel priority is 10
1010	ARL #	Activ. loop 3	This loop is not transparent, it is a special case, see text 6.5.4
1111	Dlu	Deactivate Indication	GCI clock can be disabled by MTC-20172 SIC together with other clocks see 6.2.4

** Marks functional difference;*

& Marks difference that can be merged.

 # Unconditional commands, which force an unambiguous state.

6.5.10.2 Indications (Downstream) in TE/LT-T Mode

Table 6.6.c: MTC-20172 SIC common indications (Downstream) in LT-T mode

0000	DR	Deactivation Request	Deactivation request via S/T-bus: state F3 reached in state diagrams
0100	*RSY	Receiver synchronising	Signal Received (INFO 2/4) but receiver not synchronous. It has a special meaning during loop test in the extended mode : It signals detection of a signal on the S-bus, while the rest of the receiver is linked to the looped S-bus signal
0111	PU	Power Up	GCI interface clocking is provided {TE?} acknowledges TIM, and other commands
1000	ARd	Activate Request downl	INFO2 is received, INFO3 send uplink, CON pin does not influence INFO3 TX
1100	AI8	Activate indication 8	INFO4 is received, INFO3 send, priority on D-channel is 8, acknowledges AR8
1101	AI10	Activate indication 10	INFO4 is received, INFO3 send, priority on D-channel is 10, acknowledges AR10
1111	did =DC	Deactivate confirmation	Clocks will be disabled in TE, see 6.2.4 MTC-20172 SIC in quiescent state

Table 6.6.d: MTC-20172 SIC indications (Downstream) Basic Mode only, TE/LT-T mode

0010	sd =SLIP	Slip Detected	The frame buffer slipped, cause is wander meaning identical to SLIP for SBCX 2081
0011	dis	Disconnected	Pin CON connected to GND, INFO1 disabled.
0110	ei	Error indication	Acknowledges that RSTB and ENCK pin both or that RS command is given
1010	ti	Testmode indication	Indicates that test mode i is commanded with "ssz", "scz", or that the receiver synchronizes on loop 3 signal after ARL
1001	ati	Awake Test indication	Indicates incoming INFOx during test modes with loop 3. Detection of signal via level detection only. This command is replaced by RSY during ARL in the extended mode

Table 6.6.e: MTC-20172 SIC indications
(Downstream) Extended Mode only, TE/LT-T mode

0001	RES	Reset	Acknowledges the RES command entering (optional in GCI spec)
0010	TM	Testmode	Acknowledges that TM1/TM2 command enters (optional in GCI spec)
0011	SLIP =sd	Slip Detected	The frame buffer slipped, cause is wander Meaning identical to "sd" for basic mode
1010	ARL	Activate Request loop	Acknowledges ARL, loop 3 closing, MTC-20172 SIC sends INFO3/4 not transparent to S-bus, receiver not synchronous on the looped signal; replaced by PU in the basic mode
1110	AIL	Activate Ind. with loop	Acknowledges ARL, loop 3 closing, MTC-20172 SIC receiver synchronous, i.e activation ind. replaced by ti in the basic mode

Comments:

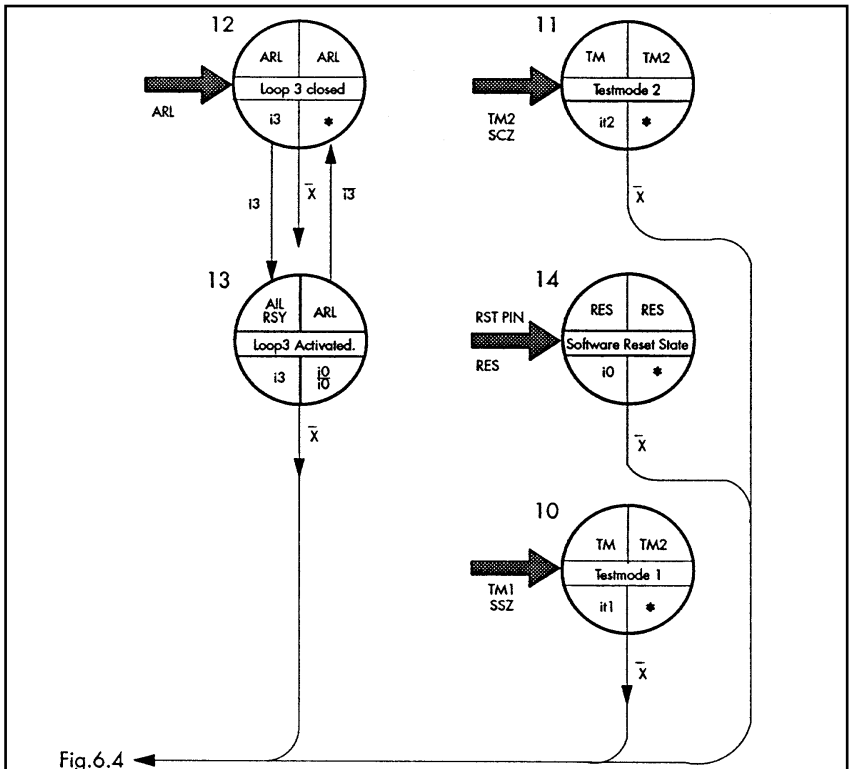
The RES indication of the extended modeis found as "ei" in the basic mode.

The "ati" indication exists only in basic mode, but the extended mode uses the RSY indication during the loop (i.e. when ARL command is given) to indicate an incoming signal.

The basic mode does not have the ARL indication, which it replaces by PU during the loop (i.e. when ARL command is given).

The basic mode has only one indication “ti”, which is equivalent to either TM or AIL of the extended mode.

The subtle differences between the indications are seen in the State diagrams explained in 6.5.4, Figures 6.4, 6.5 and 6.6.



RSY : Activation of S-BUS in state “Loop3 Activated”.
X : forcing command ARL, TMI , TM2, RES
it1: single pulses at
4 kHz, alternating polarity
it2: test signal 96 kHz
i3 : loop signal only internally

Fig. 6.10 : SDL Diagram TE, LT-T, Unconditional states, extended mode

6.6 M-Channel + MX + MR : Physical Layer

The M-channel is a byte oriented channel, where each byte is presented by the transmitter and acknowledged by the receiver. The bytes are organized in messages.

Use and Compatibility

The M-channel should not be used in the basic mode. The M-channel is an additional feature.

For compatibility, a special BUSY bit is present in the M-channel, see 7.4.

Content of the M-Channel

The content is explained in chapter 7. The length of all MTC-20172 SIC messages is 2 bytes.

Half-Duplex Operation

The GCI standard allows the two M-channels to work only half-duplex. This half duplex operation is implemented to reduce the internal buffer capacity of the M-transceiver.

Thus, the MTC-20172 SIC can NOT send and receive the M-channel simultaneously. After each received message (of exactly 2 bytes) the M-transceiver changes direction, if a message must be sent in the opposite way.

Bidirectional Operation: Message priority

The M-transceiver gives priority to outgoing messages, to avoid internal buffer overflow.
The controller on the M-channel must acknowledge the messages leaving the MTC-20172 SIC before the MTC-20172 SIC is able to receive any new message.

Failing to acknowledge the message from the MTC-20172 SIC results in a DEADLOCK: the MTC-20172 SIC waits for the acknowledge of the outgoing message, and in the meantime refuses to acknowledge the next incoming message.

Operation Speed

The operation speed of the M-channel is variable: the devices can delay the transfer by retarding the acknowledge or by delaying the delivery of subsequent bytes.

The MTC-20172 SIC will adjusts to any lower speed on the channel, but it can transfer one M-channel byte in 250 µs (both RX and TX). However, this speed is limited by the half duplex operation, and by the idle which must follow each double byte message.

6.6.1 M-Channel Activity

The M-channel can only work when the GCI interface has its clock and frame running.

6.6.2 M-Channel Format, Bit and Byte Numbering Convention

The M-channel is a byte oriented channel. Bytes (also called octets) are transmitted in ascending numerical order. Within a byte the most significant bit is transmitted first.

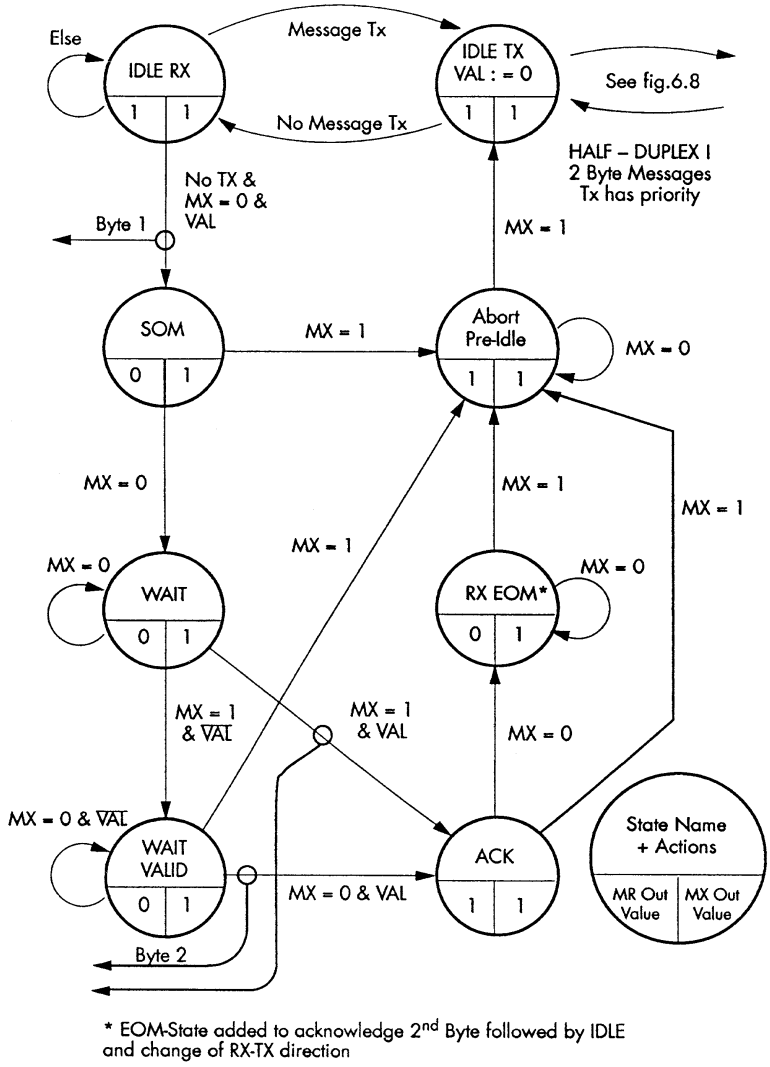


Fig. 6.11 : SDL Diagram of the M-Channel Receiver

The four most significant bits of the first message byte represent a general address, discussed under 7.2.

6.6.3 Byte Transfer Procedure

To transfer a message composed of subsequent bytes on the GCI M-channel, each byte is presented by the transmitter and acknowledged by the receiver. For that purpose, the two M-channels (to and from the MTC-20172 SIC) have separate handshake bits, the MR and MX bits in the B1*-channel, see Figure 4.2.

The MX bit signals the presence of new information in the M-byte, the MR bit signals the reading of the information by the receiver.

State Diagram and Examples of Message Passing

Simplified state diagrams of the coupled receiver and transmitter and examples of message exchanges can be found in Figures 6.10 to 6.13. Comments on the state diagram are found in 6.6.4.

6.6.3.1 Idle M-Channel

The procedure start from idle, where MX and MR are both inactive at 1. The M-channel content during idle is invalid and should be at FFh.

However, the idle value received by the MTC-20172 SIC is ignored.

On the other hand, for compatibility reasons, the fifth bit of the idle M-channel leaving the MTC-20172 SIC in the LT-T or TE mode is the BUSY bit, see 7.4.

6.6.3.2 Start Of Message (SOM) and First Byte Transfer

From the idle state, a start of message transmission is initiated by the sender with the transition of the MX-bit from inactive to the active state. The data to be transmitted are passed in the M-byte starting in the same frame as the MX-bit activation.

In normal operation the first byte must be kept constant in the M-channel until the SOM is acknowledged by the receiver.

6.6.3.3 Acknowledge of the SOM and First Byte

On detection of the SOM, the receiver will read the M-byte. It will acknowledge reception, provided that identical data were seen in the M-channel during two consecutive frames.

To acknowledge SOM and the first byte, the MR bit goes from inactive to the active state, remaining there, until:

1) a next byte is transferred, with MX indication, see next ;
2) an EOM is signalled by the transmitter;
3) the receiver wants to abort the message.

6.6.3.4 Further Byte Transfers

In the case of the second byte transfer, the sender must detect the transition of the MR bit of the receiver from inactive

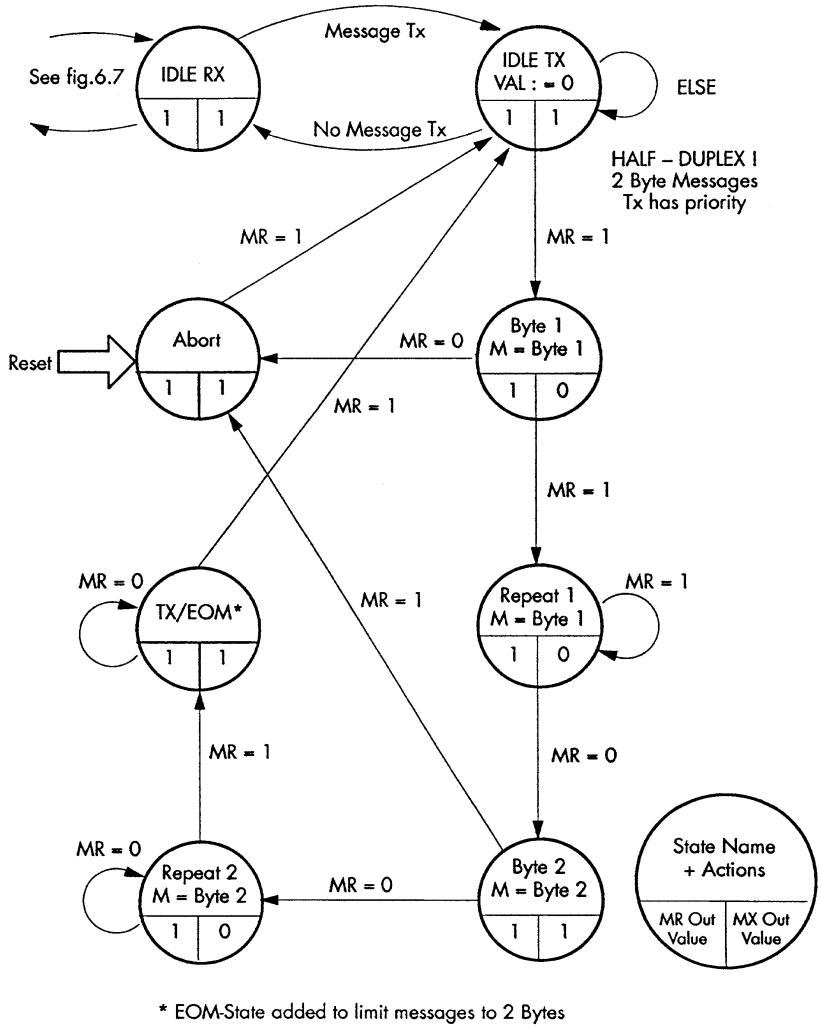


Fig. 6.12 : SDL Diagram of the M-Channel Transmitter

to the active state (negative edge 1 to 0), before transmitting the second byte, see previous paragraph.

For subsequent bytes, the sender may start further byte transmission after detecting a transition of the MR bit of the receiver from active to inactive, (positive edge 0 to 1).
The sender indicates a new byte of information by the transition of the MX bit from active to inactive, for exactly one frame. The data is valid in the same frame. In the next frame, the MX bit goes from inactive to active, and the valid data are repeated. The data are thus repeated for minimally two frames. The sender repeats the data in all subsequent frames until the receiver returns the MR bit inactive, to acknowledge the data (see next section), or to abort the message.

6.6.3.5 Further Byte Acknowledgement

Each subsequent byte (signaled by MX going high for one frame, see previous) is acknowledged by the receiver once it has seen two consecutive identical bytes in the M-channel. It acknowledges this by putting the MR inactive (at 1) for exactly one frame. In the next frame the MR bit must go back to active.

6.6.3.6 End of Message (EOM)

Once the sender has received the acknowledge of the last byte, it changes the content to FFh, moves the MX to inactive and keeps it inactive for at least two frames.

6.6.3.7 Acknowledge of EOM

After the EOM of the sender, the receiver acknowledges the EOM by putting MR bit in the inactive state for at least two frames, keeping it there until the transmitter goes active again.

6.6.3.8 Sender Not Ready

If the sender is not ready (second byte or subsequent), the MX bit will be kept in the active state and the channel byte stays constant.

6.6.3.9 Receiver Not Ready

If the receiver is not ready for the first byte, it keeps the MR in the inactive state.

If the receiver is not ready for the second byte, it refuses to acknowledge the bytes by keeping MR in the active state.

6.6.3.10 IDLE Forced From Sender

If the first byte is never acknowledged, i.e. MR staying at 1, the sender can force the M-channel and MX to IDLE.

If the reception of a subsequent byte is not (or not yet) acknowledged by the

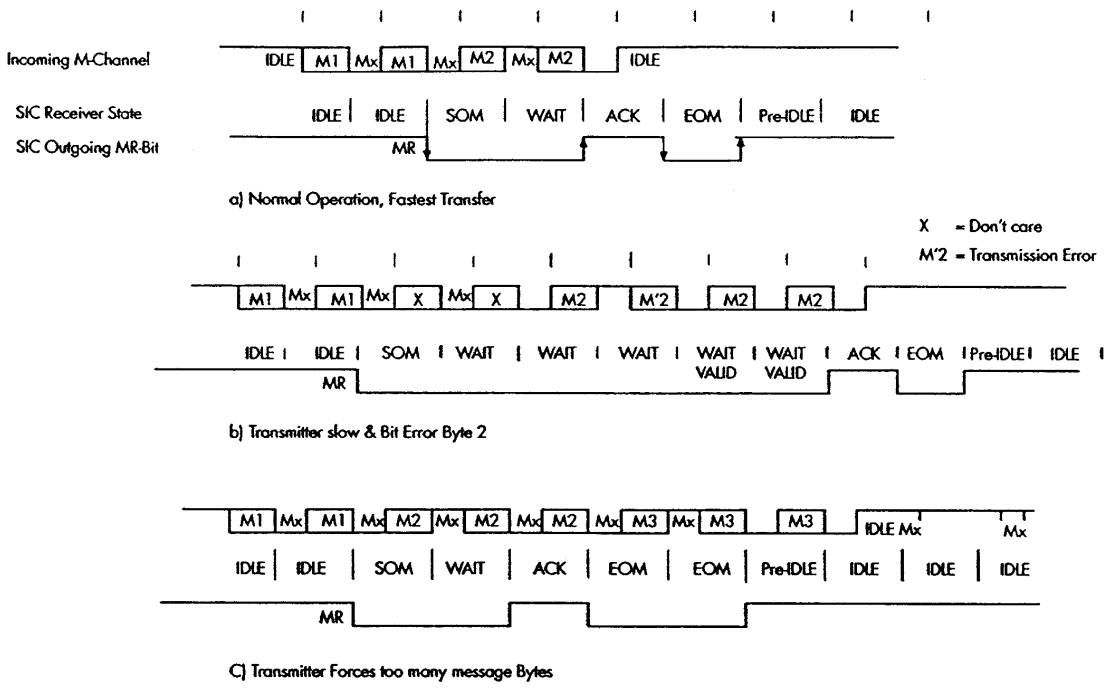


Fig. 6.13 : Examples of Received M-Channel Messages

receiver (MR is staying active at 0), the sender can put the M-channel and MX to IDLE. The receiver should return MR to inactive.
The last byte or even the complete message are never really legally acknowledged by the receiver.

6.6.3.11 Abort Request From Receiver

The receiver can abort a message after the SOM acknowledge or any subsequent byte acknowledge by forcing MR inactive for at least two frames.

The MTC-20172 SIC aborts a message ONLY when it is forced in HARD RESET.

6.6.3.12 Acknowledge Abort

The sender acknowledges the abort request by entering the idle state.

6.6.4 Comments on the MTC-20172 SIC M-transceiver State Diagrams

The state diagrams for the MTC-20172 SIC are presented in Figures 6.5 and 6.6.

The receiver oversamples the M-bytes and considers them valid after two identical values.

The receiver changes states between the M-byte reception and the sending of the outgoing MR bit.

The transmitter changes states synchronous with the MX, MR reception and interpretation.

The diagrams are derived from the GCI standard, with the following simplification:

- The RECEIVER NOT READY states are deleted;
- The SENDER NOT READY states are deleted;
- The receiver and sender work in half-duplex;
- The outgoing message has priority over a received message;
- The receiver refuses messages longer than two bytes; the EOM RX state is added to the state diagram to acknowledge a second byte, and to go to idle followed by a change of the half-duplex direction, if a message must be sent;
- The sender sends messages of only two bytes followed by idle; the EOM TX state is added to send exactly two bytes, followed by idle;
- Sender or receiver timeouts are not implemented.

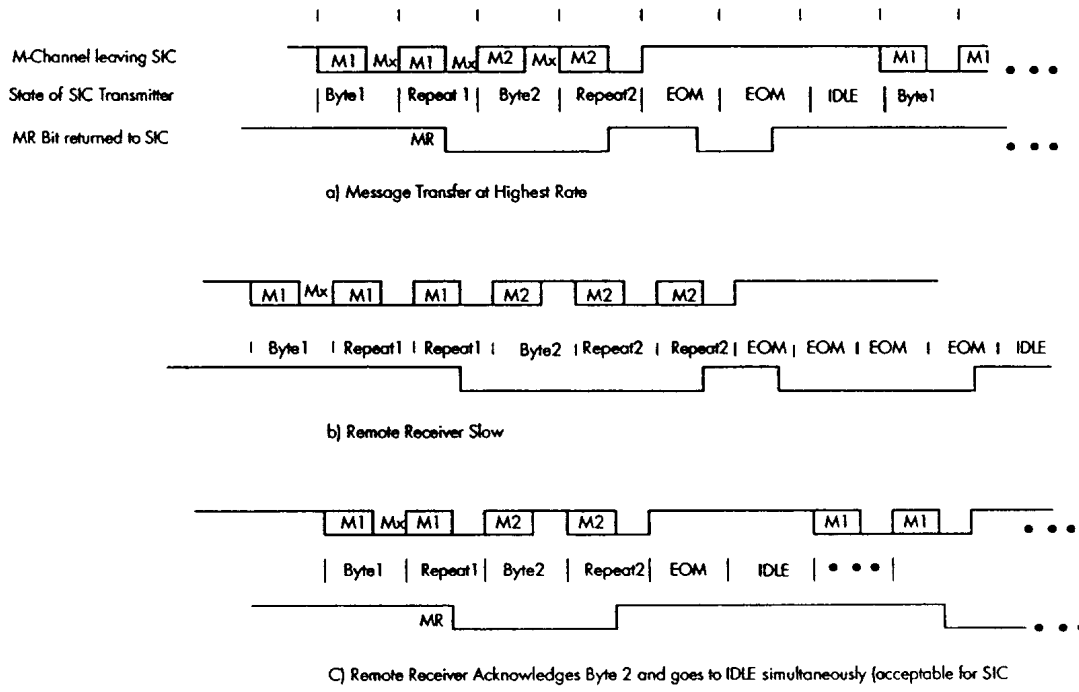


Fig. 6.14 : Examples of Received M-Channel Messages

7. M-Channel Messages and Registers

7.1 Introduction

In the MTC-20172 SIC, the M-channel is used for the transfer of operation and maintenance information:

1) The TRANSFER of system related registers (S and Q channel of the multiframing);
2) The WRITE and READ operations of internal registers;

- Test and identification registers;
- Mode registers, overriding the default state, changing the modes without having to change straps;
- Control registers to change auxiliary inputs and outputs;
- Status registers, e.g. alarm and error monitoring;

3) The transfer of the BUSY indication (TE/LT-T) for the D-channel access is present in ALL TE/LT-T modes.

M-channel use is not required for basic mode compatible operation:
In the basic mode, the use of the M-channel is not necessary. However, it is available to allow access to the multiframe S and Q bits, and to access some internal registers with additional features.

If the monitor channel is not used, the MTC-20172 SIC is forced in a default state after reset, as defined in 7.7.

7.2 M-Channel Receiver and Transmitter

In the MTC-20172 SIC, the M-channel transceiver works half-duplex, with message length 2 bytes. The M-channel goes to idle after every message, to allow a change of direction in the MTC-20172 SIC M-transceiver. The layer 1 operation of the M-channel is described in 6.6.

7.3 General Content of M-Channel Messages

In the MTC-20172 SIC, the M-channel messages are limited to double bytes.

The first nibble of the message is a general address, defined in the GCI standards. In the MTC-20172 SIC this address nibble must be one of these values:

0001b, used to access S and Q channel bits.
1000b, used to read or write internal registers.
All other values are ignored.

7.4 M-Channel, Basic Mode

In the MTC-20172 SIC in TE/LT-T, the M-channel will always contain the BUSY indication in the downlink M-channel, see 5.7.3. This happens during the IDLE and when the channel is active transferring messages.

The BUSY bit is always present, even when the Identification Register or the Version Number Register are transferred.

7.5 S And Q Channel M-Channel Messages

The MTC-20172 SIC uses double byte messages to transfer the S and Q bits.

7.5.1 S/Q M-Channel Messages, MTC-20172 SIC in NT/LT-S With Multiframing

Downlink
byte 1: 0 0 0 1 1 1 1 1
byte 2: S11 S12 S13 S14 1 1 1 1

Uplink
byte 1: 0 0 0 1 1 1 1 1
byte 2: Q1 Q2 Q3 Q4 1 1 1 1

The downlink messages to the MTC-20172 SIC contain the S11 to S14 bits.
These bits are sent continuously downlink on the S-bus via the S-channel. When the value changes by an M-channel message, the new values are put in the S-channel synchronously with the multiframe. (A double buffer is used inside the MTC-20172 SIC).

In uplink direction, the MTC-20172 SIC sends the received Q1 to Q4 bits each time they change.

7.5.2 S/Q M-Channel Messages, MTC-20172 SIC In TE/LT-T With Multiframing

Downlink
byte 1: 0 0 0 1 BUSY 1 1 1
byte 2: S11 S12 S13 S14 BUSY 1 1 1

Uplink
byte 1: 0 0 0 1 1 1 1 1
byte 2: Q1 Q2 Q3 Q4 1 1 1 1

In downlink direction, the MTC-20172 SIC sends the received S11 to S14 bits each time they change. The BUSY bit is permanently present in the M-channel.

The uplink messages to the MTC-20172 SIC contain the Q1 to Q4 bits.

These bits are sent continuously uplink on the Q-channel, provided that multiframing synchronization is found. When the Q values changes via the M-channel message, the new values are put in the Q-channel synchronously with the multiframe. (A double buffer is used inside the MTC-20172 SIC).

7.5.3 S/Q M-Channel Messages, MTC-20172 SIC Multiframing Disabled

If Multiframing is not enabled, the MTC-20172 SIC ignores the content of the incoming S/Q messages and will not generate outgoing S/Q messages. Multiframing enabling: see 5.9.2 and 7.7.3.

7.6 Internal Register M-Channel Messages

All internal register operations on the M-channel are double byte messages. Both READ and WRITE operations are possible. After every operation, the M-channel must go idle again.

Concatenation of double byte messages could result in errors. Messages which are aborted are ignored. The MTC-20172 SIC debounces the different bytes of the message.

A WRITE operation is a one way message, acknowledged only via the MR bit, see 6.6. However, every register can be read. A READ operation results in an answer, delivering the content.

The READ operation causes the two directions of the M-channel to be logically dependent! After the READ message to the MTC-20172 SIC, the incoming M-channel must return to IDLE. The M-transceiver in the MTC-20172 SIC gives priority to the delivery of the CONTENT and/or S/Q messages, before it can handle the next incoming (READ/WRITE or S/Q) message.

7.6.1 Write Operation

For a Write operation, the double byte messages is as follows:

To SIC	byte 1:	1	0	0	0	X	ADR2	ADR1	ADR0
	byte 2:	CONTENT (MSB first to LSB last)							

No outgoing message in reaction to the WRITE.

The second nibble is the address of the internal register, limited from 1 to 6 in the MTC-20172 SIC. The write addresses must differ from 0000, otherwise the READ operation is assumed.

7.6.2 Read Operation and Content Message

For a Read operation, the double byte messages is as follows:

To SIC	byte 1:	1	0	0	0	0	0	0	0
	byte 2:	X	X	X	X	X	ADR2	ADR1	ADR0

The second nibble is all zero for an internal READ operation. The fourth nibble is the address of the register, from 0 to 6.

The answer is the Content message, two bytes as follows:

From SIC	byte 1:	1	0	0	0	BUSY	ADR2	ADR1	ADR0
	byte 2:	CONTENT (MSB first to LSB last)							

The second nibble is the address of the internal register, with the BUSY bit present in TE/LT-T modes.

The second byte contains the content of the register, again with BUSY present in the fifth position in TE/LT-T modes.

7.7 Detailed Bitmap of the Internal Registers

Table 7.1: Register Bitmap of MTC-20172 SIC

Ad	name	sent first							sent last	
0h	I.D.	0	1	1	0	BUSY	0	0	0	READ
1h	V.N.	0	0	0	0	BUSY	X	X	X	READ
2h	CONF	BT1/SC	BT0	DEX1	DEX0	BUSY	MFE	LTS/T	DELT	RD/WR
3h	OUT	AUX4b1	AUX4b0	AUX3b1	AUX3b0	BUSY	TEST	AUX1b1	AUX1b0	RD/WR
4h	IN1	AUX4	AUX3	----	AUX1	BUSY	MOD2	MOD1	MOD0	READ
5h	IN2	(TEST)	SCLK	XTR4	XTR3	BUSY	XTR2	XTR1	XTR0	READ
6h	PERF	S1/Qb1	S1/Qb2	S1/Qb3	S1/Qb4	BUSY	SLIP	MFR	BER	READ
7h	TEST	device test only; not used in normal operation								RD/WR

7.7.1 Identification Register; READ Only; Address 0h

I.D.	0	1	1	0	BUSY	0	0	0

Device I.D. according to the GCI specification.

7.7.2 Version Number Register; READ Only; Address 1h

V.N.	0	0	0	0	BUSY	X	X	X

The version number of the device, starting at 00h.

7.7.3 Configuration Register; WRITE and READ; Address 2h

CONF	BT1/SC	BT0	DEX1	DEX0	BUSY	MFE	LTS/T	DELT
Reset	0	0	0	0	0	0	0	0

BT1/SC	BT0	: bus type selection in NT/LT-S mode
0	X	: bus type according to BUS pin; value at reset;
1	0	: bus type = Adaptive; BUS pin ignored, pin usable as I/O;
1	1	: bus type = Fixed; BUS pin ignored.
		SCLK pin (basic mode) disabled in TE/LT-T mode X3 pin (extended mode) disabled in TE/LT-T mode
0	X	: SCLK/XTR3 pin is enabled, basic mode compatible at Reset;
1	X	: SCLK/XTR3 is disabled, to simplify clock selection logic.
DEX1	DEX0	: Common Echo Bus mode selection (NT/LT-S)
0	X	: DE/CEB bus operates according to DEX pin, value at reset;
1	0	: DE/CEB bus not active; DEX pin ignored;
1	1	: DE/CEB bus driven and sensed; DEX pin ignored.

Busy: READ only bit, present for compatibility at TE/LT-T. Must be written at 0, writing BUSY at 1 triggers test-modes.

MFE: Multiframing enable if 1; Reset value is 0; Enabling is the OR function of this bit, and other inputs, see 5.9.2.

LTS/T: Select LTS/T mode in extended mode; LT-S mode if at 1, LT-T mode if at 0. After reset put in LT-T mode, to avoid incorrect behaviour on multipoint T-bus.

Delt: Delay trimming: compensate 650 ns on the fixed bus sampling in the NT, and on the TE/LT-T transceiver roundtrip . Effect identical to the XTR4 pin, see 5.4.3. If both DELT and XTR4 are active the compensation is doubled to 1300 ns. Reset at 0.

7.7.4 Output Register; WRITE and READ; Address 3h

OUT	AUX4b1	AUX4b0	AUX3b1	AUX3b0	BUSY	TEST	AUX1b1	AUX1b0
Reset	0	0	0	0	0	0	0	0

AUXib1	AUXib0	: Configure the AUX4, AUX3 and AUX1 input/output pins
0	0	: The AUXi pin works as listed in 4.11 and 4.12
0	1	: The AUXi pin is tristate and usable as input.
1	0	: The AUXi pin is driven low.
1	1	: The AUXi pin is driven high.

(Note: The use of the AUXi pins as generic inputs of outputs will collide with their standard use as inputs. EXAMPLE: one can use AUX1 as extra output or input. However, the pin AUX1 has the function DEX in LT-S modes.
The signal on AUX1 will therefore enable and disable the DE-bus, unless DEX is disabled via CONF register.)

Busy: READ only bit, present for compatibility. Must be written at 0, writing BUSY at 1 triggers test-modes.

Test: Must be written at 0, writing TEST at 1 triggers test-modes.

7.7.5 IN1 and IN2 Registers; READ Only; Address 4h and 5h

IN1	AUX4	AUX3	------	AUX1	BUSY	MOD2	MOD1	MOD0
IN2	(TEST)	SCLK	XTR4	XTR3	BUSY	XTR2	XTR1	XTR0

The bits represent the binary level of the input pin. All value are sampled asynchronously at the moment of the CONTENT message is assembled. The BUSY bit is also present here for compatibility.

7.7.6 Performance Register; READ Only; Address 6h

PERF	S1/Qb1	S1/Qb2	S1/Qb3	S1/Qb4	BUSY	SLIP	MFR	BER

The S1/Qbi bits are the received multiframe channel bits, sampled synchronously with the multiframing on the S-bus.

The BUSY bit is also present here for compatibility.

SLIP: SET when a slip occurred in LT-T mode, RESET after being read.

MFR: Indicates Multiframing synchronization if at 1, in TE/LT-T.

BER: SET each time the BER pin goes low, RESET after being read.

7.8 M-Channel Operation Messages Overview

Table 7.2: M-Channel Message Overview

	To the SIC				From the SIC	
	READ message		WRITE message		CONTENT mess.	
register name	Byte 1	Byte 2	Byte 1	Byte 2	Byte 1	Byte 2
Identification	80h	00h	--	-	80h	content
Version Number	80h	01h	--	--	81h	content
Configuration	80h	02h	82h	content	82h	content
Output	80h	03h	83h	content	83h	content
Input1	80h	04h	(test only)		84h	content
Input2	80h	05h	(test only)		85h	content
Performance	80h	06h	--	--	86h	content
Test	(test only)		(test only)		(test only)	
S/Q channel	--	--	1Fh	S/Q	1Fh	S/Q

7.9 Reset of the M-Channel Transceiver

At reset, the M-channel transceiver is forced to the idle state. All message bytes are put to idle, the MX and MR bits are forced to 1, aborting any ongoing message.

8. Loops, Test-Modes, System Tests

Overview. Five different types of test situations are provided for:

8.1 Test of the Device on the Wafer before Bonding.

8.2 Test of the Single Packaged Device.

8.3 Equipment Tests, ISDN loop tests, Acceptance Test.

8.4 System tests, for characterization of all modes.

The tests outlined in 8.3 and 8.4 are system tests, performed by the user - they are not used to test proper device operation prior to shipment. They are documented here as a user guide only.

8.1 Wafer-Test of the Device

A simplified version of the test for packaged devices allows a coarse rejection of defective devices. As this is used only for initial screening during production test, it is not specified further here.

8.2 Packaged Device Test

Complete RAM and functional test, using test patterns and a special test mode in which the device is forced to speed up the checking.
Beside digital test, the following functional analog tests are performed (information only, subject to change):

- The power consumption NT and TE modes
- The crystal oscillator (start and range),
- The PLL and DPLL ranges;
- The S-bus Driver amplitudes;
- Receiver and activity detector sensitivity;
- Receiver AGC.
- Receiver synchronization.

8.3 Equipment Tests, ISDN Loop-Tests, Acceptance Test.

These are mainly functional tests, described here to assist the evaluation of the device in a real application. A number of loops and test signals are used.

8.3.1 Test of the Device on the Assembled DSP Board

This is a check of the correct behaviour on the PCB, with more detailed diagnostics used for maintenance and repair. Functional testing of some pins of the device can be done via the M-channel.

Test-modes can force special signals on the S-bus: The test signals SSZ, SCZ, TM1, TM2 can be forced with C/I commands, or in the NT via dedicated input pins. The signal level and frequency correctness of the assembly can be checked.

In the NT, in is possible to force the UIC into sending a special test signal, by giving it the "ei" indication. The "ei" can be forced as output of the MTC-20172 SIC (see 6.5.8.2) by pulling both RSTB and SCZ- (located at the SCLK pin) low.

Other test can done with functional loops, either internal or external. An external functional loop can validate the complete equipment.

An external loop at the S-bus allows complete confidence test of the equipment, including the external S-bus devices (protection, ...). This works only in NT/LT-S modes, with the adaptive bus timing.

The internal loops allow signals (B-channel and D-channel) to traverse the digital part and a major part of the analog part of the MTC-20172 SIC.

If faulty behaviour of the external loop is found, the internal loops or normal (half duplex) signal transfers can pin-point the position of the fault.

In TE mode, no external loop test is available. The best way to do a functional test of the MTC-20172 SIC in TE mode, is to couple it to an "reference" NT and loop signals at the NT position. The SIC does not allow the loop3 test in an EXTERNAL mode.

8.3.2 ISDN Loops and Other Tests of the Complete Equipment

The standard CCITT I.430 loop-tests can be performed, via the command interface. LOOP2 in NT/LT-S, LOOP3 in TE/LT-T.

To test installed NT/LT-S equipment including the actual S-bus, the test-mode Send Continuous Zeros can be used to force an easily detected 96 kHz on the cabling.

The test signal of the UIC in the NT can also be forced by pulling RSTB

and SCZ- pins of MTC-20172 SIC low. MTC-20172 SIC will send the "ei" indication to the UIC, which responds with the test signal.

The BER pin or the BER bit in the internal performance register can be used to detect occasional bit errors. In the NT, this could be a simple LED indication.

8.4 System Tests, for Characterization of all Modes.

To characterize MTC-20172 SIC, a number of system tests can be performed:

8.4.1 PLL and DPLLs

All frequencies must be put at maximal relative ranges. All frequency jumps or jitter (e.g. XTLI from the MTC-2071 UIC) can be tested.

In LT-T, the correct locking of the SCLK should be checked, and also the handling of slip between the local GCI clock and the S-bus timing.

8.4.2 State Machines of the C/I Codes

Normal behaviour and incorrect commands.

8.4.3 M-Channel

Operation of the M-channel transceiver: MX and MR bits, protection against single byte errors in the messages, etc...

Scan and drive of all inputs and outputs, enabling and disabling all functions.

8.4.4 D-Channel Access Protocol

Correctness, fairness, advance of the RDY signal.

8.4.5 Echo Channel and Echo Bus

Speed of the integrated pull-up. Error-rate. Correctness in the 22 pin package version, where the DE and DEX pins are NOT available, but active internally.

8.4.6 S-bus Receiver

Complex reflection on all cables in TE/LT-T short bus.

Adaptive bus timing: Synchronization, loss of sync.

Fixed bus timing: complex superposition of signals in NT/LT-S mode short bus.

Line attenuation range in point-to-point.

DPLL locking.

Minimal Impedance when no local VDD on MTC-20172 SIC.

Balanced operation: longitudinal balance, in the presence of the disturbing signals specified by CCITT. E.g. a 200 kHz interfering signal, with amplitude 100 mVpp (peak to peak) is applied as specified in CCITT I.430 8.6.2.1.

8.4.7 S-bus Input to Output (TE/LT-T)

Jitter, delay, operation in multipoint bus (short bus, extended bus).

8.4.8 Power-down in NT and TE

Power saving. Reliable behaviour even when GCI bus is not shut-down according to spec.

8.4.9 Power-up in NT and TE

S-bus Activity detection. GCI bus activation. No deadlock.

9. Electrical, Physical and Environmental Specifications

Related documents:
See chapter 11.

9.1 Absolute Maximum Ratings

Absolute Maximum Ratings are those parameter limits above which permanent damage to the integrated circuit may occur. It is not implied that more than one of these conditions can be applied simultaneously. The maximum ratings are specified at an ambient temperature of 25 °C ± 50 °C (unless specified otherwise) and with ground connected.

- min/max VDD supply voltage, relative to ground potential.
  Min -0.3 V, Max 7.0 V.

- limits for all digital inputs and outputs:

Max voltage	VDD+0.5 V
Min voltage	-0.5 V
Max current (Latch-up)	50 mA (at 80 °C)

- maximum power dissipation:
  200 mW.

- Storage Conditions:
  Temperature should be in the range -55 °C to 110 °C.
  In case of IC deliveries in dry bag, the conditions of time and humidity during storage are specified in Mietec spec 16650.
  In case of IC deliveries not in dry bag, the conditions for a maximum storage period 2 years are as follows :

Ambient Temperature (°C)	Relative humidity (%)
20	80
30	70
40	60
50	50

During testing, output terminations shall withstand a short circuit to either ground or VDD for up to 0.5 second, with 1 minute between events.

9.2 Transient Energy Capabilities: ESD and LATCH-UP

See 10.2.2.

9.3 Thermal Data

The junction to ambient thermal resistance RthA when mounted on a horizontal printed board in still air is less than 60 °C/W for the 22DIL and 90 °C/W for the 28 PLCC package. The ambient temperature when testing the device on ATE equipment shall be raised in function of the test time as to guarantee the same chip temperature as on board level at 70 °C ambient.

9.4 Recommended Electrical Operating Conditions

Unless otherwise specified, the characteristic limits for the static and dynamic characteristics apply over an operating ambient temperature of 0 to +70 °C, and for applied voltage ranges, relative to GND, as follows:

VDD = 5 Volt +/- 5%
IDD = 40 mA max.

9.5 Static Characteristics.

See also the related documents, chapter 11.

9.5.1 Power Supply.

Table 9.1: Static Characteristics of the Power Supply

SYMBOL	PARAMETERS	TEST COND.	MIN	TYP	MAX	UNIT
VDD	power supply	S-bus open	4.75		5.25	V
ICC	supply current	no external load		10	13 #	mA
ICC	supply current	INFO4, 50Ω bus		14 *		mA
ICC	supply current	INFO2, 50Ω bus		18	21 &	mA
ICC	supply current	INFO2, shorted bus		23	28 &	mA
ICC	supply current	power-down, clocks running			3	mA
ICC	supply current	power & clock down			0.3	mA

Remark: supply current when DCLK runs at 512 KHz

 # Maximal total supply current = 13 mA, with INFO2 as output signal with a maximal (100%) mark density, digital inputs at VDD or VSS, digital outputs unloaded, S-bus outputs unloaded.

** To the supply current the S-bus driver current must be added! Typical total supply current will be less than 14 mA, during active periods of the component (RX and TX both ACTIVE), while sending INFO4, with a normal (50%) mix of marks and zeros, on the nominal S-bus impedance.*

& INFO2 (= 46 to 48 Marks per S frame) requires 8 mA ICC, to drive a 7.5 mA differential current in the nominal impedance of 200Ω with 1.5 V amplitude (transformed with 2:1 ratio). If the MTC-20172 SIC S-bus outputs are driving a shorted bus an output current limitation of 13.3 mA (worst case) is active and the MTC-20172 SIC will consume an extra current of maximally 15 mA.

9.5.2 Static Characteristics Of Digital Inputs.

Digital Inputs are TTL compatible:

Table 9.2: Static Electrical Characteristics, Digital Inputs

SYMBOL	PARAMETERS	TEST COND.	MIN	TYP	MAX	UNIT
VIL	low level input V				0.8	V
VIH	high level input V		2.0			V
IIL	low level input leakage current	Vin = 0V	-0.01			mA
IIH	high level input leakage current	Vin = 5V			0.01	mA
CIN	input capacitance			1.1	10	pF

9.5.3 Static Characteristics of Digital Inputs.

Table 9.3: Static Electrical Characteristics, pull-up resistors

	Internal pull-up resistance				
pin name	MIN	TYP	MAX	UNIT	Presence (para. 3.5)
XTR4	66	100	150	kΩ	Permanent
AUX1, AUX3 AUX4, XTR0	33	50	75	kΩ	Mode Dependent
DOUT	12.5	20	30	kΩ	Mode Dependent

The current of the integrated pull-up devices must be added to the IIL current.

9.5.4 Static Characteristics of Analog S-bus Inputs.

Table 9.4: Static Electrical Characteristics, outputs

PARAMETERS	TEST COND.	MIN	TYP	MAX	UNIT
DC impedance	VDD = 5V ± 5%	350	500		kΩ
DC Input Current	indiv. input			10	µA
DC Common Mode V (Output)	DC current =0	-5%	VDD/2	+5%	V
AC Input Impedance	VDD = 5V 5%			25	pF
AC Impedance Not powered	VDD=0V, note 1		20		kΩ
AC Input V, not powered	VDD=0V, note 1	-0.5		+0.5	V
AC Differential Inp. Volt.	VSS = 5V 15%			2.6	V
AC Input Voltage Range	see note 2	0		VDD	V
AC Common Mode rejection	see note 3	32			dB
AC Input Voltage Range to reject Common Mode AC	see note 3 indiv. input	1.2		VDD - 1.2	V
AC Input Imped. Mismatch	see note 3				

Note 1: Input voltage range and impedance when not powered
When the MTC-20172 SIC is not powered, the AC input voltages are limited to ± 0.5V by the protection devices of the inputs. External resistance (typ. 10 kΩ) must be added in series with each input to limit the current as discussed under 5.3.3.

Note 2: AC input signal range
The AC S-bus input signal can drive each individual input to 0V and VDD provided that no large unwanted common mode signal is present. Common mode noise can not be rejected, unless the limits of note 3 are respected.
The worst case situation happens when one input would be kept at a constant DC voltage (with a capacitor) and the S-bus signals (times the transformer ratio of 1:2) plus the same DC offset are present on the other input. The input stage sees the wanted differential signal plus a common mode signal with half the amplitude of the differential signal.
(Note that in this case, the S-bus transformer is also asymmetrically terminated, which affects the symmetry of the S-bus)

Note 3: AC input signal range with common mode rejection
The differential input stage is symmetrical. Therefore, it will reject unwanted AC common mode noise signals with 32 dB, provided that each individual input pin never goes below 1.2V or above (VDD - 1.2V). E.g. an unwanted 1.1V (peak) common mode signal added to a wanted 1.5V (peak) differential S-bus signal will be sufficiently rejected. Normally the common mode signal is already removed to a large extent by the input transformer and other external devices, which present a low-ohmic path to ground or a high series impedance; see 5.3.1.

9.5.5 Static Characteristics Of Analog S-bus Outputs.

Table 9.6: Static Characteristics of the S-bus Outputs

PARAMETERS	TEST COND.	MIN	TYP	MAX	UNIT
External Series Impedance	SIC side		70		Ω
Output Impedance MARK	on S-bus	20 #			Ω
Output Impedance ZERO	SIC side	30 *			kΩ
Output Not powered (VDD=0V)	SIC side	30 &			kΩ
Output Current	SIC side		± 7.5	± 13.3	mA
differentially	(load imped.:)		(200)	(0)	Ω
Output Voltage on S-bus	S-bus 50Ω	675	750	825	mV
(magnitude)	Fig 5.3	90	100	110	%
Output Voltage on S-bus	S-bus 400Ω	675	1000	1200	mV
(magnitude)	Fig 5.4	90	133	160	%
Open Circuit Output Voltage	SIC side	2025	2100	2175	mV
(magnitude)	VDD = 5V	135	140	145	%

 # Total impedance of series resistors, transformer(2:1) + SIC drivers.

** External transformer (minimally 2.5 kΩ) in parallel on the S-bus.*

& Guaranteed if S-bus differential signals are below 1.2 V peak.

9.6 Dynamic Characteristics.

Dynamic timing parameters are shown in Figures 9.1 to 9.4.

9.6.1 Master Clock

The timing parameters and signal thresholds are shown in Figure 9.1.

The master clock has a nominal period of 130.2 ns.

Table 9.7: Dynamic Characteristics of the Master Clock

PIN	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
XTLI	Tr, Tf	Rise and Fall Time			12	ns
XTLI	Tp	Clock Period	65			ns
XTLI	Tw (high)	Clock Width High	20			ns
XTLI	Tw (low)	Clock Width Low	20			ns
XTLO #	Tr, Tf	Rise and Fall Time			12	ns
XTLO #	Tw (high)	Clock Width High	55.1		75.1	ns
XTLO #	Tw (low)	Clock Width Low	55.1		75.1	ns
XTLI/O#	frequency	Master clock freq.		7.68		MHz
XTLI/O#	freq error	clock deviation	-100		+100	ppm

 # Characteristics at the XTLO output when the on chip free running crystal oscillator is used. The load on XTLO is maximum 30 pF.

However, the clock period is allowed to be modulated, as could be needed to adjust its frequency. In all applications (NT/TE/LT) the period can be shortened to as low as 65 ns, provided that the width (high or low) never descends below 20 ns.
Note that all jitter on the master clock is observed on the S-bus transmit signals, see 5.2.5, and on all other derived clocks.

9.6.2 DCL Output Clock (TE) and Other Derived Clock Signals

The DCL, SCLK and the other derived clock signals on pins XTR3, XTR2, and XTR1 have a duty cycle between 1:2 and 2:1. Among those signals there is an unknown phase relation. Also the phase relation of SCLK and XTRi to the master clock and the GCI clock signals is not specified or can not specified.

The jitter on the master clock is transferred to all the derived clocks.

Moreover, some clocks are locked to the S-interface as marked with "*" in 4.11, TABLE 9.7. Those clocks will adjust their periods with one XTLI 7.68 MHz period every 250 µs. The position of this DPLL adjustment relative to the S-bus frame or the GCI frame is not specified. Note that jitter or width modulation of the 7.68 MHz XTLI input signal can amplify the DPLL adjustments on the clocks marked with "*", which are locked on the downlink S-bus timing.

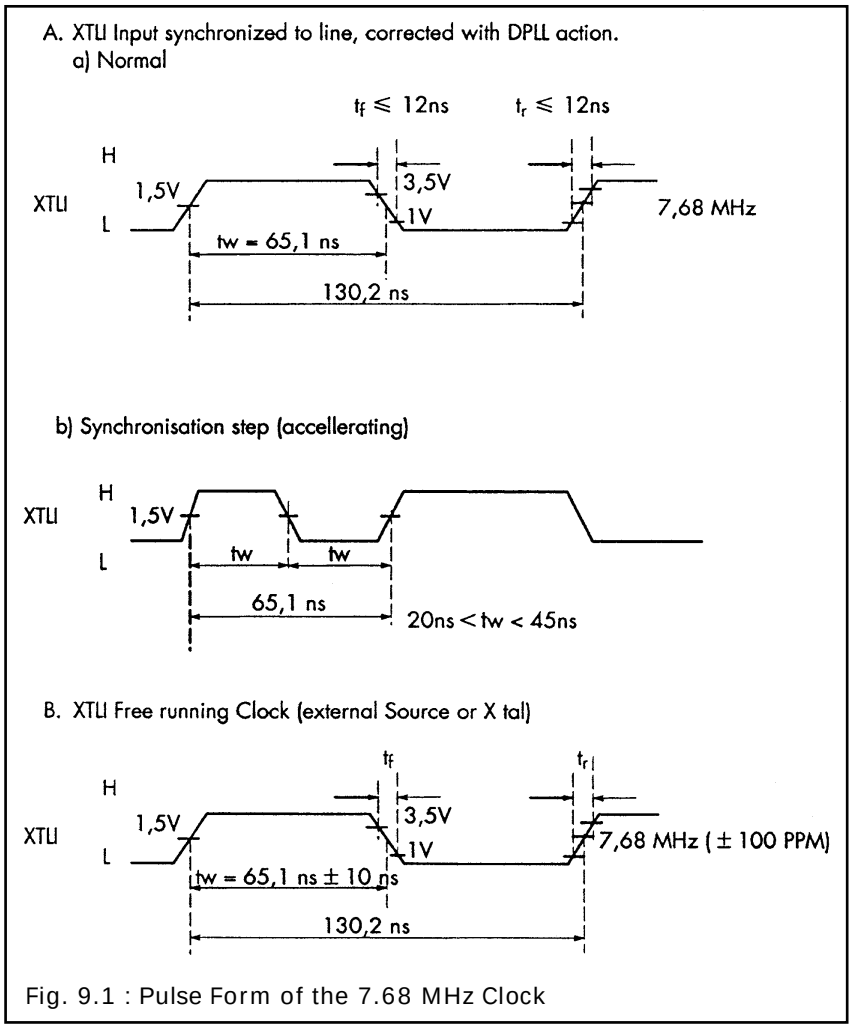


Fig. 9.1 : Pulse Form of the 7.68 MHz Clock

Table 9.8: Dynamic Characteristics of Derived Clock Signals

PIN	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
DCLK SCLK XTRi	Tr, Tf	Rise and Fall Time			20 #	ns

 # on a 100 pF load capacitance

9.6.3 Serial GCI Interfaces

Figure 9.2 explains the general behaviour of the signals. Note the MASTER modes (TE), where the MTC-20172 SIC generates the DCLK clock and DFR frame signals and the SLAVE modes, where the MTC-20172 SIC receives DCLK clock and DFR frame.

Table 9.9: Characteristics of GCI Signals, Master modes

PARAMETERS	TEST COND.	MIN	TYP	MAX	UNIT
TDD	Data Delay to Clock#			100	ns
TDD(extended)	Falling Data Delay#		100&		ns
TDD(extended)	Rising Data Delay #			xxx*	ns
TDF	Frame Delay to Clock	-20		20	ns
TSD	Data Setup Time	20			ns
THD	Data Hold Time	50			ns

 # bus capacity at 150 pF
& The falling edges are influenced by the external pull-up resistor in expended TE mode.

** The rising edge on the Dout pin is imposed by the external pull-up resistor in expended TE mode.*

9.6.3.1 MASTER Modes

Figure 9.2 shows the timing parameters of both MASTER modes : the GCI case and the inverted case.

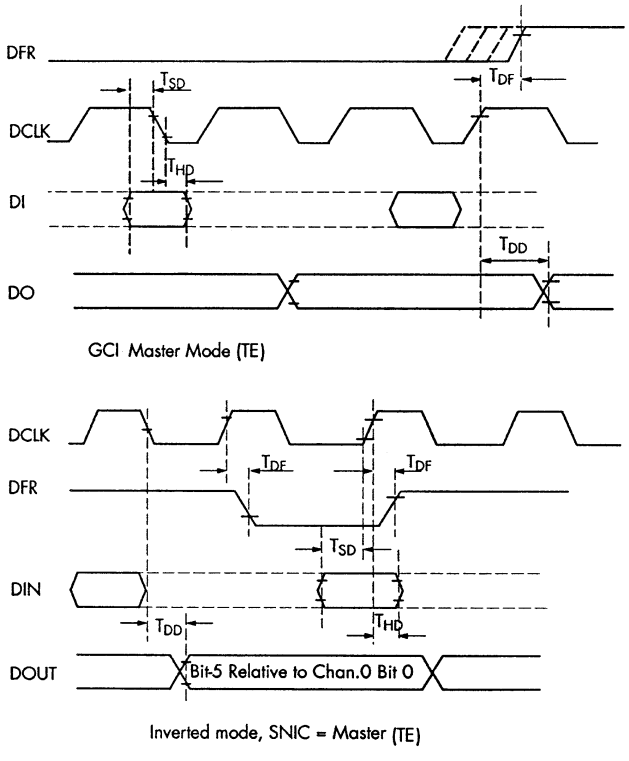


Fig. 9.2 : GCI Timing Parameters in TE

9.6.3.2 SLAVE Modes

Figure 9.3 shows the timing parameters.

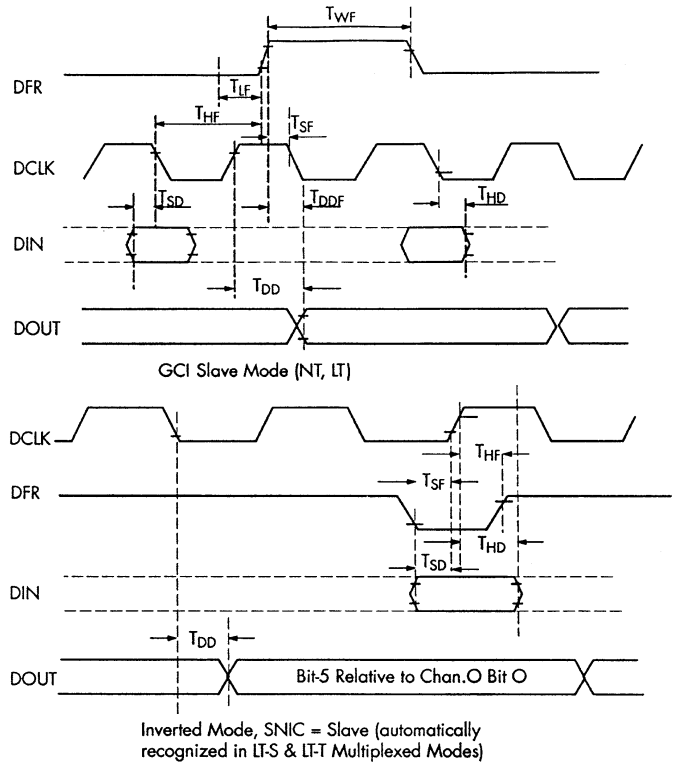


Fig. 9.3 : GCI Timing Parameters in NT, LT-Sand LT-T Mode

Table 9.10: Characteristics of GCI Frame, Slave modes

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNIT
	GCI mode				
THF	Frame Hold Time	30			ns
TSF	Frame Setup Time	50			ns
TWF	Frame Width (high)	40			ns
TLF	Frame Low Time	##			ns
	Inverted mode				
THF	Frame Hold Time	50			ns
TSF	Frame Setup Time	20			ns
TWF	Frame Width (low)	70	**		ns

Frame Low Time (GCI): more than two DCLK periods.

*** Frame Width low (inverted): nominally one DCLK period. This is necessary to recognize the modes automatically.*

Table 9.11: Characteristics of GCI Data, Slave modes

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNIT
TDD#	Data Delay, push-pull			100	ns
TDD#	Falling Data Delay (open drain)		100&		ns
TDD#	Rising Data Del.,extern.pull-up			xxx*	ns
TDD#	Rising Data Delay (NT basic mode)			900$	ns
TDDF	Data Delay to Frame			150	ns
TSD	Data Setup Time	20			ns
THD	Data Hold Time	50			ns

bus capacitance at 150 pF

& The falling edges are influenced by the external pull-up resistor in open drain bus (or multiplexed modes).

** Rising edge on the Dout pin is imposed by the external pull-up resistor when DOUT is open drain.*

$ Integrated pull-up resistor in NT basic mode, clock speed limited

9.6.4 RDY Pin

The timing is discussed in 5.7.5 and shown on Figure 5.6. The RDY pin Delay to the GCI DCLK signal is maximally 100 ns, for a 50 pf load.

9.6.5 ECHO Pin

The timing of the ECHO pin is the same as the DOUT pin. The ECHO pin is permanently at 1, except during the E bits, which coincide with the D-bits in the GCI frame on the DOUT pin, as shown on Figure 5.6.

9.6.6 RSTB Pins

Active low for minimally 1 ms.

9.6.7 DE/CEB Bus Timing

The falling edge (open drain) is maximally 20 ns when loaded with 50 pF. The rising edge is dependent on the INTERNAL 50 kΩ pull-up resistor, the number of active SICs on the DE/CEB bus, the bus capacitance, and possibly an extra external pull-up resistor.

Driving and Sensing the DE/CEB bus:

The individual SICs on the DE/CEB bus pull the bus low when a D-channel bit at binary 0 is sampled, i.e. a MARK on the S-bus. The edges on the bus are related to the internal sampling clock of the S-bus input data. Therefore, the absolute timing can not be specified, as shown on Figure 5.5. The maximal delay is 1.5µs relative to the last edge of the D-bit on the SRP and SRN analog inputs.

Sensing is done during the bit preceding the E-bit on the S-bus, as shown on Figure 5.5. All SICs participating on the bus are sensing the E-bus and driving the S-bus with a relative uncertainty of 1520 ns.

9.6.8 BER Pin

The timing of the BER pin is related to the internal sampling clock of the S-bus input data. Therefor, the absolute timing can not be specified. The falling edge (open drain) is maximally 20 ns when loaded with 50 pF. The rising edge is dependent on the EXTERNAL pull-up resistor.

9.6.9 TM1-, TM2-, SCZ-, SSZ-Pins

Force unconditional state change of the MTC-20172 SIC to send TEST1 or TEST2 signal on the S-bus outputs. The reaction time is depending of the state of the MTC-20172 SIC S-bus transceiver, as controlled via the C/I channel. Reaction times depend on the activation state of the GCI clock signals and the presence of the XTLI signal, or the activation (2ms) of the crystal connected between XTLO and XTLI.

9.6.10 The AUX Pins Used As General Purpose I/O

Signals are driven or sensed asynchronously via the M-channel messages, see 7.7.4. Output rise and fall times 20 ns on 50 pF, if no (internal or external) pull-up resistor is present.

10. Quality and Reliability Specifications

Related documents: See chapter 11.

10.1. Quality

10.1.1 Product acceptance tests

All products are tested 100 %, at ambient temperatures with full temperature range performance guardband, by means of production test programs that guarantee optimal coverage of the product specification.

10.1.2 Lot-by-lot acceptance test

Lot conformance to specification of products delivered in volume production is guaranteed by means of following tests:

Table 10.1: Acceptance Criteria

Test	Conditions	AQL level	Inspection level
Electrical, functional and parametric	To product specification at Tamb=25°C functional and with full temperature range performance parametric guardband.	0.15	I
External visual	Physical damage to body or leads. Dimensions affecting PCB manufacturability such as bent leads, coplanarity,...	0.15	II
External visual	Correctness of marking. All other major defects.	0.65	II

10.1.3 Assembly monitor

Assembly related product conformance is guaranteed by means of:

- the quality system of the assembly subcontractor
- incoming inspection on assembled material
- the IQA (incoming quality assurance) function including subcontractor audit
- the assembly monitor as specified in Table 10.2.

Table 10.2 : Assembly Monitor

Test	Conditions	Acceptance criteria
Hermeticity (only for cavity packages such as CLCC, SB, PGA,...)	Fine leak	AQL 0.40 IL II
Hermeticity (only for cavity packages such as CLCC, SB, PGA,...)	Gross leak	AQL 1.00 IL II
Solderability	T=245 °C, min 95% wetting of terminations. Meniscography	0 rejects on sample of 5 per package type per week.

10.1.4 Delivery lot Certification

Each delivery lot to be accompanied by a Certificate of Conformance

10.1.5. Quality System

A quality system with certification against ISO9001 is maintained.

10.2 Reliability Specification

In order to guarantee the specified reliability, Mietec performs a product qualification for each product. In order to minimize reliability testing, structural similarity is applied. This qualification procedure together with the application of structural similarity is described in the Mietec specification documents 15501, 15502, and 15503.

10.2.1 The Intrinsic Failure Rate

When used under benign conditions and a junction temperature of 50 °C, the failure rate will not exceed :

- 1000 ppm during the first year in the field
- 100 FIT or ppb/hour after the first year (long term failure rate)

Expected early failure rate is below 100 ppm.

Failures due to external overstress such as ESD, voltage and current overstress (e.g. due to EMI), mechanical and thermal shocks, ... are not included in these Figures.

10.2.2 External Stress Immunity

- Electrostatic discharge : The device withstands 1000 Volt Standardized Human Body Model ESD and 250 Volt CDM pulses when tested according to Mietec spec 15951.

- Latch-up : Static latch-up protection level is 50mA when tested according to JEDEC no. 17.

10.2.3 The Useful Life

The useful life, when used under moderate conditions, is at least 20 years. The term useful life is specified as the point in the lifetime, where the intrinsic failure rate exceeds the long term failure rate specified under 10.2.1

11. Related Documents

11.1 Related Documents

(1) MTC-20172 SIC Advance Information sheet, DS0139c.

(2) MTC-2072 UIC Data sheet and user manual.

(3) ISDN Application note - CCITT LAPD. AN0148a

(4) GCI interface, Industry standard bus, description agreed by Siemens, Alcatel, Plessey and Italtel. Evolution of the Siemens IOM-1 (trademarked), and later further enhanced to Siemens IOM-2 (also trademarked).

(5) "Mietec Packaging Handbook" PB026a, and specification number 16505

(6) "Standard Marking specification", specification number 16020

11.2 Other Documents

(1) CCITT Recommendation I.430 Edition 5/86, blue book, plus updates for the subsequent releases.

12. Application note for ETS-TM3 Qualification

12.1 Scope

This application note describes results of consultancy tests done at a qualified lab to perform ETSI-TM3 ISDN layer 1 conformance tests. A number of electrical tests specified in these conformance tests are sensitive to the SIC, external transformer and series resistances. Results will be given for a number of transformers. Also a number parameters will be given to setup a number of variables for the TM3 qualification.

12.2 External Circuit

See figure 12.1

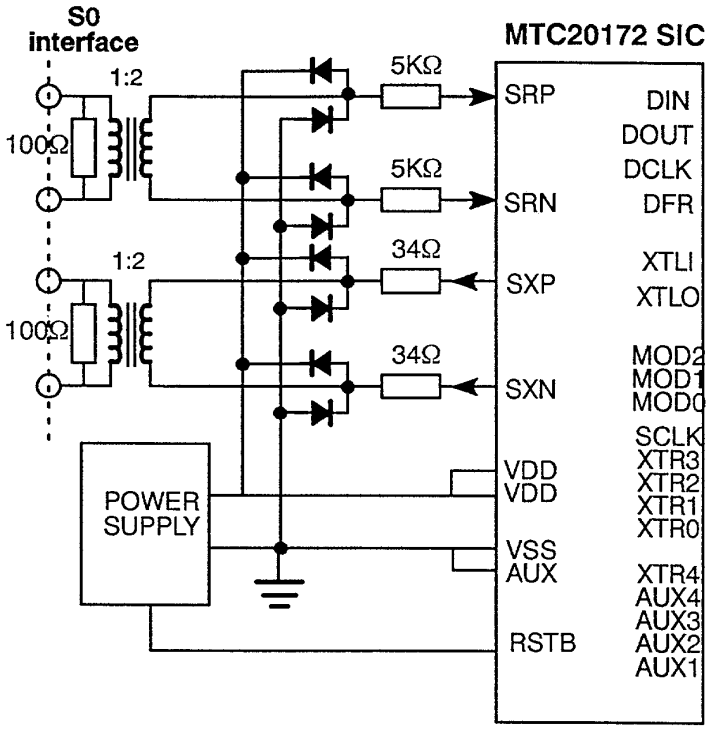


Fig. 12.1 : MTC-20172 SIC external circuity

12.3 ETSI-TM3 Configuration Setup

In order to pass succesfull the conformance test procedures a number of device dependant parameters mst be set :

12.3.1 Network Terminations (NT)

12.3.2 Terminal Equipments (TE, LTT)

Use a range for PX M; .....False
Frame Regain Frames (PX M) 6
Use a range for PX N: .....False
Frame Loss Frames (PX N) 2
Sendix Frame Type: IX-96KHz

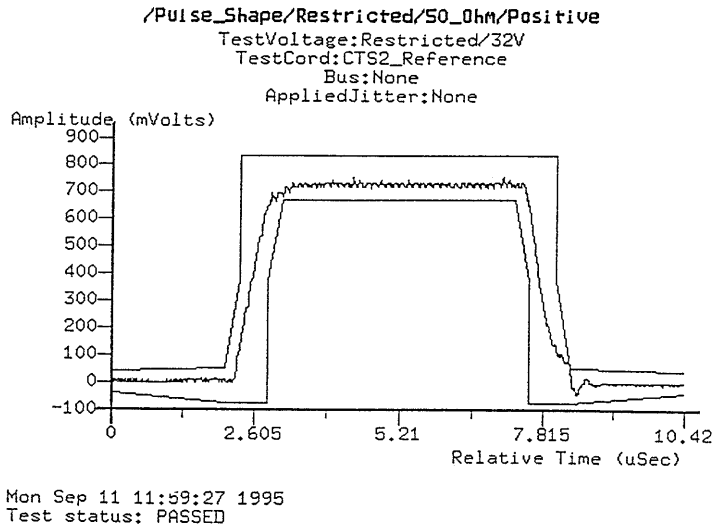
12.4 Qualification Results

Results will be shown for the pulse template tests and input and output impedance tests. The LCL test is not mentioned in this application note because it strongly depends on board layout and housing of the equipment. Following configurations have been measured :

Transformer	Transmitter series resistance	MTC-20172 version
VAC ZKB505/105	2 x 34Ω	FICA_OAB

12.4.1 Transformer VAC ZKB505/105

12.4.1.1 Output pulse Template for 50Ω



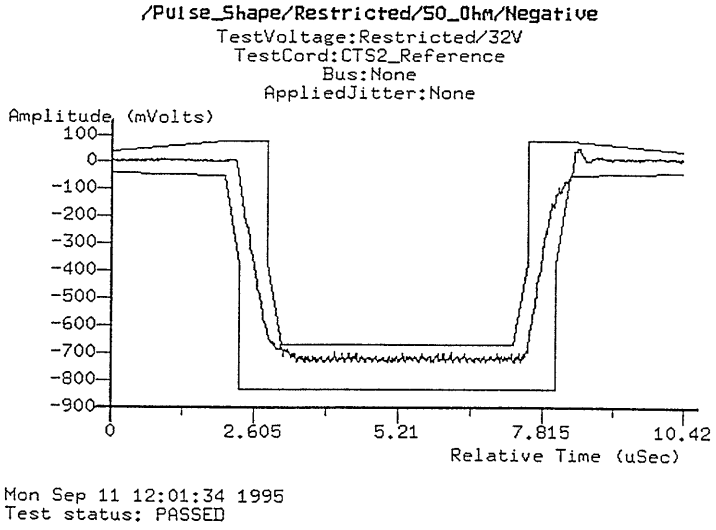
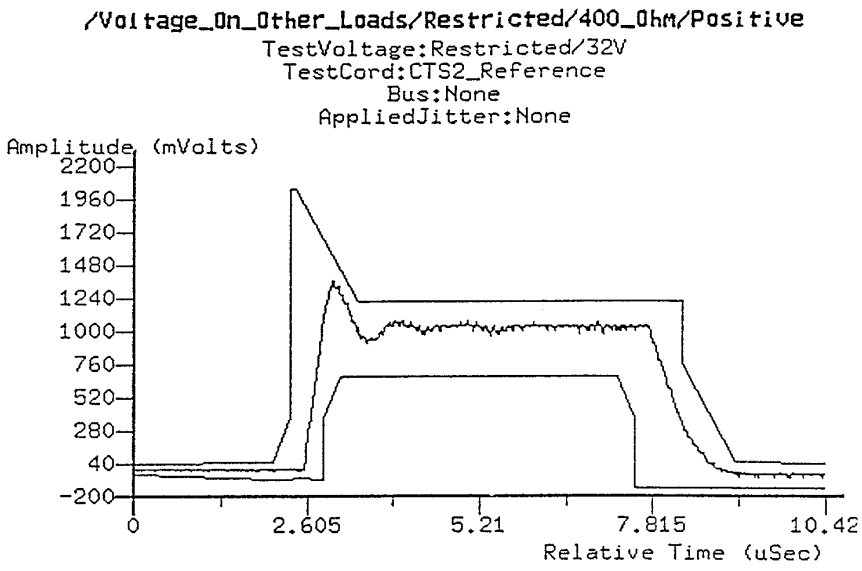


Fig. 12.2 : Output pulse template for 50Ω

12.4.1.2 Output Pulse Template for 400Ω



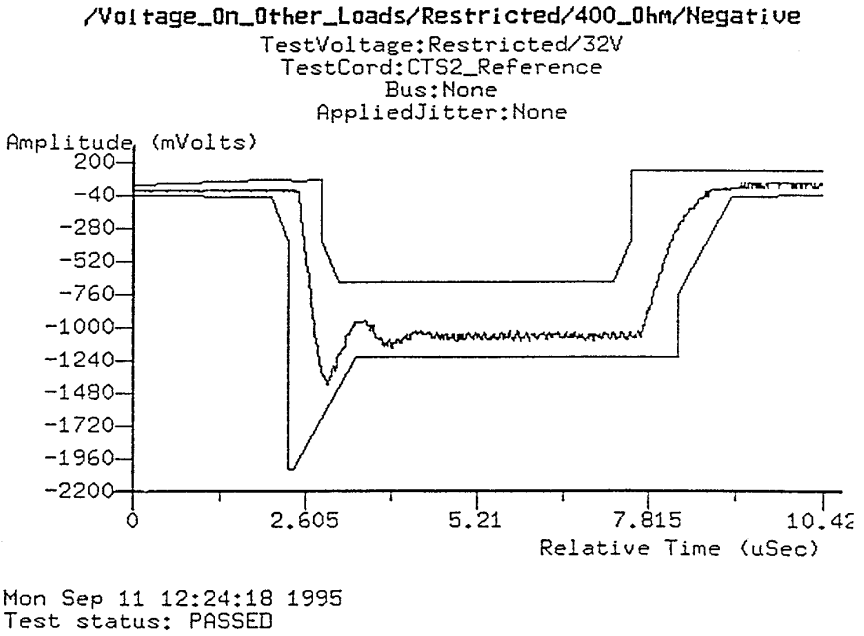


Fig. 12.3 : Output pulse template for 400Ω

12.4.1.3 Output Impedance Power off State

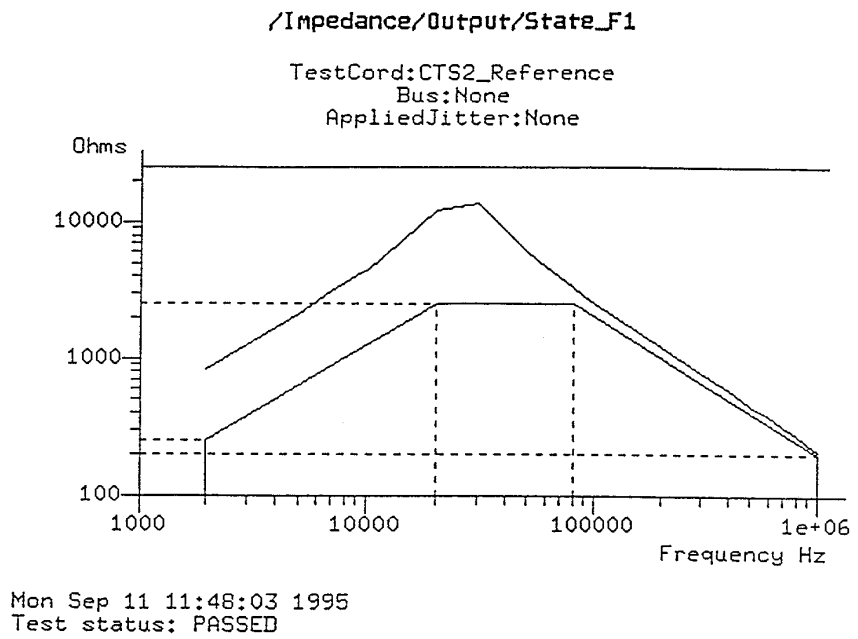


Fig. 12.4 : Output impedance State_F1

12.4.1.4 Output Impedance Power on State

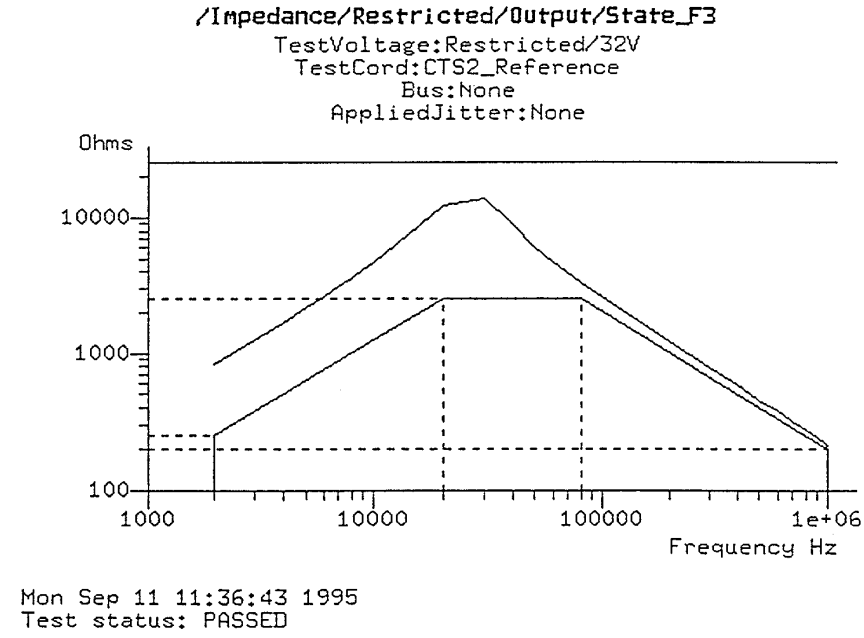


Fig. 12.5 : Output impedance State_F1

12.4.1.5 Input Impedance Power off State

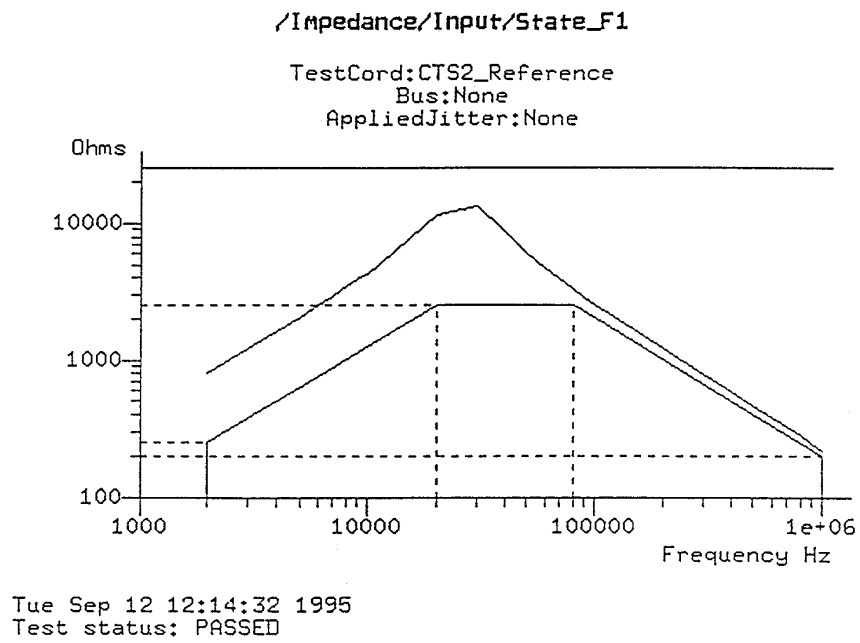


Fig. 12.6 : Input impedance State_F1

12.4.1.4 Input Impedance Power on State

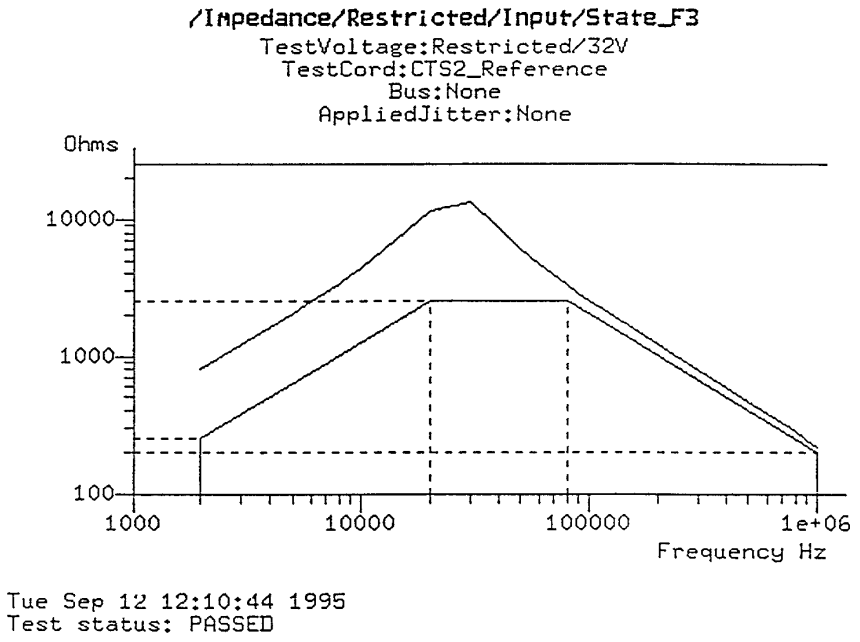


Fig. 12.7 : Input impedance State_F1

13. Application Note Network Terminator

13.1 Scope

This application not describes how to use the MTC-20172 in a network termination (NT) configuration. Also recommendations are given for the choice of external components in the receive and transmit path.

13.2 NT Mode with MTC-2071 4B3T UIC

13.2.1 Schematic Diagram

See figure 13.1

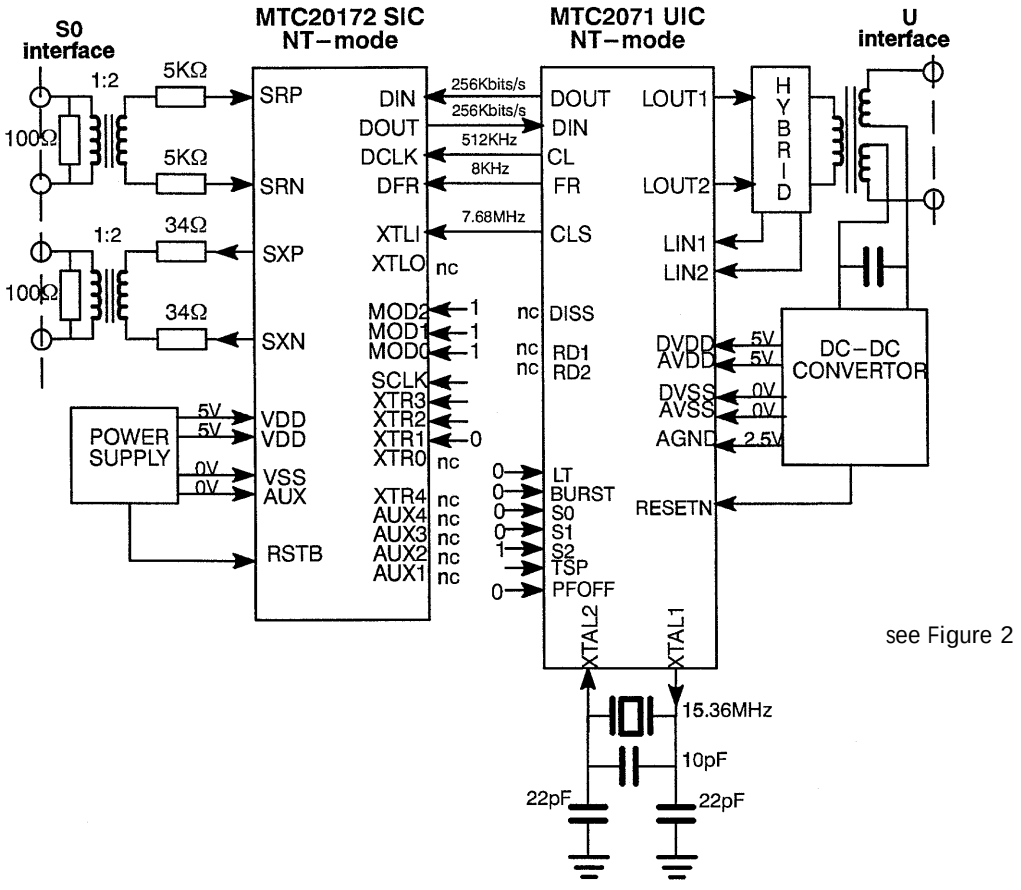


Fig. 13.1 : MTC-20172 SIC in NT mode with MTC2071 UIC

13.2.2 Description

Atthesubscriberpremises,the2–wire U–interface is terminated by a UIC in NT–mode. This UIC is connected to the SIC in NT- mode via the serial interface, to provide a 4–wire So–interface.

The SIC receives its clock from the UIC via the pin CLS. This clock (7.6BMHz) is synchronous to the received data at the U–interface and is derived from the master clock at the central office.

A number of pins can be strapped either to O or 1:

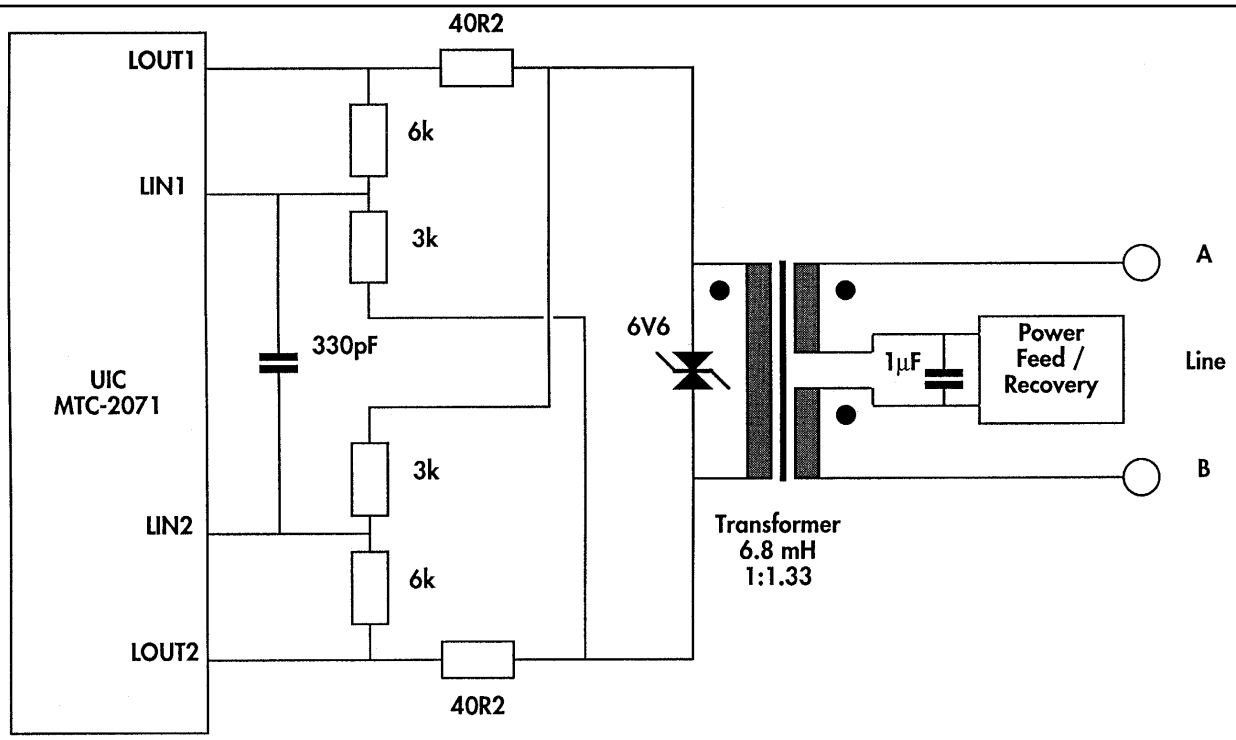


Fig. 13.2 : MTC-2071 UIC - recommended Hybrid and Transformer configuration

The device is initialized when the pin RESETB is held low. It is necessary to reset the device after the power is supplied to VDD. There commended time to keep RESETB low is ≥1 ms after VDD reaches 5V.

The device is delivered in a 22DIL or 28PLCC package. There are a number of pins only used in the 28PLCC package. The pins XTR4, AUX1, AUX3 and AUX4 can be left unconnected if the functionality is not needed. We recommend to connect the pin VDD(pin28) to the 5V power supply and the pin AUX(pin25) to the OV power supply.

Pin	Value	Description
SCLK	0	Switch on SCZ (send continuous zeros) testmode
	1	No action
XTR3	0	Adaptive timing for point to point mode
	1	Fixed timing for short passive bus mode (<200m)
XTR2	0	Switch on SSZ (send single zeros) testmode
	1	No action

13.3 Requirements for the Input and Output Stage

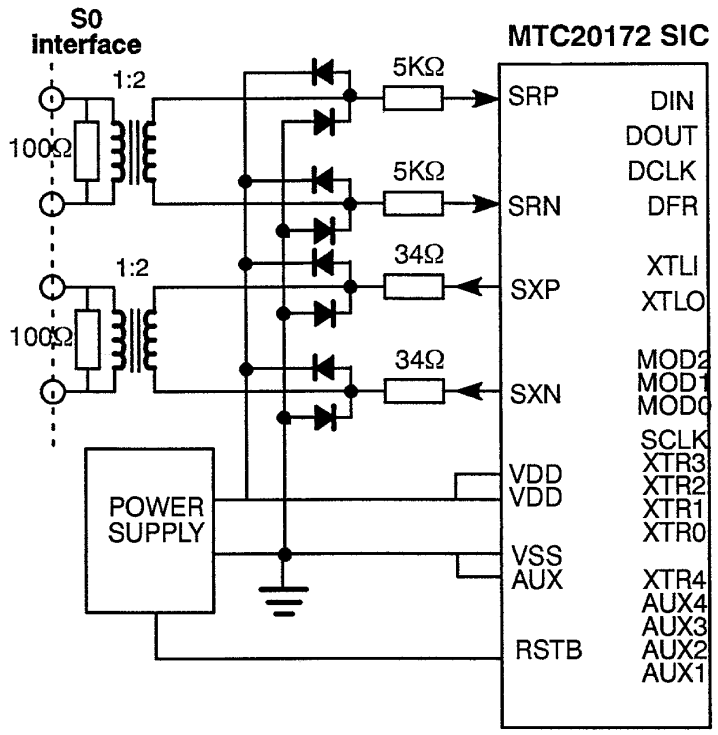


Fig. 13.3 : Schematic of MTC-20172 input and output stage

In the receive path the So-interface is terrninated with 50Ω (1 00Ω in the NT and 1 00Ω at the end of the So-bus). The input stage of the MTC-20172 SIC is fully differential.
A capacitance to ground as in the is not necessary and should be removed to benefit the higher immunity to common mode signals. The path also must contain 2 series resistances of 5KΩ to fuKil the CCITT 1.430 input impedance requirement. Protection circuitry must be present after the secondary of the transformer to make sure the SRP and SRN pin are not stressed higher than VDD+0.6V or lower than VSS-0.6V.

To fulfill the CCITT 1.430 requirement that the transmitter impedance must be ≥ 20Ω seen at the So-interface (so 80Ω seen at the secondary of the 1:2 transformer). To fuifil the CCITT 1.430 pulse amplitude requirement of 750mV over 50Ω at the So- bus, the MTC-20172 SIC driver has been designed as a current limited voitage source of 2.1V. With an extra series resistance of 80Ω in the transmit path both CCITT 1.430 requirements are met. The series resistance includes the transformer primary and secondary series resistance and the resistance of the connecting cord. A vaiue of 2x34Ω is recommended for the external resistors. Protection circuitry must be present after the secondary of the transformer to make sure the SXP and SXN pin are not stressed higher than VDD+0.6V or lower than VSS-0.6V.

MTC-20172
Data Sheet & Reference Manual
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