MTC-20144

Integrated ADSL
CMOS Analog Front-End
Circuit

Data Sheet

Rev. 1 - December1998

Features

- **Fully integrated AFE for ADSL**
- **Overall 12 bit resolution, 1.1MHz signal bandwidth**
- **8.8 MS/s ADC**
- **8.8 MS/s DACs(One)**
- **THD: - 60dB @ full scale**
- **1V full scale input**
- **Differential analog I/O**
- **Accurate continuous-time channel filtering**
- **3rd & 4th order tunable continuous time LP Filters**
- **64 pin TQFP package**
- **0.5 Watt at 3.3V**

Applications

- **ADSL Front-end for full rate and Lite standards**

General Description

The MTC-20144 is a fourth generation Analog Front End (AFE) designed for DMT based ADSL (Asynchronous Digital Subscriber Line) modems compliant with ANSI T1.413 category 2 standard.
It includes one 12-bit DACs and one 13-bit ADC. It is intended to be used with the MTC-20146 DMT/ATM processor as part of the MTK-20140 chipset, but may also be used to support other xDSL signal processors.

The MTC-20144 provides programmable low pass filters for each of the three channels and automatic gain control. A configuration pin allows the filters to be switched from ATU-R mode to ATU-C mode.
The pipeline ADC architecture provides 13 bit dynamic range and a signal bandwith of 1.1MHz.
The device consumes only 0.5 Watt in full operation and has a power down mode for standby. It is housed in a compact 64 pin thin plastic quad flat pack.

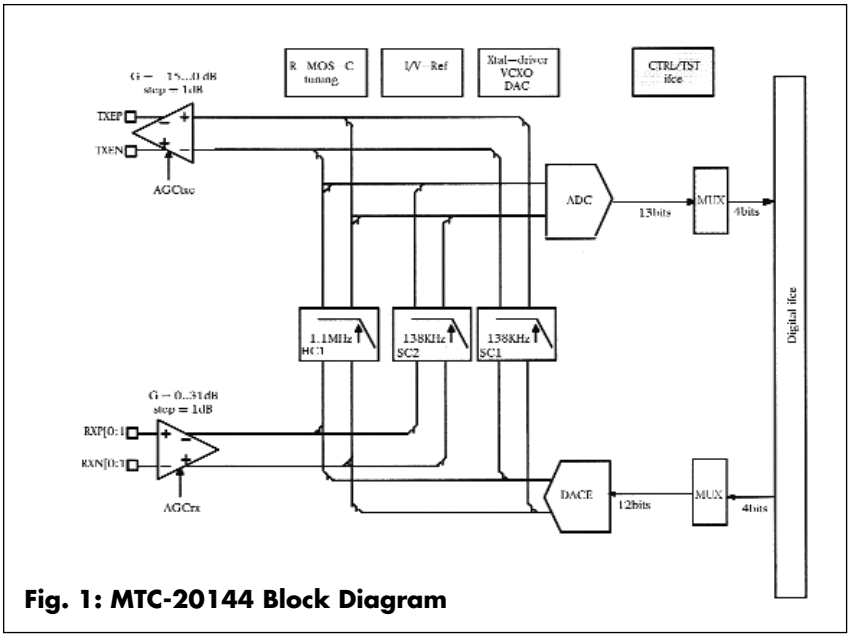


Fig. 1: MTC-20144 Block Diagram

Ordering Information

Part number	Package	Temp
MTC-20144TQ-I	64 pin TQFP	-40 to +85°C
MTC-20144TQ-C	64 pin TQFP	0 to +70°C

Can also be ordered using kit number MTK-20140

Functional Description

The MTC-20144 chip can be used on the ATU-C side (LT), and on the ATU-R (NT) side (defined by LTNT pin). The selection consists mainly of a filter interchange between the RX and TX path . The filters (with a programmable cutoff frequency) use automatic continuous time tuning to avoid time varying phase characteristics which can be of dramatic consequence for DMT modems. It requires few external components, uses a 3.3V supply and is packaged in a 64 pins TQFP in order to reduce PCB area. On the digital interface, a alternative mode with lower sampling rate (OSR=2; 4.4 Msamples/s) is provided. This allows support of xDSL digital components operating at different frequencies.

The Receiver (RX)

The DMT signal coming from the line to the MTC-20144 is first filtered by the two following external filters:
- POTS HP filter: Attenuation of speech and POTS signalling.
- Channel filter: Attenuation of echo signal to improve RX dynamic.

An analog multiplexer allows the selection between two input ports which can be used to select an attenuated (0,10 dB for ex.) version of the signal in case of short loop or large echo. The signal is amplified by a low noise gain stage (0-31 dB) then low-pass filtered to avoid anti-aliasing and to ease further digital processing by removing unwanted high frequency out-of-band noise.
A 12 bits A/D converter samples the data at 8.832 MS/s (a 4.416 Ms/s mode is also possible), transforms the signal into a digital representation and send it to the DMT signal processor via the digital interface.

The Transmitter (TX/TXE)

The 12 bits data at 8.832 Ms/s (or 4.416 Ms/s) coming from the DMT signal processor through the digital interface are transformed by a D/A converter into a analog signal.
This signal is then filtered to decrease DMT sidelobes level and meet the ANSI transmitter spectral response but also to reduce the out-of-band noise (which can be echoed to the RX path) to an acceptable level. The pre-driver buffers the signal for the external line driver and in case on short loop provide attenuation provision (-15..0 dB).

The VCXO

The VCXO is divided in a XTAL driver and a auxilliary 8 bits DAC for timing recovery.
The XTAL driver is able to operate at 35.328 MHz and provides an amplitude regulation mechanism to avoid temperature/supply/technology dependent frequency pulling.
The DAC which is driven by the CTRLIN pin provides a current output with 8 bits resolution and can be used to tune the XTAL frequency with the help of external components. A time constant between DAC input and VCXO output can be introduced (via the CTLIN interface) and programmed with the help of an external capacitor (on VCOCAP pin).

The Digital Interface

The digital part of the MTC-20144 can be divided in 3 parts :
The data interface converts the multiplexed data from/to the DMT signal processor into valid representation for the TX/TXE DAC and RX ADC.
The control interface allows the board processor to configure the MTC-20144 paths (RX/TX gains, filter band, ...) or settings (OSR, vcodac enable, digital/analog loopback, ...).

Package

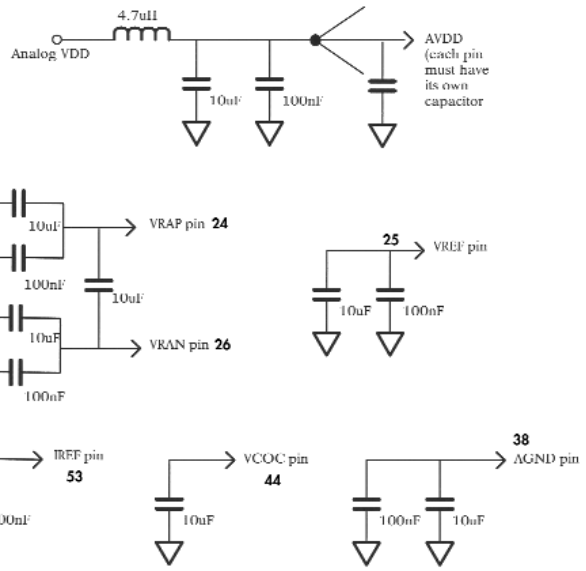
The MTC-20144 is housed in a 64-pin TQFP package.

Pin Assignment

Table 1 : Pinning Description MTC-20144 AFE

Pin No	Name	Description	PCB Connection	Supply
Analog Interface				
24	VRAP	positive voltage reference ADC	Decoupling network	AVDD3
25	VREF	ground reference ADC		AVDD3
26	VRAN	negative voltage reference ADC		AVDD3
29	N/C	no connection	Open	AVDD4
30	N/C	no connection	Open	AVDD4
31	TXP	pre driver output	Line-driver input	AVDD4
32	TXN	pre driver output		AVDD4
38	AGND	analog ground (1.65V=AVDD/2)	Decoupling network	AVDD5
44	VCOC	VCODAC time constant capacitor	VCODAC cap.	AVDD5
45	GC0	External Gain control output LSB		AVDD5
46	GC1	External Gain control output MSB		AVDD5
47	RXIN0	analog receive negative input Gain 0	Echo filter output	AVDD5
48	RXIP0	analog receive positive input Gain 0		AVDD5
49	RXIN1	analog receive negative input Gain 1 (most sensitive input)		AVDD5
50	RXIP1	analog receive positive input Gain 1 (most sensitive input)		AVDD5
53	IREF	current reference TX DAC/DACE	Decoupling network	AVDD2
55	VCO	current reference VCO DAC	VCO bias network	AVDD1
56	VCXO	VXCO control current	VCXO filter	AVDD1
59	XTALI	XTAL oscillator input pin	Crystal + varicap	AVDD1
60	XTALO	XTAL oscillator output pin		AVDD1
Digital Interface				
1	TX1	digital transmit input, parallel data		DVDD2
2	TX0	digital transmit input, parallel data		DVDD2
3	N/U		Ground	
4	N/U		Ground	
5	N/U		Ground	
6	N/U		Ground	
7	CTRLIN	serial data input (settings)	sync interface	DVDD2
9	CLKM	master clock output, f=35.328 MHz	Load=CL<30pF	DVDD2
10	CLNIB	nibble clock output, f=17.664 MHz (OSR=2) or ground (OSR=4)		DVDD2
11	CLWD	word clock output , f=8.832/4.416 MHz		DVDD2
12	RX3	digital receive output, parallel data	Load=CL<30pF	DVDD2

Pin No	Name	Description	PCB Connection	Supply
13	RX2	digital receive output, parallel data		DVDD2
14	RX1	digital receive output, parallel data		DVDD2
15	RX0	digital receive output, parallel data		DVDD2
18	PDOWN	power down select, "1"= power down	Power down input	DVDD2
19	LTNT	NT / LT select pin, NT=0/LT=1	VDD in LT-mode	DVDD2
20	RESETN	reset pin (active low)	RC-reset	DVDD2
22	GP0	General purpose output 0 (on AVDD !)	Echo Filter output	AVDD
33	GP1	General purpose output 1 (on AVDD !)	Echo Filter output	AVDD
43	GP2	General purpose output 2 (on AVDD !)	Echo Filter output	AVDD
63	TX3	digital transmit input, parallel data	Load=CL<30pF	DVDD2
64	TX2	digital transmit input, parallel data		DVDD2
57	XTALbypass	DC coupling for XTAL	AVSS	AVDD1
Supply Voltages				
8	DVSS1		DVSS	
16	DVDD1	Digital I/O supply voltage	DVDD	
17	DVDD2	Digital internal supply voltage	DVDD	
23	AVSS3		AVSS	
27	AVDD3	ADC supply voltage	AVDD	
28	AVDD4	TX pre-drivers supply	AVDD	
34	AVSS4		AVSS	
35	AVSS5		AVSS	
41	AVDD5	CT filter supply	AVDD	
42	AVDD6	LNA supply	AVDD	
51	AVSS6		AVSS	
52	AVSS2		AVSS	
54	AVDD2	DAC and support circuit	AVDD	
58	AVDD1	XTAL oscillator supply voltage	AVDD	
61	AVSS1		AVSS	
62	DVSS2		DVSS	



See chapter 'VCXO' for the external circuit related to the VCXO.
MTC-20144 grounding and decoupling networks

Fig. 2: MTC-20144 Grounding and Decoupling Networks

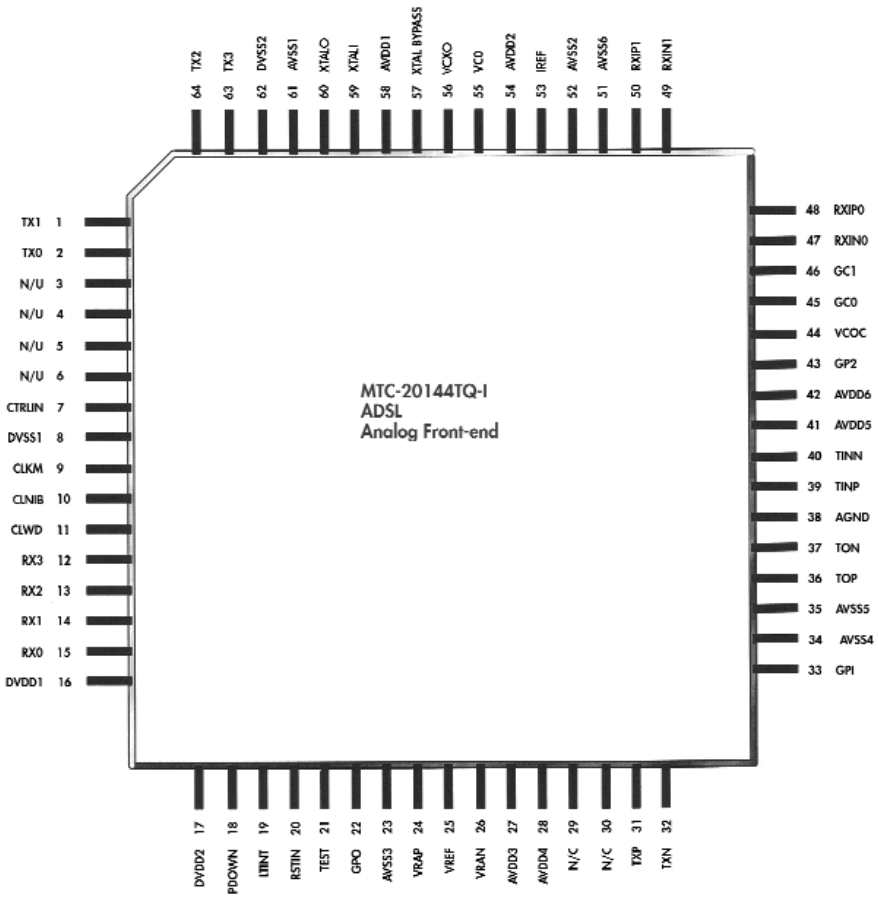


Fig. 3: Package MTC-20144: 64-Pin TQFP

Analog TX/RX Signals

The reference impedance for all power calculation is 100 Ω.

DMT Signal

A DMT signal is basically the sum of N independently QAM modulated signals, each carried over a distinct carrier. The frequency separation of each carrier is 4.3125 KHz with a total number of 256 carriers (ANSI). For N large, the signal can be modelled by a gaussian process with a certain amplitude probability density function. Since the maximum amplitude is expected to arise very rarely, the signal is clipped to trade-off the resulting SNR loss against AD/DA dynamic range.
A clipping factor (Vpeek/Vrms = "crest factor") of 5 is used resulting in a maximum SNR of 75 dB.
ADSL DMT signals are nominally sent at -40 dBm/Hz +/- 3 dB (-3.65 dBm/carrier) with a maximal power of 100 mW for downlink transmitter and 4.5 mW for uplink trasmitter.

The minimum SNR+D needed for DMT carrier demodulation is about (3*N+20) dB with a minimum of 38 dB where N is the constellation size of a carrier (in bits).

Table 2 : Signal Levels (on the line)

	LT side		NT side	
Description	**RX**	**TX**	**RX**	**TX**
Max level	839 mVpdif	15.8Vpdif	3.95 Vpdif	3.4Vpdif
Max RMS level	168 Vrms	3.16Vrms	791mVrms	671mVrms
Min level	54 mVpdif	3.95 Vpdif	42 mVpdif	839mVpdif
Min RMS level	11 mVrms	791mVrms	8 mVrms	168mVrms

Table 3 : Total Signal Level (on the line)

	LT side	NT side
Description	**RX**	**RX**
Max level for receiver	4 Vpdif (Long line)	4.2 Vpdif (Short line)

ATU_C Side Block Diagram

The transformer at ATU_C-side has 1:2 ratio. The termination resistors are 12.5Ω. in case of 100Ω lines.
The hybrid bridge resistors should be < 2.5 kΩ for low-noise.
An HP filter must be used on the TX path to reduce DMT sidelobes and out of band noise influence on the receiver.
On the RX path, a LP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver.
The POTS filter is used in both direction to reduce crosstalk between ADSL signals and POTS speech and signalling.

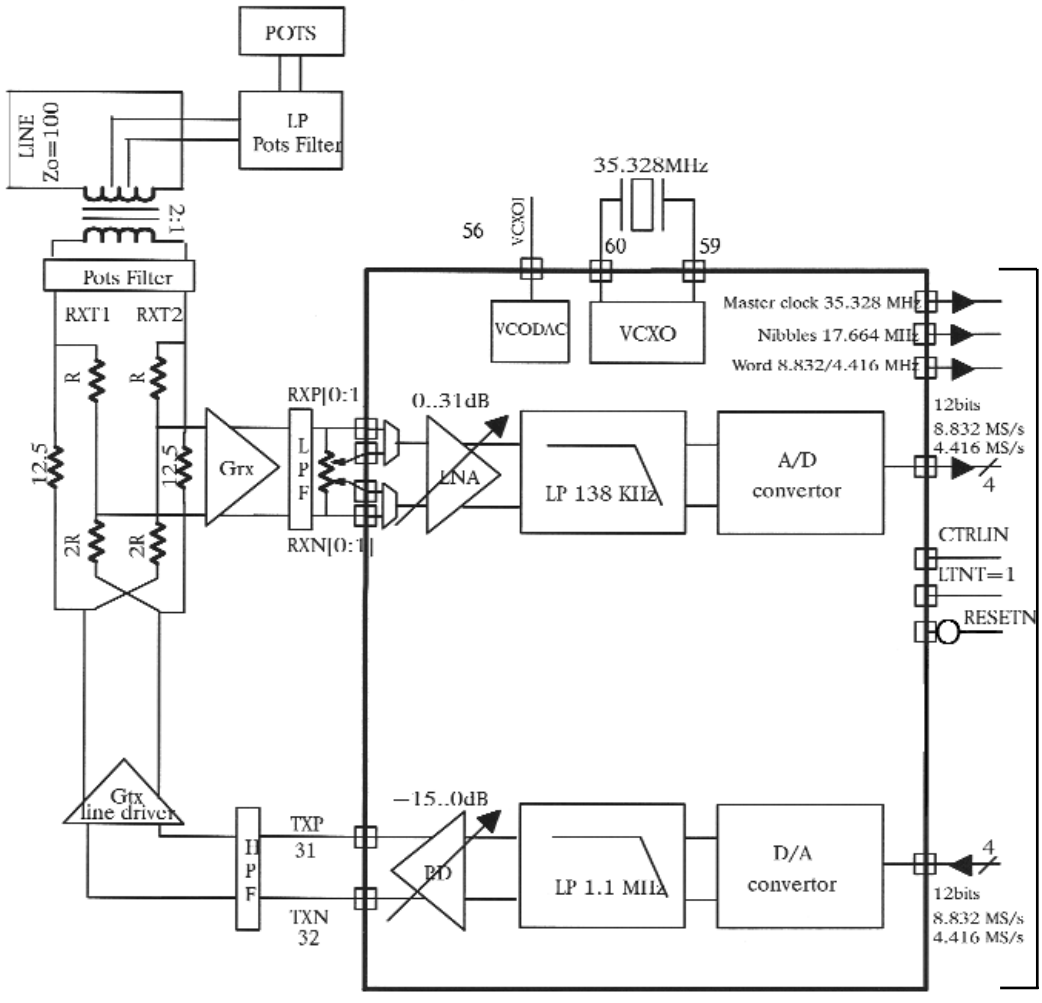


Fig. 4: ATU-C AFE Schematics

(For detailed schematics request MTK-20140 reference design.)

ATU_R Side Block Diagram

The ATU-R-side block diagram is equal to the ATU_C-side block diagram with the following differences :
- The transformer ratio is 1:1
- Termination resistors are 50Ω for 100Ω lines.

An LP filter may be used on the TX path to reduce DMT sidelobes and out of band noise influence on the receiver.
On the RX path, a HP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver.
The POTS filter is used in both direction to reduce crosstalk between ADSL signals and POTS speech and signalling.

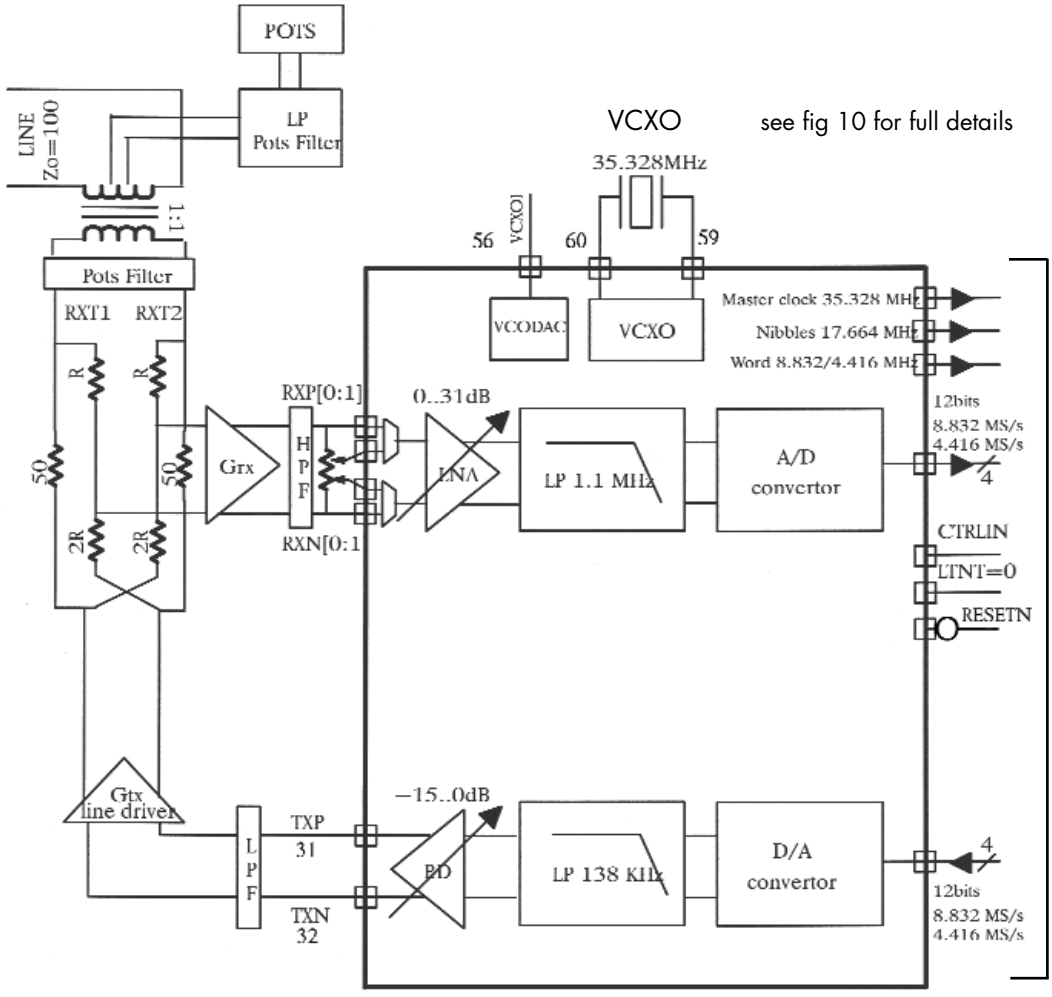


Fig. 5: ATU-R AFE Schematics

MTC-20144 RX PATH

Speech Filter

An external bidirectional LC filter for up and downstream POTS service splits out the speech signal to the analog telephone circuit on both the NT and LT sides of the line.
The ADSL analog front end Integrated circuit does not contain any circuitry for the POTS service but guarantees that the POTS bandwidth is not disturbed by spurious signals from the ADSL-spectrum.

Channel Filters

The purpose of these external analog circuits is to provide partial echo cancellation by an analog filtering of the receive signal for both ATU_R (Reception of downstream channel) and ATU_C (Reception of upstream channel). This is feasible because the upstream and the downstream data can be modulated on separate carriers (FDM).

RX Common-mode Voltage

Description	Value/Units
Common mode signal VCM at RXIN1 and RXIN2 :	1.6V < VCM < 1.7V

AGC of RX Path

The AGC gain in the RX-path is controlled through a 5-bits digital code. Four inputs are provided for RX input and the selection is made with the RXMUX bits of the CTRLIN interface. This can be used to make lower gain paths in case of high input signal.
The AGC characteristics are :

Description	Value/Units
Input refered noise (max. gain)	< 20 nVHz $^{-1/2}$ (an external gain is needed)
Max. input level	1 Vpd
Gain range :	0 dB ... 31 dB with step = 1 dB
Gain and step accuracy:	+- 0.3 dB

RX Filters

The combination of the external filter (an LC ladder filter typically) with the integrated lowpass filter provides :
- echo reduction to improve dynamic range
- DMT sidelobe and out of band (anti-aliasing) attenuation.
- Anti alias filter (60 dB rejection @ image freq.)

ATU-R-RX filters

The integrated filter has the following characteristics :

Description	Value/Units
Type	3th order butterworth
Frequency band	1.104 MHz (f0)
Frequency tuning	f0/1.4375 -> f0
Max. in-band ripple	1 dB

Phase characteristic :

Description	Value/Units
Total RX filter group delay	< 50 us @ 138kHz < f < 1.104 MHz
Total RX filter group delay distortion	<15 us @ 138kHz < f < 1.104 MHz

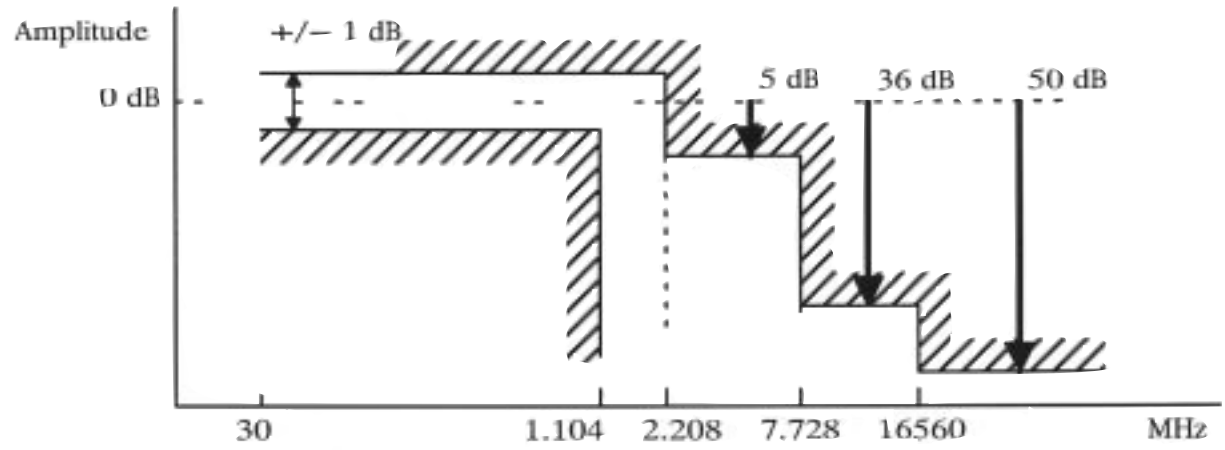


Fig 6:ATU-R-RX Filter Mask

ATU-C-RX Filter

This filter is the same as the one used for ATU_R_TX.

Linearity of RX

Linearity of the RX analog path is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.5Vpd amplitude (total _1Vpd) at the output of the RX-AGC amplifier (i.e: before the ADC) for the case of minimal AGC setting.

Linearity of ATU_R-RX

f1 (0.5Vpd)	300kHz	500kHz	700kHz
f2 (0.5Vpd)	200kHz	400kHz	600kHz
S/IM3	59.5dB @100kHz	59.5dB @300kHz	48.0dB @500kHz
(AGC=0dB)	53.5dB @400kHz	48.0dB @600kHz	42.5dB @800kHz
	43.5dB @700kHz		
	42.5dB @800kHz		

Linearity of ATU-C-RX

f1 (0.25Vpd)	80kHz
f2 (0.25Vpd)	70kHz
S/IM3	56.5dB @60kHz
(AGC=20dB)	56.5dB @90kHz

A/D Convertors

A pipeline architecture is used for the A/D convertor.

Number of bits :	13bits
Minimum resolution of the A/D convertor	11bits
Linearity error of the A/D convertor (range: -6dB FS)	<4LSB (out of 13bits)
Full scale input range :	1.1 Vpdif (+- 5% @ 3.3V)
Sampling rate :	8.832MHz (or 4.416MHz in alternative mode)
Maximum attenuation at 1.1 MHz :	< 0.5 dB without in-band ripple
Latency :	5 sampling clock periods

Power Supply Rejection

The noise on the power supplies for the RX-path must be lower than the followings :
< 50mVrms in band white noise for any AVDD.

MTC-20144 TX Path

Transmitter spectral Response

The two figures below show the ANSI spectral response mask for ATU_C and ATU_R transmitters

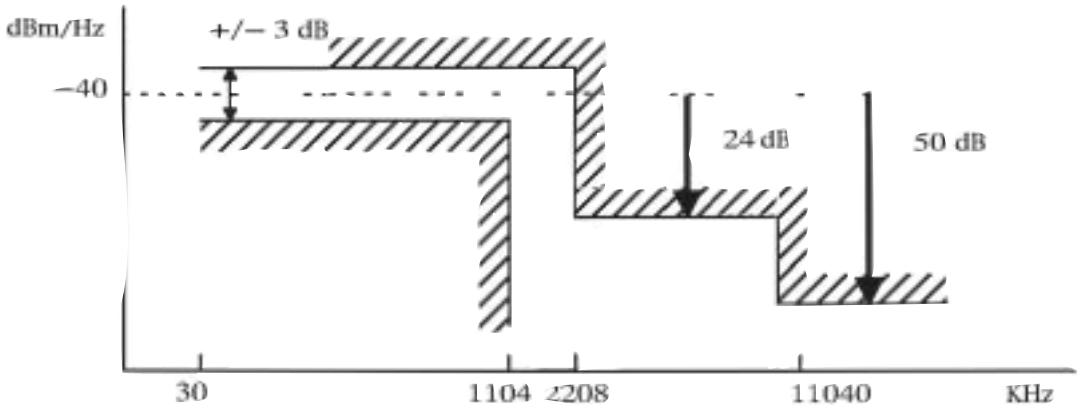


Fig.7 : ATU_C PSD Mask

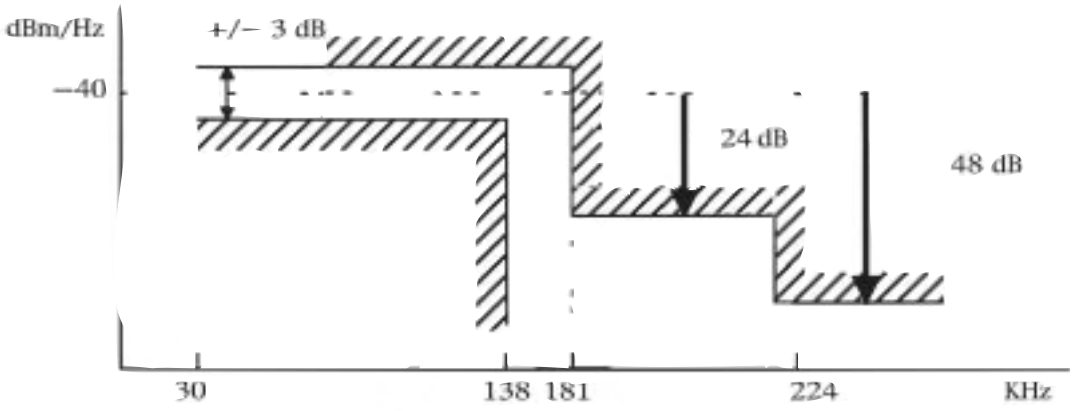


Fig.8 : ATU_R PSD Mask

AGC of TX Path (from filter output to TXO1 and TXO2)

Input level (nominal)	1 Vpd
Ouput level (nominal)	1.5 Vpd
AGC range :	14.5 dB ... 0 dB
AGC step :	0.97 dB
Gain and step accuracy :	+- 0.3 dB
Minimal code (0000) stands for AGC=-15dB and maximal (1111) for AGC=0dB.	

TX Pre-driver Capability

The pre-driver drives an external line power amplifier which transmits the required power to the line.

TX drive level to the external line driver for max AGC setting		1.5 Vpdif
External line driver input impedance :	resistive	>500Ω
	capacitive	<30pF
Pre-driver characteristics :		
closed loop gain :	-15dB...0 dB with step=1dB	
output offset voltage (0 dB) :	<10 mV	
input noise voltage (0 dB):	<20 nVHz$^{-1/2}$ @ f > 250k	
	<50 nVHz$^{-1/2}$ @ 34.5k<f< 138k	
output common mode voltage :	1.6V < Vcm < 1.7V	

TX Filter

The TX filters act not only to suppress the DMT sidebands but also as smoothing filters on the D/A convertor's output to suppress the image spectrum. For this reason they are realised in a time continuous approach.

ATU_R-TX Filter

The purpose of this filter is to remove out-of-band noise of the ATU_R-TX path echoed to the ATU_R-RX path. In order to meet the transmitter spectral response, an additional filtering is (digitally) performed. The integrated filter has the following nominal characteristics :

ATU_C-TX Filter

Same filter as ATU_R-RX. Its purpose is now is to remove image frequency of the transmitted signal according the ANSI definition.

Description	**Value/Units**
Input refered noise	220 nV/Hz$^{1/2}$
Max. input level	1 Vpd
Max. output level	1 Vpd
Type	4th order chebychef
Frequency band	138 KHz (f0)
Frequency tuning	f0/1.23 -> 1.25*f0
Max. in-band ripple	1 dB

Phase characteristic:

Description	**Value/Units**
Total RX filter group delay	<50 us @ 34.5kHz < f < 138kHz
Total RX filter group delay distortion	<8 us @ 34.5kHz < f < 138kHz

Note: The total TX path (including DAC) group delay distortion is 8 µs

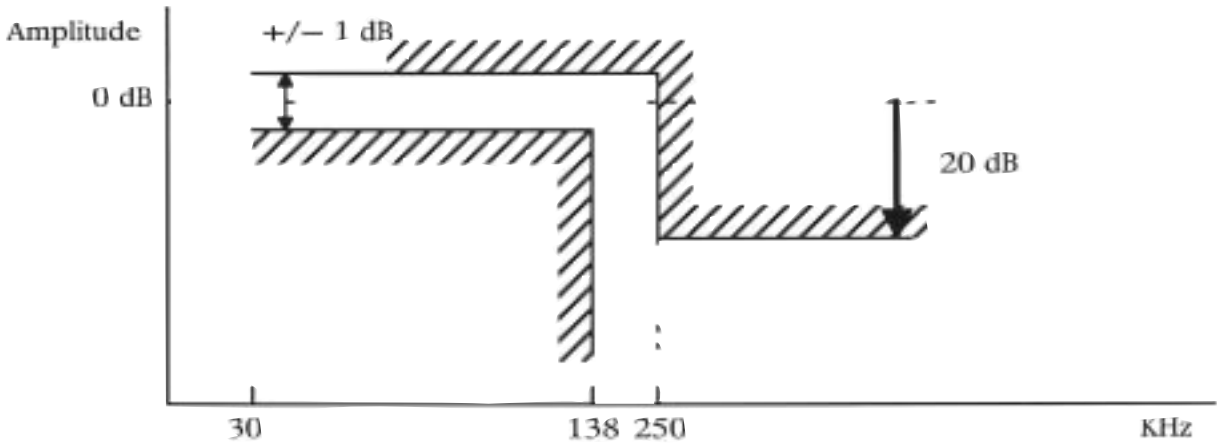


Fig. 9 : Filter Mask

D/A Convertor

Description	Value/Units
Number of bits :	12bits
Minimum resolution of the D/A convertor	11bits
Linearity error of the D/A convertor	<1LSB (out of 12bits)
Full scale output range :	1 Vpdif +- 5%
Sampling Rate :	8.832MHz (or 4.416 in alternative mode)
Latency :	1 sampling clock periode

Linearity of ATU_C-TX

Linearity of the TX is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.25Vpd amplitude (-6dB FS) at the output of the pre-driver for the case of a total AGC=0dB.

Linearity of ATU_C-TX

f1 (0.25Vpd)	300kHz	500kHz	700kHz
f2 (0.25Vpd)	200kHz	400kHz	600kHz
S/IM3	59.5dB @100kHz	59.5dB @300kHz	48.0dB @500kHz
(AGC=0dB)	53.5dB @400kHz	45.0dB @600kHz	42.5dB @800kHz
	43.5dB @700kHz		
	42.5dB @800kHz		

Linearity of ATU_R-TX

f1 (0.25Vpd)	80k
f2 (0.25Vpd)	70k
S/IM3 (AGC=0dB)	59.5dB(60k/90k)

Power Supply Rejection

The noise on the power supplies for the TX-path must be lower than the followings :
< 50mVrms in band white noise for AVDD.
< 15mVrms in band white noise for Pre-driver AVDD .

VCXO

A voltage controlled crystal oscillator driver is integrated in MTC-20144. Its nominal frequency is 35.328MHz. The quartz crystal is connected between the pins XTAL1 and XTAL2.
The principle of the VCXO control is shown on the figure below. The information coming from the digital processor via the CTRLIN path is used to drive a 8 bits I-DAC which generate a control current.
This current is externally converted and filtered to generates the required control voltage (range: -15 to 0.5V) for the varicap. The VCXO characteristics are given in Table 4.
N.B: Frequency tuning range is proportional to the crystal dynamic capacitance Cm.

The tuning is monotonic with 8-bit resolution with the worst-case tuning step of < 2ppm/LSB (8-bit). The time constant of the tuning can be selected through an external capacitor Ct.

Table 4: VCXO Characteristics

Parameters	Min	Nominal	Max	Note
Absolute frequency accuracy	-15ppm	35.328Mhz	+ 15ppm	
Frequency tunning range		±50ppm		
VCXO output current		100 µA		Rref=16,5 kΩ AVDD=3.3V

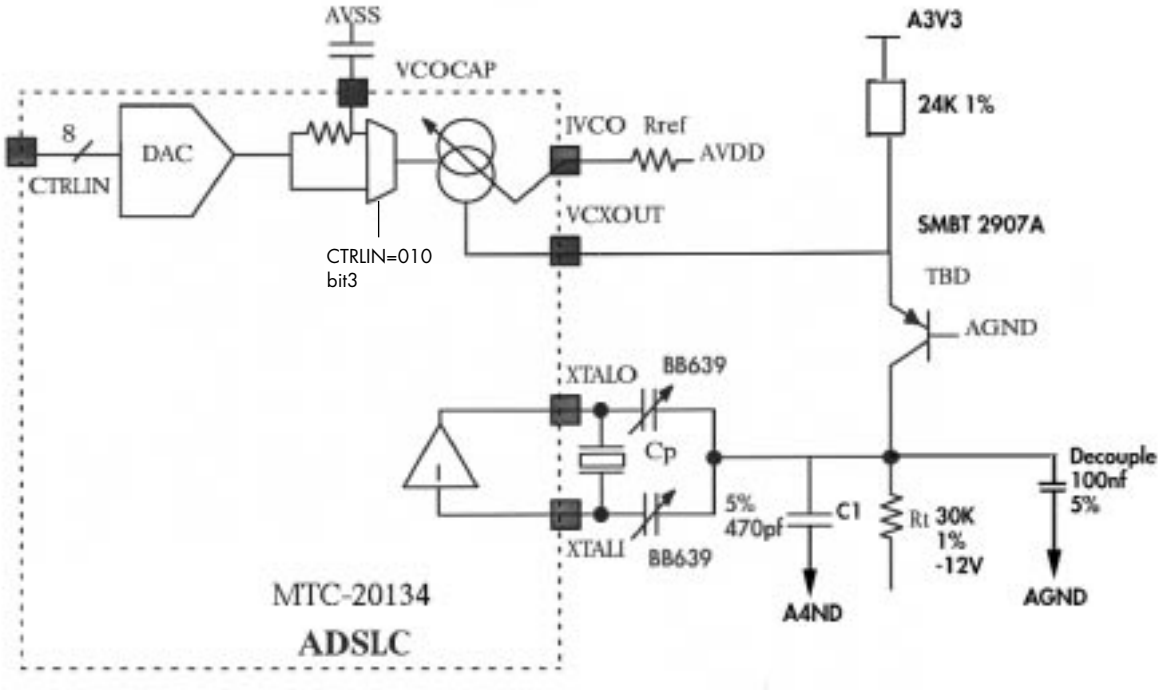


Fig. 10: Principle of VCXO Control

Digital Interface

Control Interface

The digital code setting for the MTC-20144 configuration is sent over a serial line (CTRLIN) using the word clock (CLWD). The data burst is composed of 16 bits from which the first bit is used as start bit ('0'), the three LSBs being used to identify the data contained in the 12 remaining bits. Test related data are latched but they are overuled by the normal settings if the TEST pin is low.

Control Interface Bit Mapping

CTRLIN[2:0]	Description	Bits mapping
"000"	RX settings	
	2 bit for external attenuation control (GC1, GC0) reset value = 00b	b[14:13]
	1 bit for RX input selection ("0"=IN0 .. "1"=IN1) reset value = 0b	b[12]
	5 bits for AGC RX - MSB first ("00000" = 0 dB, "11111" = 31 dB) reset value = 00000b	b[11:7]
	2 bits to force an HC filter selection for RX path used in LT configuration to use an HC filter as RX filter overloaded when test is active (direct selection) "00" & "11" normal mode "01" HC2 -> RX, AGND -> TX, "10" HC1 -> RX, AGND -> TXE power up HC1 if Echo not enabled ! reset value = "00"	b[6:5]
"001"	TX settings	
	4 bits for AGC TX - MSB first ("0000" = -15 dB, "1111" = 0 dB) reset value = 0000b	b[14:11]
	4 bit for AGC TXE - MSB first ("0000" = -15 dB, "1111" = 0 dB) reset value = 0000b	b[10:7]
	3 general purpose pins (GP2, GP1, GP0) reset value = 000b	b[6:4]
"010"	ADSLC configuration	
	1 bit for digital loopback ('1' enabled) reset value = 0b	b[14]
WARNING	1 bit for analog loopback ('1' enabled) **reset value = 1b**	b[13]
	1 bit for VCO DAC enable ('1' enabled) reset value = 1b	b[12]
	Reserved	b[11]
	1 bit for OSR ('0'=4, '1'=2) reset value = 0b	b[10]

	3 bit for SC frequency selection ("111"=138KHz=f0, "011"=f0/1.25 "100"=1.23*f0) reset value = 111b	b[9:7]
	3 bit for HC frequency selection ("100"=1.104MHz=f0, "011"=f0/1.4375) reset value = 100b	b[6:4]
	1 bit for filtered VCXO output ('1' = filtered) reset value = 0b	b[3]
"011"	VCO DAC value	
	8 bits for VCO DAC current ("0..0" = Min, "1..1" = Max current) reset value = 1000_0000b	b[14:7]
"100"	TEST ONLY : power down states	
	12 bits for analog power down, each bit controls one block: TXD (b14), TXED, ADC, HCF2, HCF1, SCF2, SCF1, LNA, DAC, DACE, VCODAC, XTAL (b3) reset value = 0000_0000_0000b	b[14:3]
"101"	TEST ONLY : TO output selection/ TI input selection	
	4 bits for analog test output selection, each code controls 1 (or none) blocks: DACE ("0001", DAC, LNA, SC1, SC2, HC1, HC2, VTUNESC, VTUNEHC, TEMPDIODE ("1010") reset value = 0000b	b[14:11]
	1 bits for uncoded ADC output (3X6bits on RXi, LTNT, PDOWN) reset value 0b	b[10]
	1 bits for SC1 input selection: DACE('0'), TIN ('1') reset vamue = 0b	b[9]
	2 bits for SC2 input selection: DAC ("00"), LNA, TIN, AGND ("11") reset value = 00b	b[8:7]
"110"	TEST ONLY : TIN input selection	
	2 bits for HC1 input selection: DACE ("00"), LNA, TIN, AGND ("11") reset value = 00b	b[14:13]
	2 bits for HC2 input selection: DAC ("00"), LNA, TIN, AGND ("11") reset value = 00b	b[12:11]
	2 bits for ADC input selection: SC2 ("00"), HC2, HC1, TIN ("11") reset value = 00b	b[10:9]
	2 bits for TXE input selection: HC1 ("00"), SC1, TIN, AGND ("11") reset value = 00b	b[8:7]
	2 bits for TX input selection: HC2 ("00"), SC2, TIN, AGND ("11") reset value = 00b	b[6:5]
	1 bits for external filter tuning frequency (onLTNT) reset value = 0b	b[4]
"111"	Not used. Reserved.	

Control Interface Timing

The word clock (CLWD) is used to sample at negative going edges the control informations. The start bit b15 is transmitted first followed by b[14:0] and at least 16 stop bits need to be provided to validate the data.

Data set up and hold time versus falling edge CLWD > 10nsec.

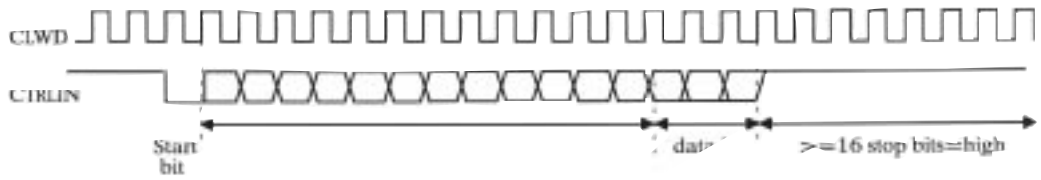


Fig. 11: Control Interface Timing

Receive / Transmit Interface

Receive / Transmit Protocol

The digital interface is based on a 4 * 8.832 MHz (35.328 MHz) clock. The 8.832MHz 12 bits A/D output signal or D/A input signal are SIPO multiplexed over 4 parallel 35.328 MHz data lines in the following table. If OSR=2 bit is selected, CLKNIB is used as nibble clock (17.664 MHz, disabled in normal mode), and all the RXi, TXi, CLKWD periods are twice as long as in normal mode. This ensure with lower frequencies digital chips.

	N0	N1	N2	N3
RXD0 / TXD0 will contain	b0	b4	b8	b12
RXD1 / TXD1 will contain	b1	b5	b9	b13
RXD2 / TXD2 will contain	b2	b6	b10	b14
RXD3 / TXD3 will contain	b3	b7	b11	b15

TX / TXE Signal Dynamic

The dynamic of the signal for both DACs is 12 bits extracted from the available signed 16 bit representation coming from the digital processor.

The maximal positive number is 2^{14}-1, the most negative number is -2^{14}, the 3 LSBs are ignored. Any signal exceeding these limits is clamped to the maximal value.

sign	sign	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	n.u.	n.u.	n.u.

Fig.12: TX/TXE Bit Map

RX Signal Dynamic Range

The dynamic range of the signal from the ADC is limited to 13 bits. Those bits are converted to a signed representation with a maximal positive number of 2^{14}-1 and a most negative number of 2^{14}. The 2 LSBs are filled with '0'.

sign	sign	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	0	0

Fig.13: RX Bit Map

Receive / Transmit Interface Timing

This interface is a triple (RX,TX, TXE) nibble-serial interface running at 8.8 MHz sampling (normal mode). The data are represented in 16 bits format, and transferred in groups of 4 bits (nibbles). The LSBs are transferred first. The MTC-20144 generates a nibble clock (= master clock in normal mode, CLKNIB in OSR=2 mode) and word signals shared by the three interfaces.
Data is transmitted on the rising edge of the master clock (CLKM/CLKNIB) and sampled on the low going edge of CLKM/CLKNIB. This holds for the data stream from MTC-20144 and from the digital processor.
Data, CLWD setup and hold times are 5 ns with reference to the falling edge of CLKM/CLKNIB.
RXD is sampled with CLKM rising edge.

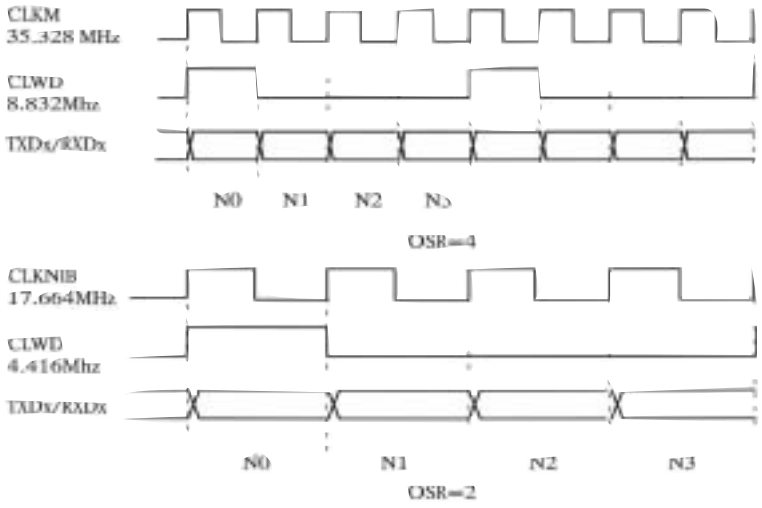


Fig. 14: TX/TXE/RX Digital Interface Timing

Power Down

When pin Pdown="1", the chip is set in power down mode. In this mode all analog functional blocks are deactivated except : preamplifiers (TX/TXE), clock circuits for output clock CLKM. PDown does not affect the digital part of the chip. The chip is activated when Pdown="0".

Power Down Conditions

In power down mode the following conditions hold :
- Output voltages at TX01/TX02=AGND
- The XTAL output clock on pin CLKM keeps running.
- All digital settings are retained.
- Digital output on pins RXDx don't care (not floating).

Following external conditions are added:
- Clock pins CLWD is running.
- CTRLIN signals can still be allowed.
- AGND remains at AVDD/2 (circuit is powered up)
- Input signals at TXDx inputs are not strobed.

Reset Function

The reset function is implied when the RESETN pin is at a low voltage input level.
In this condition, the reset function can be easily used for power up reset conditions.

Detailed Description

During reset :
- All clock outputs are deactivated and put to logical "1"
- (except for the XTAL and masterclock CLKM)

After reset :
- OSR = 4
- All analog gains (RX, TX, TXE) are set to minimum value.
- Nominal filter frequency bands (138 KHz, 1.104MHz)
- LNA input = "11" (max attenuation)
- VCO dac and Echo path disabled
- Depending of the LTNT pin value the following configuration is choosen:

Digital outputs are placed in don't care condition (non-floating)

'0' (NT)	
	RX : LNA -> HC2 -> ADC
	TX : DAC -> SC2 -> TX
'1' (LT)	
	RX : LNA -> SC2 -> ADC
	TX : DAC -> HC2 -> TX

Electrical Ratings and Characteristics

Absolute Maximum Ratings

Operation of the device beyond these limits may cause permanent damage. It is not implied that more than one of these conditions can be applied simultaneously.

Symbol	Parameter Description	Min	Max	Unit
VDD	Any VDD supply voltage, related to substrate	-0,5	4.8	Vhh
Vin	Voltage at any input pin	-0,5	VDD +0.5	V
Tstg	Storage Temperature	-60	150	°C
TL	Lead Temperature (10 second soldering)		300	°C
Pd	Power Dissipation		600	mW
Tj	Junction Temperature		150	°C

Operating Conditions

Unless specified, the characteristic limits of 'Static characteristics' in this document apply for the following operating conditions:

Symbol	Parameter Description	Min	Max	Unit
AVDD	AVDD supply voltages, related to substrate	3.0	3.6	V
DVDD	DVDD supply voltages, related to substrate	2.7	3.6	V
Vin, Vout	Voltage at any input and output pin	0	VDD	V
Ta	Ambient Temperature - I version	-40	85	°C
Ta	Ambient Temperature - C version	0	70	°C

Static Characteristics

Digital Inputs

Schmitt-trigger inputs : TXi, TXEi,
CTRLIN, PDOWN, LTNT, RESETN, TEST

Symbol	Parameter Description	Min	Max	Unit
VIL	Low level input voltage		0.2*DVDD	V
VIH	High level input voltage	0.8*DVDD		V
VH	Hysteresis	1.0	1.3	V
Cinp	Input capacitance		3	pF

Digital Outputs

Hard driven outputs : RXi

Symbol	Parameter Description	Test conditions	Min	Max	Unit
VOL	Low level output voltage	Iout=-4 mA		.15*DVDD	V
VOH	High level output voltage	Iout= 4mA	.85*DVDD		V
Cload	Load capacitance			30	pF

Clock Driver output : CLKM

Symbol	Parameter Description	Test conditions	Min	Max	Unit
VOL	Low level output voltage	Iout=-4 mA		.15*DVDD	V
VOH	High level output voltage	Iout= 4mA	.85*DVDD		V
Cload	Load capacitance			30	pF
Dcycle	Duty cycle		45	55	%
IDDPD	Supply current	Power down mode		TBD	mA
IDD	Supply current	Running		1650	mA

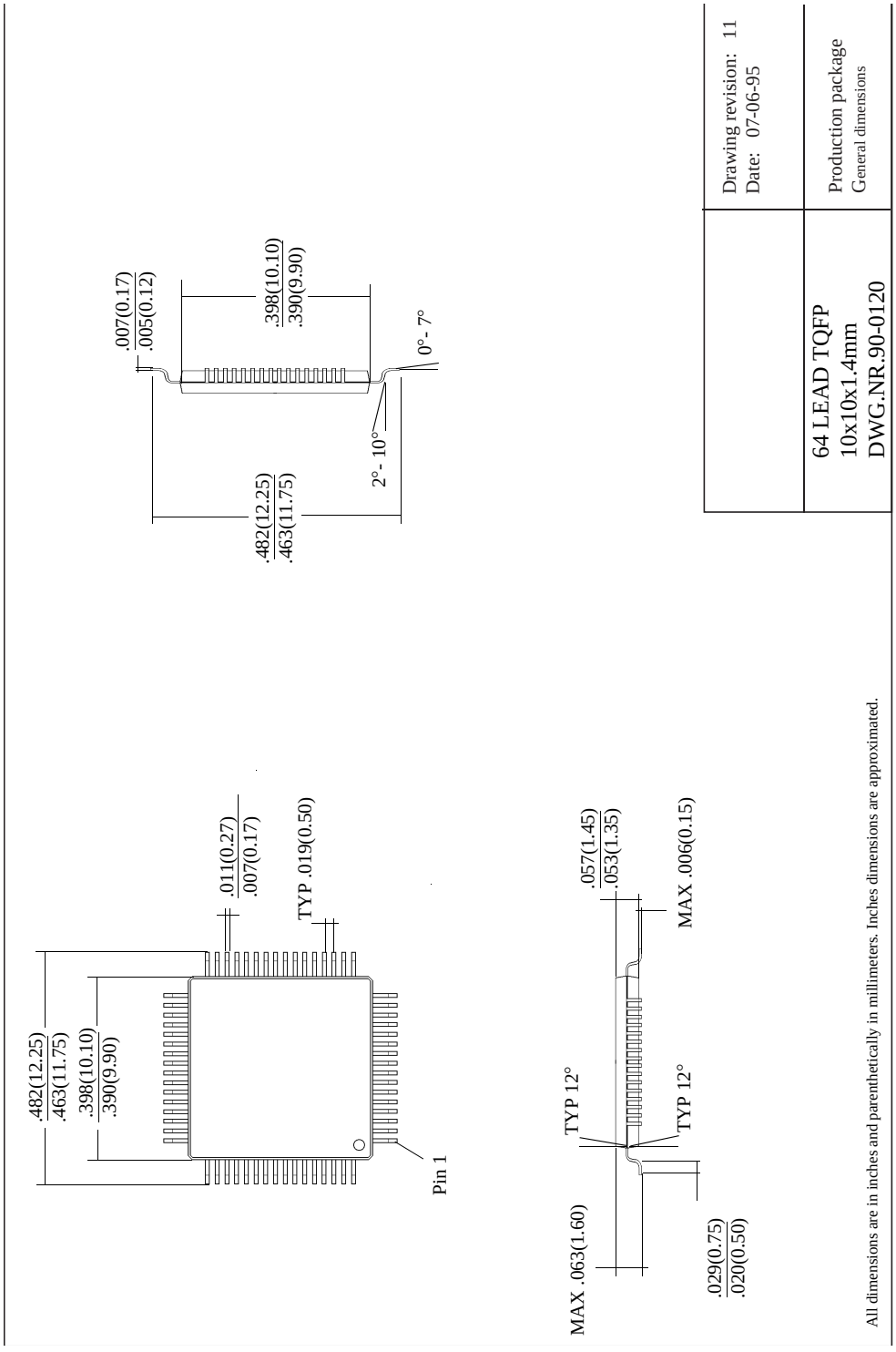


Fig.15: Package 64 Lead TQFP

MTC-20144

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