MT90502

Multi-Channel AAL2 SAR

Preliminary Information

DS5420 ISSUE 1 November 2000

Ordering Information

MT90502AG 456 Pin Plastic BGA

0 to +70°C

Features

- AAL2 Segmentation Reassembly device capable of simultaneously processing up to 1023 active CIDs (AAL2 Channel Identifier) and 1023 active VCC (Virtual Channel Connections).
- ATM VCCs can support up to 255 CIDs.
- Implements AAL2 Common Part Sub-layer (CPS) functions specified in ITU I.363.2.
- CPS packet payload can support up to 64 bytes.
- Can support over-subscription of 10:1.
- TDM Bus supports Multiple Data Transfer formats such as ITU G.711, G.726, G.723, G.728 and G.729.
- Support for a DSP array to perform a variety of operations such as compression of voice. Interface to DSP is by means of bit and byte aligned HDLC encoding on the TDM interface.
- Two UTOPIA ports: Ports A & B are configurable as a single 8-bit UTOPIA Level 2 PHY Port with 5 ADDR lines or dual 8-bit UTOPIA Level 1 configurable as PHY or ATM.
- Third UTOPIA port for connection to an external AAL5 SAR processor, or for chaining multiple MT90502 devices.
- TDM bus provides 32 bidirectional serial TDM streams operating at 2.40, 4.096, and 8.192 Mbits/s.
- Support clock recovery and generation.
- Performs silence suppression for PCM and ADPCM.
- Capability to inject and recover CPS packets through the CPU host processor bus.
- 8-bit or 16-bit microprocessor port, configurable to Motorola or Intel timing.
- IEEE 1149 (JTAG) interface.

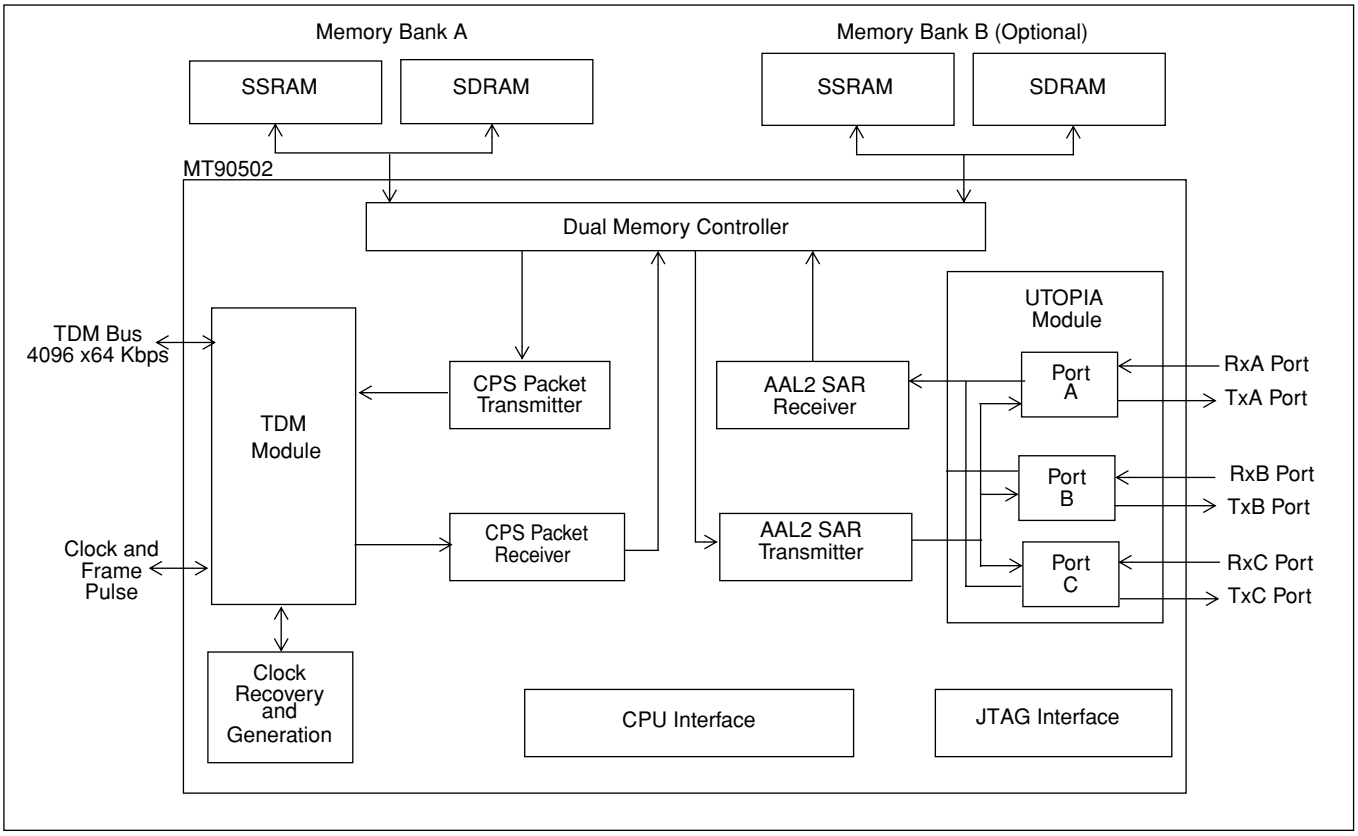


Figure 1 - MT90502 Functional Block

Applications

Gateway
ATM Edge Switch
Next Generation Digital Loop Carrier
Multiservice Switching Platform
3rd Generation Mobile System Equipment

Description

The MT90502 Multi-Channel AAL2 SAR bridges a standard TDM (Time Division Multiplexed) backplane to a standard ATM (Asynchronous Transfer Mode) bus. The device provides the CPS (Common Part Sublayer) and SAR (Segmentation and Reassembly) engines. The MT90502 has the capability of simultaneously processing 1023 bi-directional CIDs (AAL2 Channel Identifiers) and bi-directional VCCs (Virtual Channel Connections). The device can be connected directly to an H.110 compatible bus. The TDM bus consists of 32 bi-directional serial data streams operating at 2.048, 4.096, or 8.192 Mbits/s.

The MT90502 directly accepts PCM (Pulse Code Modulation) and ADPCM (Adaptive Differential Pulse Code Modulation) traffic for packetization. For the G.711 and G.726 data formats, the device also implements silence suppression and comfort noise generation. To support other voice compression algorithms, the MT90502 connects directly to commercially available DSPs through synchronous serial data streams. The Variable Bit Rate (VBR) traffic is HDLC encapsulated and carried over the serial data streams.

The interface to the ATM domain is provided by three UTOPIA ports (Ports A, B, and C). All three of the UTOPIA ports can operate in ATM (master) or PHY (slave) mode. Ports A and B combined, architects a compliant UTOPIA Level 2 Multi-PHY port. Port C is UTOPIA Level 1 compliant. The MT90502 provides the capability of routing ATM cells to different UTOPIA interfaces, SAR engine or CPU. This feature can be used to connect another MT90502 (to support over 2000 phone calls) or to connect an external AAL1 and AAL5 SAR.

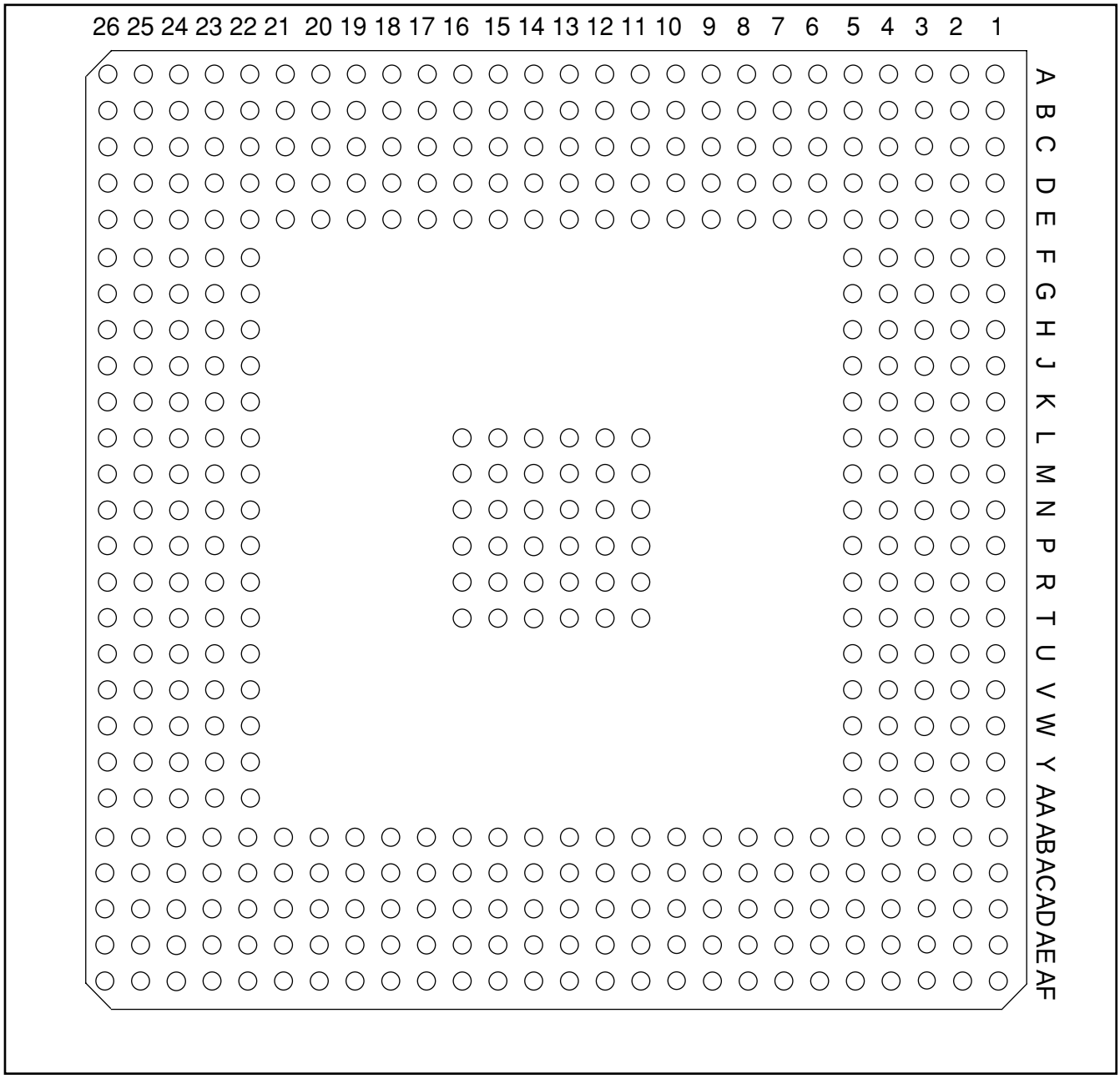


Figure 2 - 456 PBGA

Pin Description

EPBGA Pin	Name	Description (see notes 1-8)
		CPU Bus Interface Pins
AC3	mclk_src	CPU Clock.
F25, F23, J24, J23	cpu_mode[3:0]	CPU Interface Mode Select (4 bits). The CPU Interface Mode Select bits must be hardwired.
AA3, AA4, Y1, Y2, Y3, Y4, W1, W2, W3, W4, V1, V2, V3, V4, U1	cpu_a[14:0]	CPU Address bus.
T2	cpu_wr_rw	Intel Write & Motorola Read/Write
T1	cpu_rd_ds	Intel Read & Motorola Data Strobe
U4	cpu_ale	Address Latch Enable
T4	cpu_a_das	Direct Access Select. '1' selects the direct address space. '0' selects the indirection registers contained in the CPU interface. This pin can be connected to the MSB of an address bus but does not behave as an address pin.
U3	cpu_cs	CPU chip select
T3, R1, R2, R3, R4, P1, P2, P3, P4, N1, N2, N3, N4, M1, M2, M3	cpu_d[15:0]	CPU Data bus
U2	cpu_rdy_ndtack	Intel Ready & Motorola Data Ack.
AC2	interrupt1	Interrupt 1 (configurable polarity)
AC1	interrupt2	Interrupt 2 (configurable polarity)
		UTOPIA Interface Pins
C21	txa_led	UTOPIA port A TX LED
A19	rxa_led	UTOPIA port A RX LED
D21	rxa_alarm	UTOPIA port A PHY alarm
D12	txa_clk	UTOPIA port A TX clock
D14	txa_soc	UTOPIA port A TX Start of Cell
A13	1. $\overline{\text{txa\_enb}}$ 2. txa_clav	1. UTOPIA port A TX Enable (in ATM) 2. UTOPIA port A TX Cell Available (in PHY)
B13	1. txa_clav 2. $\overline{\text{txa\_enb}}$	1. UTOPIA port A TX Cell Available (in ATM) 2. UTOPIA port A TX Enable (in PHY)
C15, B15, A15, C14, B14, A14, D13, C13	txa_d[7:0]	UTOPIA port A TX Data bus
D15	txa_prty	UTOPIA port A TX Parity
A9	rxa_clk	UTOPIA port A RX clock
C12	rxa_soc	UTOPIA port A RX Start of Cell
B9	1. $\overline{\text{rxa\_enb}}$ 2. rxa_clav	1. UTOPIA port A RX Enable (in ATM) 2. UTOPIA port A RX Cell Available (in PHY)

Pin Description (continued)

EPBGA Pin	Name	Description (see notes 1-8)
C9	1. rxa_clav 2. $\overline{\text{rxa\_enb}}$	1. UTOPIA port A RX Cell Available (in ATM) 2. UTOPIA port A RX Enable (in PHY)
A12, C11, B11, A11, D10, C10, B10, A10	rxa_d[7:0]	UTOPIA port A RX Data bus
B12	rxa_prty	UTOPIA port A RX Parity
D17	txb_led	UTOPIA port B TX LED
C17	rxb_led	UTOPIA port B RX LED
B17	rxb_alarm	UTOPIA port B PHY alarm
D5	txb_clk	UTOPIA port B TX clock
D8	txb_soc	UTOPIA port B TX Start of Cell
A6	1. $\overline{\text{txb\_enb}}$ 2. txb_clav	1. UTOPIA port B TX Enable (in ATM) 2. UTOPIA port B TX Cell Available (in PHY)
B6	1. txb_clav 2. $\overline{\text{txb\_enb}}$	1. UTOPIA port B TX Cell Available (in ATM) 2. UTOPIA port B TX Enable (in PHY)
B8, A8, D7, C7, B7, A7, D6, C6	txb_d[7:0]	UTOPIA port B TX Data bus
C8	txb_prty	UTOPIA port B TX Parity
E4	rxb_clk	UTOPIA port B RX clock
A4	rxb_soc txa_addr[4]	UTOPIA port B RX Start of Cell. txa_addr[4] when UTOPIA is configured as single PHY port.
D3	1. $\overline{\text{rxb\_enb}}$ 2. rxb_clav	1. UTOPIA port B RX Enable (in ATM) 2. UTOPIA port B RX Cell Available (in PHY)
C1	1. rxb_clav 2. $\overline{\text{rxb\_enb}}$	1. UTOPIA port B RX Cell Available (in ATM) 2. UTOPIA port B RX Enable (in PHY)
A2, D4, A1, B1, C2	rxb_d[4:0] rxa_addr[4:0]	UTOPIA port B RX Data bus [4:0]. rxa_addr[4:0] when UTOPIA is configured as single PHY port.
A3, B3, B2	rxb_d[7:5] txa_addr[2:0]	UTOPIA port B RX Data bus [7:5]. txa_addr[2:0] when UTOPIA is configured as single PHY port.
B4	rxb_prty txa_addr[3]	UTOPIA port B RX Parity. txa_addr[3] when UTOPIA is configured as single PHY port.
J4	txc_clk	UTOPIA port C TX clock
D2	txc_soc	UTOPIA port C TX Start of Cell
G1	1. $\overline{\text{txc\_enb}}$ 2. txc_clav	1. UTOPIA port C TX Enable (in ATM) 2. UTOPIA port C TX Cell Available (in PHY)
G2	1. txc_clav 2. $\overline{\text{txc\_enb}}$	1. UTOPIA port C TX Cell Available (in ATM) 2. UTOPIA port C TX Enable (in PHY)
E3, E2, E1, F3, F2, F1, G4, G3	txc_d[7:0]	UTOPIA port C TX Data bus
D1	txc_prty	UTOPIA port C TX Parity
L1	rxc_clk	UTOPIA port C RX clock
H3	rxc_soc	UTOPIA port C RX Start of Cell

Pin Description (continued)

EPBGA Pin	Name	Description (see notes 1-8)
L2	1. $\overline{\text{rxc\_enb}}$ 2. rxc_clav	1. UTOPIA port C RX Enable (in ATM) 2. UTOPIA port C RX Cell Available (in PHY)
L3	1. rxc_clav 2. $\overline{\text{rxc\_enb}}$	1. UTOPIA port C RX Cell Available (in ATM) 2. UTOPIA port C RX Enable (in PHY)
H1, J3, J2, J1, K4, K3, K2, K1	rxc_d[7:0]	UTOPIA port C RX Data bus
H2	rxc_prty	UTOPIA port C RX Parity
H.110 Interface Pins		
A22	ct_c8_a	H.110 compatible 8MHz clock A
A21	ct_c8_b	H.110 compatible 8MHz clock B
A24	ct_frame_a	H.110 compatible Frame A
B22	ct_frame_b	H.110 compatible Frame B
A17	ct_netref1	H.110 compatible Netref 1
A16	ct_netref2	H.110 compatible Netref 2
D18	ct_mc	H.110 compatible Message Channel. If this pin is connected to the H100 bus, gpio[2] must be used to drive it.
C25, D25, E26, E25, E24, F26, F24, G26, G25, G24, G23, H24, J26, J25, K26, K24, L23, L24, M25, M24, N25, P24, P23, R24, R25, T26, U23, U26, V23, V24, V26, W23	ct_d[31:0]	H.110 compatible serial data bus
B20	sclk	SCBUS system clock
C20	sclkx2	SCBUS system clock x 2
C18	c16p	H-MVIP 16 MHz clock
A18	c16n	H-MVIP 16 MHz clock
D20	c2	MVIP 90-bit clock
C19	c4	MVIP 90-bit clock x 2
B21	frcomp	compatibility frame pulse
Memory Interface Pins		
AF2	mem_clk_i	Master clock: memory clock (common to both bank A and B) and is employed as the internal master clock.

Pin Description (continued)

EPBGA Pin	Name	Description (see notes 1-8)
AF11, AD10, AF10, AD9, AF9, AE8, AC7, AE7, AD7, AF8, AD8, AE9, AC9, AE10, AC10, AE11	mema_d[15:0]	SDRAM/SSRAM bank A data bus
AD11, AF7	mema_p[1:0]	SDRAM/SSRAM bank A parity bits
AF4, AE3	mema_cs[1:0]	SSRAM bank A Chip selects 1, 0
AE5	mema_rw	SSRAM bank A Read/Write
AE4, AF5	mema_bws[1:0]	SSRAM bank A Byte Write Selects 1:0
AE12	mema_cas	SDRAM bank A Column Address Select
AD12	mema_ras	SDRAM bank A Row Address Select
AF12	mema_we	SDRAM bank A Write Enable
AD6, AE6, AF6, AD5, AF3, AC12, AE13, AF13, AF14, AD13, AE14, AC14, AE15, AC15, AE16, AF16, AD15, AF15, AD14	mema_a[18:0]	SDRAM/SSRAM bank A address bus
AE22, AD22, AF24, AE24, AD25, AC25, AB24, AB26, AB25, AC26, AD26, AE26, AE23, AF23, AD21, AE21	memb_d[15:0]	SDRAM/SSRAM bank B data bus
AF22, AA24	memb_p[1:0]	SDRAM/SSRAM bank B parity bits
W25, W26	memb_cs[1:0]	SSRAM bank B Chip selects 1,0
Y25	memb_rw	SSRAM bank B Read/Write
W24, Y26	memb_bws[1:0]	SSRAM bank B Byte Write Selects 1,0
AC20	memb_cas	SDRAM bank B Column Address Select
AD20	memb_ras	SDRAM bank B Row Address Select
AF21	memb_we	SDRAM bank B Write Enable
AA25, AA26, Y23, Y24, AC21, AE20, AC19, AF20, AE19, AD19, AF19, AE18, AC17, AE17, AD16, AF17, AD17, AF18, AD18	memb_a[18:0]	SDRAM/SSRAM bank B address bus

Pin Description (continued)

EPBGA Pin	Name	Description (see notes 1-8)
		Miscellaneous Pins
AA1	nreset	Global Hardware Reset
AF26, AC24, AB23, AA23, T24, R26, N23, M23	gpio[7:0]	General Purpose I/Os
		Test Pins
A26	trst	Test Reset (Test Pin)
D22	tck	Test Clock (Test Pin)
A25	tdi	Test Data In (Test Pin)
C23	tms	Test Mode Select (Test Pin)
A23	tdo	Test Data Out (Test Pin)
		Phase Lock Loop (PLL) Pins
AB2	pll_clk	PLL clock used for H.100 Master clock generation
AC5	crpll_clk_o	Clock Recovery PLL Output
AF1	crpll_clk_i	Clock Recovery PLL Input
A5	PLLVDD1	PLL Power Pin (3.3V)
AB3	PLLVDD2	PLL Power Pin (3.3V)
AE2	PLLVDD3	PLL Power Pin (3.3V)
B5	PLLGND1	PLL Ground Pin (0V)
AB1	PLLGND2	PLL Ground Pin (0V)
AE1	PLLGND3	PLL Ground Pin (0V)

VSS (0V): D9, D11, E5, E6, E9, E10, E13, E14, E17, E18, E21, E22, F4, F5, F22, H4, J5, J22, K5, K22, L4, L11, L12, L13, L14, L15, L16, M4, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16, N22, P5, P11, P12, P13, P14, P15, P16, P22, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, U5, U22, V5, V22, AA5, AA22, AB5, AB6, AB9, AB10, AB13, AB14, AB17, AB18, AB21, AB22

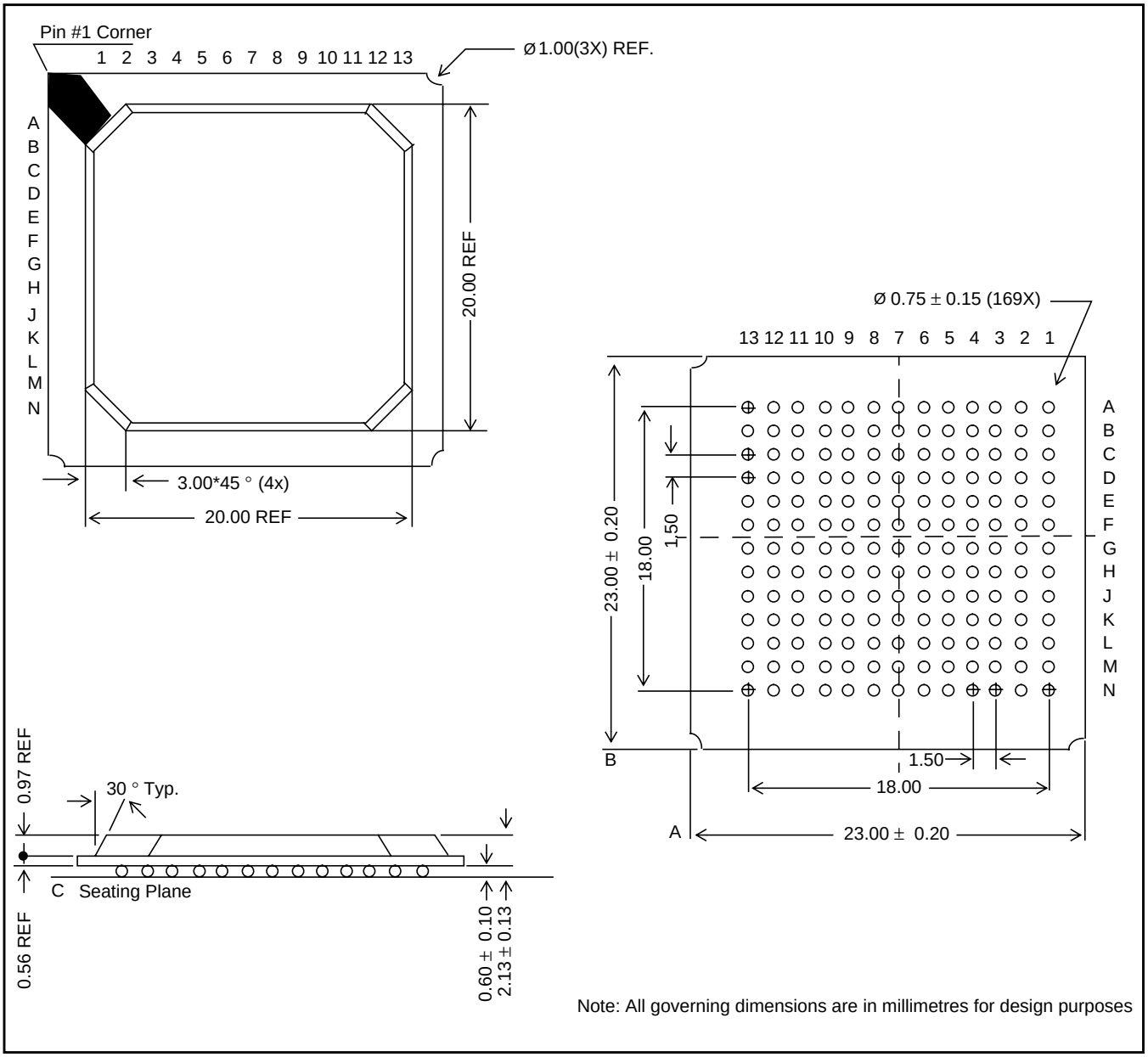
VDD3 (3.3 V): C3, C24, D23, E7, E8, E11, E12, E15, E16, E19, E20, G5, G22, H5, H22, L5, L22, M5, M22, R5, R22, T5, T22, W5, W22, Y5, Y22, AB7, AB8, AB11, AB12, AB15, AB16, AB19, AB20, AC4, AC23, AD3, AD24

If MT90502 is only connected to 3.3V devices on the H.100/H.110 bus, then 3.3V can be connected to the following pins. If any devices are 5V then these pins must be connected to 5V.

VDD5 (3.3 V or 5.0 V): B25, D24, H26, L26, P25, U24

Not Connected (Leave Floating): A20, B16, B18, B19, B23, B24, B26, C4, C5, C16, C22, C26, D16, D19, D26, E23, H23, H25, K23, K25, L25, M26, N24, N26, P26, R23, T23, T25, U25, V25, AA2, AB4, AC6, AC8, AC11, AC13, AC16, AC18, AC22, AD1, AD2, AD4, AD23, AE25, AF25

Notes:
1. All outputs are +3.3 V_{DC}.
2. All input and output pins that are designated (F) can withstand 5 V_{DC} being applied to them.
3. All input and output pins that are designated (F) are tested with a 50 pF load unless otherwise specified.
4. Designations under the “rst” (reset condition) table column are: X = undefined; Z = high impedance; 1 = high (+3.3 V_{DC}).
5. I/O types include: Output (O), Input (I), Bidirectional (I/O), Power (PWR) and Ground (GND).
6. All buses have pins listed in order from MSB to LSB.
7. Pins with more than one function are listed under their main (default) function.8. Unused H.100/H.110 input pins should be tied high with an external pull-up.
8. Unused H.100/H.110 input pins should be tied high with an external pull-up.



Note: All governing dimensions are in millimetres for design purposes

Ball Gate Array

120-BGA	144-BGA	160-BGA
MT90823	MT90863	MT90826

ZARLINK SEMICONDUCTOR

http://www.zarlink.com

World Headquarters - Canada
Tel: +1 (613) 592 0200
Fax: +1 (613) 592 1010

North America - West Coast
Tel: (858) 675-3400
Fax: (858) 675-3450

North America - East Coast
Tel: (978) 322-4800
Fax: (978) 322-4888

Asia/Pacific
Tel: +65 333 6193
Fax: +65 333 6192

Europe, Middle East, and Africa (EMEA)
Tel: +44 (0) 1793 518528
Fax: +44 (0) 1793 518581