SIRENZA MICRODEVICES

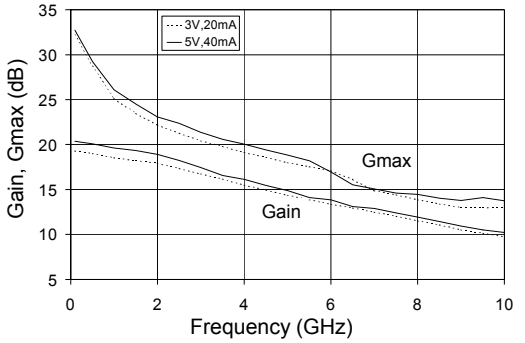
SPF-3043

Low Noise pHEMT GaAs FET

Product Description

Sirenza Microdevices' SPF-3043 is a high performance 0.25µm pHEMT Gallium Arsenide FET. This 300µm device is ideally biased at 3V,20mA for lowest noise performance and battery powered requirements. At 5V,40mA the device can deliver OIP3 of 32dBm. It provides ideal performance as a driver stage in many commercial and industrial LNA applications.

Typical Gain Performance



Product Features

- **DC-10 GHz Operation**
- **0.5 dB NF_{MIN} @ 2 GHz**
- **22 dB G_{MAX} @ 2 GHz**
- **+32 dBm OIP3 (5V,40mA)**
- **+20 dBm P1dB (5V,40mA)**
- **Low Current, Low Cost**
- **Apps circuits available for key bands**

Applications

- **Analog and Digital Wireless Systems**
- **3G, Cellular, PCS**
- **Fixed Wireless, Pager Systems**
- **Driver Stage for Low Power Applications**

Symbol	Device Characteristics	Test Conditions V_{DS}=5V, I_{DQ}=40mA, 25ºC (unless otherwise noted)	Test Frequency	Units	Min.	Typ.	Max.
G_{MAX}	Maximum Available Gain	$Z_S=Z_S^*$, $Z_L=Z_L^*$	0.9 GHz 1.9 GHz	dB		26.5 23.4	
NF_{MIN}	Minimum Noise Figure	$Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$	0.9 GHz 1.9 GHz	dB		0.32 0.54	
S_{21}	Insertion Gain [1]	$Z_S=Z_L=50\Omega$	0.9 GHz	dB	18.5	20.0	21.5
NF	Noise Figure [2]	LNA Application Circuit Board	1.9 GHz	dB		1.05	1.40
Gain	Gain [2]	LNA Application Circuit Board	1.9 GHz	dB	14.0	15.3	
OIP_3	Output Third Order Intercept Point [2]	LNA Application Circuit Board	1.9 GHz	dBm	26.0	28.5	
P_{1dB}	Output 1dB Compression Point [2]	LNA Application Circuit Board	1.9 GHz	dBm	15.0	17.0	
V_P	Pinchoff Voltage [1]	V_{DS}= 2V, I_{DS}= 0.1 mA		V	-1.1	-0.8	-0.5
I_{DSS}	Saturated Drain Current [1]	V_{DS}= 2V, V_{GS}= 0 V		mA	30	60	120
g_m	Transconductance [1]	V_{DS}= 2V, V_{GS}= 0 V		mS	90	150	
BV_{GSO}	Gate-Source Breakdown Voltage [1]	I_{GS}= 0.03 mA, drain open		V		-10	-8
BV_{GDO}	Gate-Drain Breakdown Voltage [1]	I_{GD}= 0.03 mA, source open		V		-10	-8
Rth	Thermal Resistance	junction-to-lead		ºC/W		150	
V_{DS}	Operating Voltage	drain-source		V			5.5
I_{DS}	Operating Current	drain-source		mA			55

[1] 100% tested - DC parameters tested on-wafer, insertion gain tested using a 50 ohm contact board (no matching circuitry) during final production test.
[2] Sample tested - Samples pulled from each wafer/package lot. Sample test specifications are based on statistical data from 500 devices across 5 wafers, 3 wafer lots. The test fixture is an engineering application circuit board (parts are pressed down on the circuit board). The application circuit represents a trade-off between the optimal noise match and input return loss.

522 Almanor Ave., Sunnyvale, CA 94085 Phone: (800) SMI-MMIC http://www.sirenza.com

Junction Temperature Calculation

MTTF is inversely proportional to the device junction temperature. For junction temperature and MTTF considerations the device operating conditions should also satisfy the following expression:

$$P_{DC} < (T_J - T_L) / R_{TH}$$

where:

$P_{DC} = I_{DS} * V_{DS}$ (W)
T_J = Junction Temperature (C)
T_L = Lead Temperature (pin 2) (C)
R_{TH} = Thermal Resistance (C/W)

Biasing Details

The SPF-3043 is a depletion mode FET and requires a negative gate voltage to achieve pinchoff. As such, power supply sequencing circuitry is strongly recommended to prevent damaging bias transients during turn-on. Active bias circuitry is also recommended to maintain a constant drain current from part-to-part.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Current	I_{DS}	60	mA
Forward Gate Current	I_{GSF}	30	µA
Reverse Gate Current	I_{GSR}	30	µA
Drain-to-Source Voltage	V_{DS}	7	V
Gate-to-Source Voltage	V_{GS}	<-3 OR >0	V
RF Input Power	P_{IN}	15	dBm
Storage Temperature Range	T_{stor}	-40 TO +150	C
Power Dissipation	P_{DISS}	420	mW
Junction Temperature	T_J	+150	C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page 1.

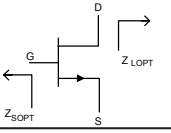
Typical Performance - Engineering Application Circuits (See App Note AN-043)

Freq (GHz)	V_{DS} (V)	I_{DQ} (mA)	NF (dB)	Gain (dB)	P1dB (dBm)	OIP3[3] (dBm)	S11 (dB)	S22 (dB)	Configuration	Comments
0.90	5	40	1.00	19.3	19.0	29.0	-10	-15	Single-Ended	0.85-0.96 GHz, dual-supply
0.90	5	80	0.75	23.3	19.9	30.0	-20	-20	Balanced	0.8-1.0 GHz, dual-supply
1.90	5	40	1.05	15.3	17.0	28.5	-10	-15	Single-Ended	1.8-2.0 GHz, dual-supply
1.90	5	80	0.95	20.0	23.0	32.5	-20	-20	Balanced	1.8-2.0 GHz, dual-supply
2.14	5	40	1.80	15.3	18.5	30.0	-20	-8	Single-Ended	2.1-2.2 GHz, dual-supply
2.45	5	40	1.25	14.9	18.5	27.5	-15	-18	Single-Ended	2.4-2.5 GHz, dual-supply
5.50	5	40	1.30	15.5	18.0	29.0	-18	-18	Single-Ended	5.1-5.9 GHz, dual-supply

[3] P_{OUT}= 0 dBm per tone, 1MHz tone spacing

Refer to the application note for additional RF data, PCB layouts, BOMs, biasing instructions, and other key issues to be considered. For the latest application note please visit our site at www.sirenza.com.

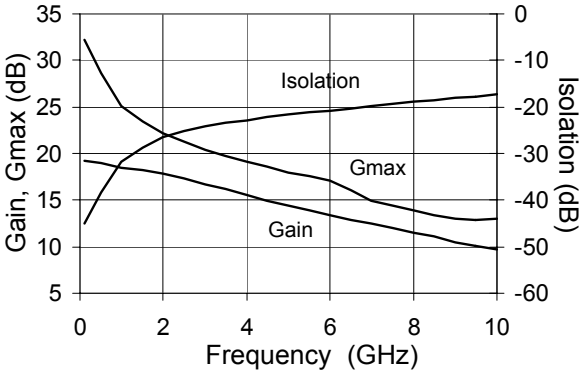
Peak RF Performance Under Optimum Matching Conditions

Freq (GHz)	V_{DS} (V)	I_{DQ} (mA)	NF_{MIN} [4] (dB)	Gmax (dB)	P1dB [5] (dBm)	OIP3 [6] (dBm)	
0.90	3	20	0.25	25.5	15.5	29	
	5	40	0.32	26.5	20.0	32	
1.90	3	20	0.50	22.4	15.5	29	
	5	40	0.54	23.3	20.0	32	

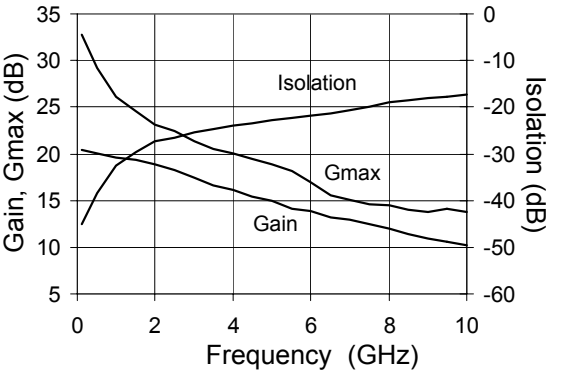
[4] $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$, The input matching circuit losses have been de-emebedded.
[5] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$, where Z_{SOPT} and Z_{LOPT} have been tuned for max P1dB
[6] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$, where Z_{SOPT} and Z_{LOPT} have been tuned for max OIP3
Note: Optimum NF, P1dB, and OIP3 performance cannot be achieved simultaneously.

Typical Performance - De-embedded S-Parameters

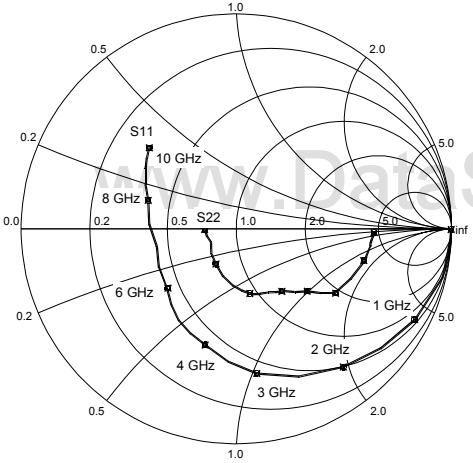
Gain vs Frequency (3V,20mA)



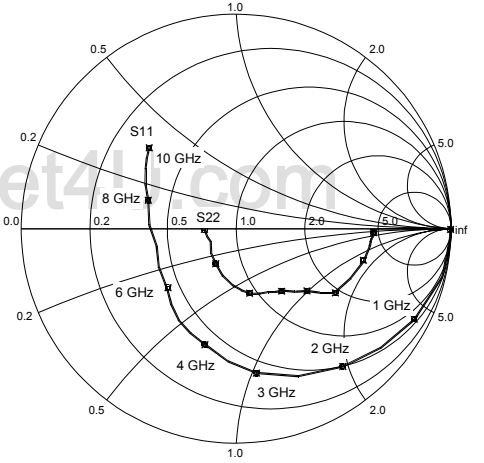
Gain vs Frequency (5V,40mA)



S11,S22 vs Frequency (3V,20mA)



S11,S22 vs Frequency (5V,40mA)



Note: S-parameters are de-embedded to the device leads with $Z_S=Z_L=50\Omega$. The device was mounted on a 0.010" PCB with plated-thru holes close to pins 2 and 4. De-embedded s-parameters can be downloaded from our website (www.sirenza.com).

Typical Performance - Noise Parameters

Freq (GHz)	V_{DS} (V)	I_{DS} (mA)	NF_{MIN} [7] (dB)	Γ_{OPT} Mag ∠ Ang	r_N	Gmax (dB)
0.90	3	20	0.25	0.79 ∠ 12	0.22	25.5
	5	40	0.32	0.75 ∠ 12	0.25	26.5
1.90	3	20	0.50	0.62 ∠ 34	0.19	22.4
	5	40	0.54	0.62 ∠ 33	0.20	23.3

[7] $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$, NF_{MIN} is a noise parameter for which the input matching circuit losses have been de-emebedded. The noise parameters were measured using a Maury Microwave Automated Tuner System. The device was mounted on a 0.010" PCB with plated-thru holes close to pins 2 and 4.

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

SPF-3043 Low Noise pHEMT GaAs FET

Pin Description

Pin #	Function	Description
1	Gate	RF Input / Gate Bias
2	Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output / Drain Bias
4	Source	Same as Pin 2

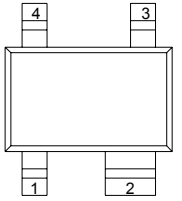
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SPF-3043	7"	3000

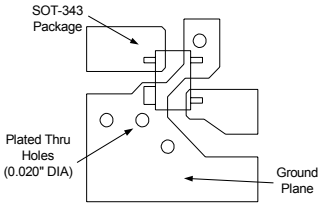
Part Symbolization

The part will be symbolized with the "F3" designator and a dot signifying pin 1 on the top surface of the package.

Pin Designation

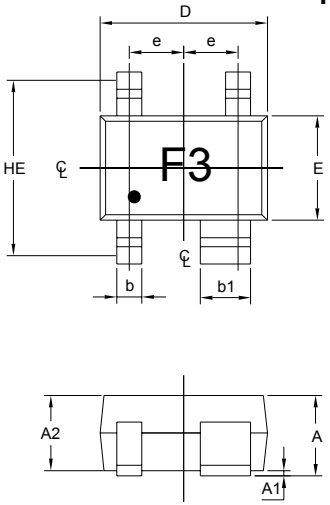


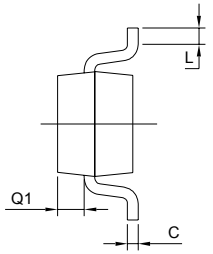
Recommended PCB Layout



Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.

Package Dimensions





NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70.
5. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM. ie :REVERSE TRIM/FORM.
6. PACKAGE SURFACE TO BE MIRROR FINISH.

SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.10	0.30