



PD54008 - PD54008S

RF POWER TRANSISTORS

The *LdmoST* Plastic FAMILY

PRELIMINARY DATA

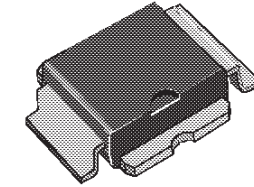
N-CHANNEL ENHANCEMENT-MODE LATERAL MOSFETs

- EXCELLENT THERMAL STABILITY
- COMMON SOURCE CONFIGURATION
- POUT = 8 W with 10 dB gain @ 500 MHz / 7.5V
- NEW RF PLASTIC PACKAGE

DESCRIPTION

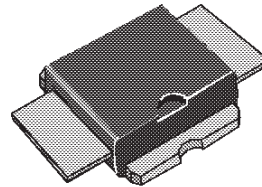
The PD54008 is a common source N-Channel, enhancement-mode, lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 7V in common source mode at frequencies of up to 1GHz. PD54008 boasts the excellent gain, linearity and reliability of ST's latest LDMOS technology mounted in the first true SMD plastic RF power package, PowerSO-10RF. PD54008's superior linearity performance makes it an ideal solution for portable radio.

The PowerSO-10 plastic package, designed to offer high reliability, is the first ST JEDEC approved, high power SMD package. It has been specially optimized for RF needs and offers excellent RF performances and ease of assembly.



PowerSO-10RF
(Formed Lead)

ORDER CODE	BRANDING
PD54008	XPD54008



PowerSO-10RF
(Straight Lead)

ORDER CODE	BRANDING
PD54008S	XPD54008S

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25 °C)

Symbol	Parameter	Value	Unit
V _{(BR)DSS}	Drain Source Voltage	25	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Drain Current	5	A
P _{DISS}	Power Dissipation (@ T _c = 70 °C)	73	W
T _j	Max. Operating Junction Temperature	165	°C
T _{STG}	Storage Temperature	-65 to 165	°C

THERMAL DATA

R _{th(j-c)}	Junction-Case Thermal Resistance	1.3	°C/W
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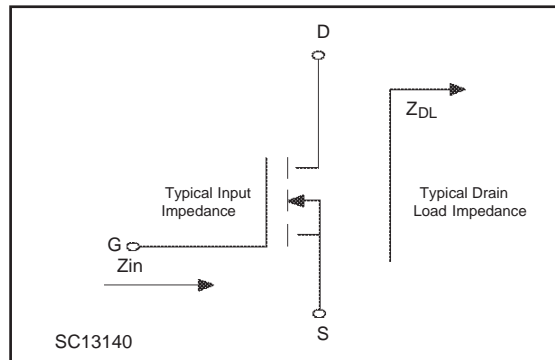
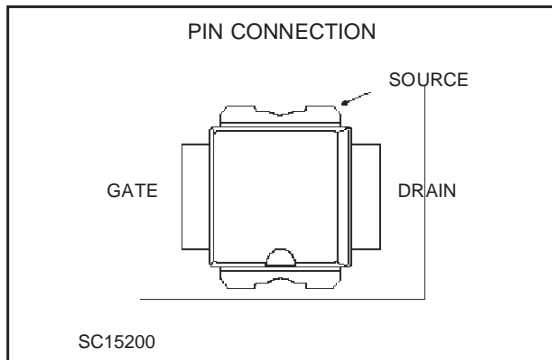
ELECTRICAL SPECIFICATION ($T_{CASE} = 25\text{ }^{\circ}\text{C}$)

STATIC

Symbol	Parameter			Min.	Typ.	Max.	Unit
I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$				1	μA
I_{GSS}	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$				1	μA
$V_{GS(Q)}$	$V_{DS} = 10\text{ V}$	$I_D = 150\text{ mA}$		2.0		5.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 2\text{ A}$				0.7	V
g_{FS}	$V_{DS} = 10\text{ V}$	$I_D = 2\text{ A}$		2.0	2.5		mho
C_{ISS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 7.5\text{ V}$	$f = 1\text{ MHz}$		91		pF
C_{OSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 7.5\text{ V}$	$f = 1\text{ MHz}$		68		pF
C_{RSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 7.5\text{ V}$	$f = 1\text{ MHz}$		8.5		pF

DYNAMIC

Symbol	Parameter				Min.	Typ.	Max.	Unit
P_{OUT}	$f = 500\text{ MHz}$	$V_{DD} = 7.5\text{ V}$	$I_{DQ} = 150\text{ mA}$		8			W
G_{PS}	$f = 500\text{ MHz}$	$V_{DD} = 7.5\text{ V}$	$P_{OUT} = 8\text{ W}$	$I_{DQ} = 150\text{ mA}$		10		dB
η_D	$f = 500\text{ MHz}$	$V_{DD} = 7.5\text{ V}$	$P_{OUT} = 8\text{ W}$	$I_{DQ} = 150\text{ mA}$		50		%
LOAD Mismatch	$f = 500\text{ MHz}$	$V_{DD} = 9.5\text{ V}$	$P_{OUT} = 8\text{ W}$	$I_{DQ} = 150\text{ mA}$	20:1			VSWR
	ALL PHASE ANGLES							



IMPEDANCE DATA

PD54008

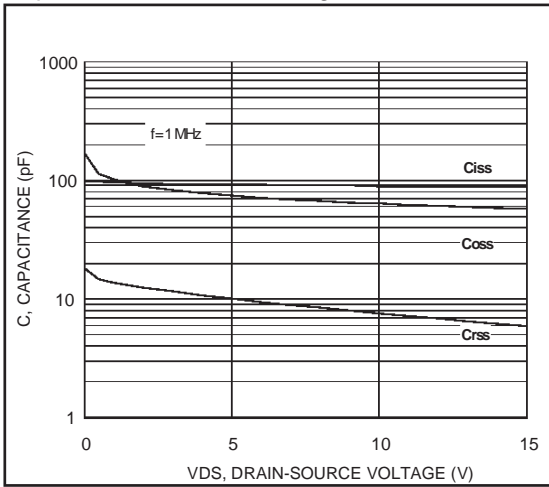
Frequency MHz	Z_{in} Ω	Z_{dl} Ω
480	$2.00 - j1.44$	$1.41 - j.38$
500	$1.92 - j1.21$	$1.58 - j.70$
520	$2.18 - j.88$	$1.61 - j1.05$

PD54008S

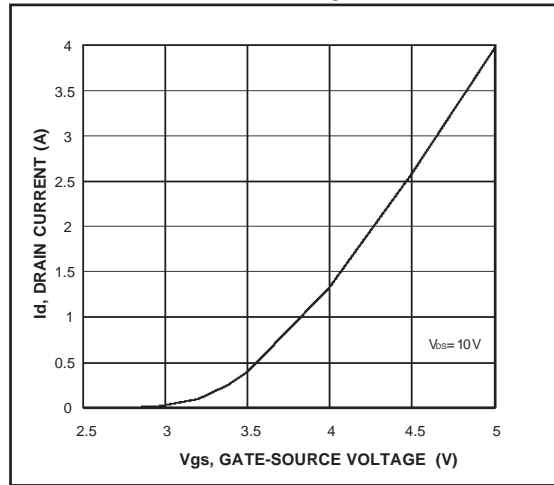
Frequency MHz	Z_{in} Ω	Z_{dl} Ω
480	$1.69 - j1.48$	$1.65 - j.40$
500	$1.63 - j1.40$	$1.49 - j.09$
520	$1.75 - j.71$	$1.36 - j.88$

TYPICAL PERFORMANCE

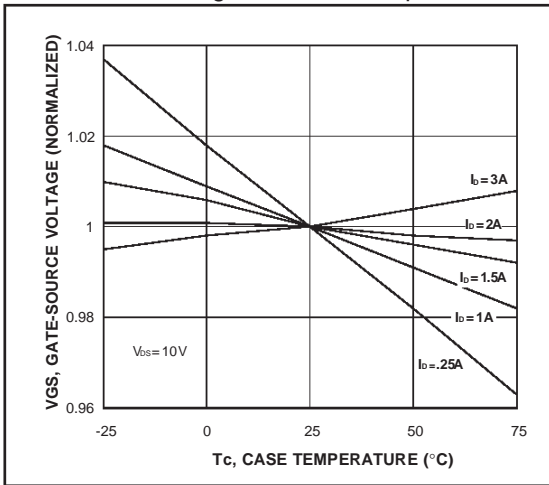
Capacitance vs. Drain Voltage



Drain Current vs. Gate Voltage



Gate-Source Voltage vs. Case Temperature

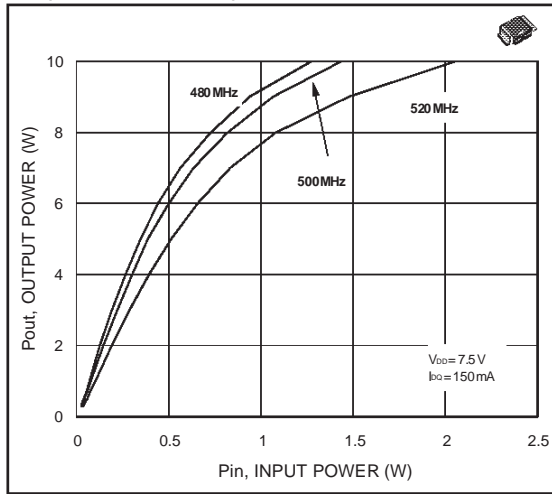


PD54008 - PD54008S

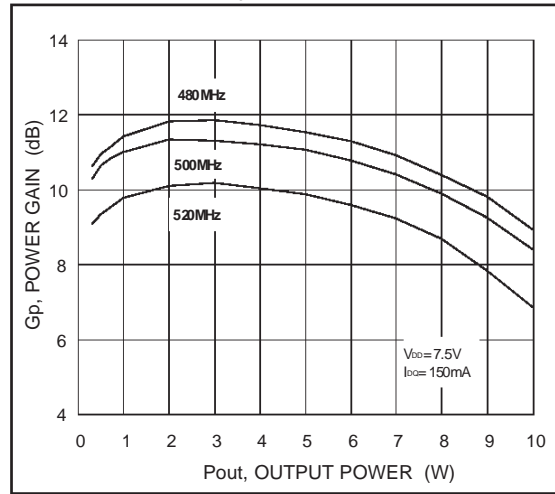
TYPICAL PERFORMANCE

Output Power vs. Input Power

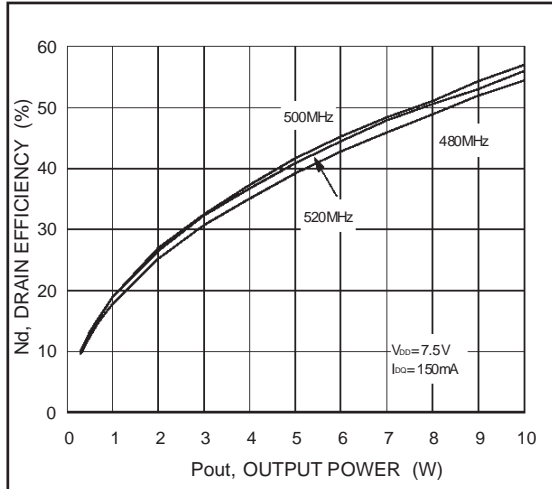
PD54008



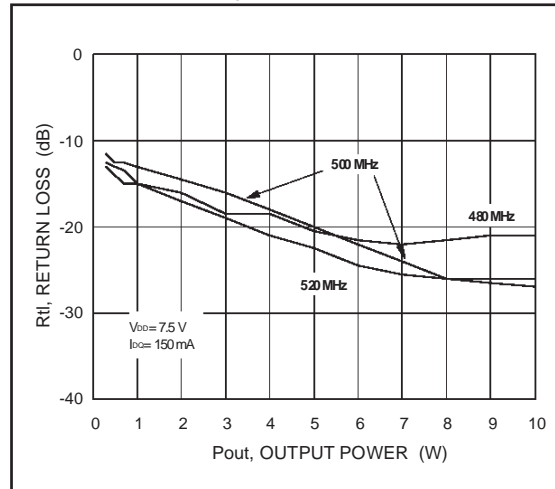
Power Gain vs. Output Power



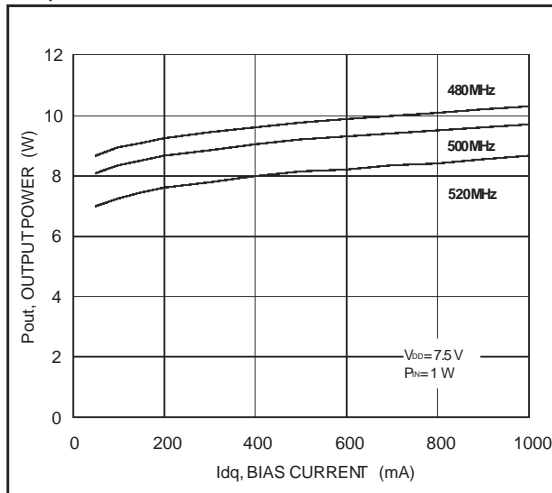
Drain Efficiency vs. Output Power



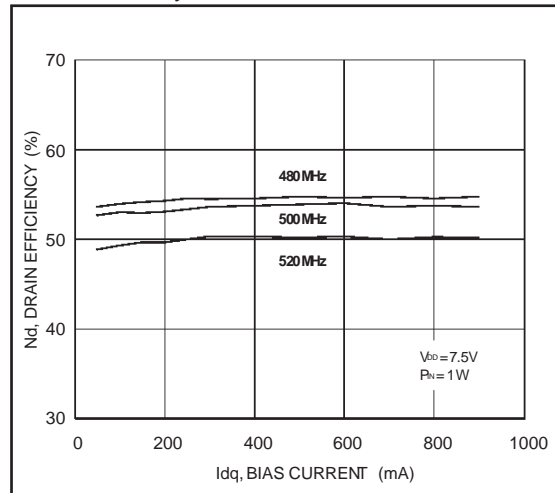
Return Loss vs. Output Power



Output Power vs. Bias Current

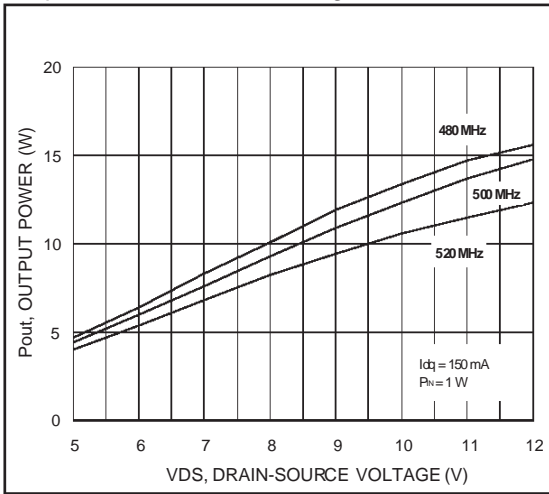


Drain Efficiency vs. Bias Current

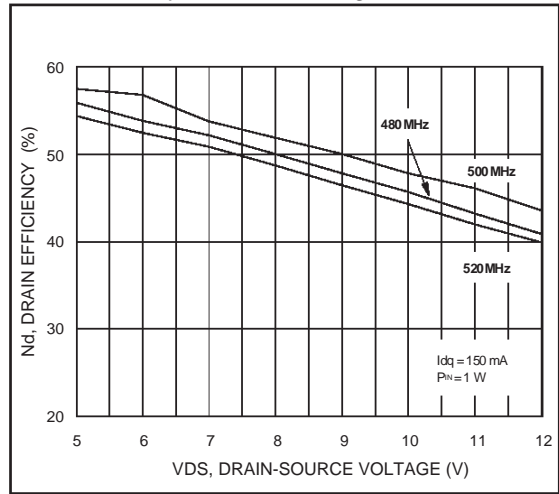


TYPICAL PERFORMANCE

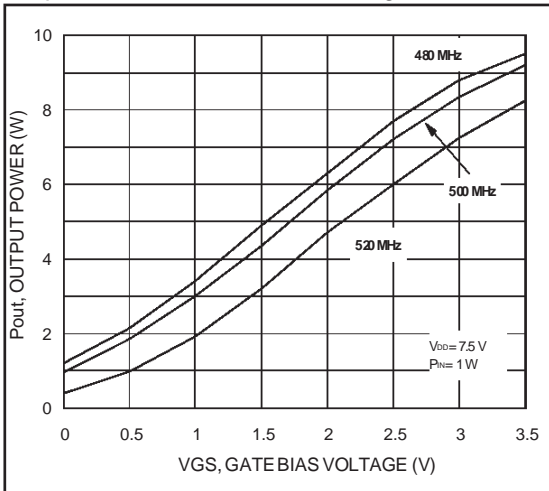
Output Power vs. Drain Voltage



Drain Efficiency vs. Drain Voltage

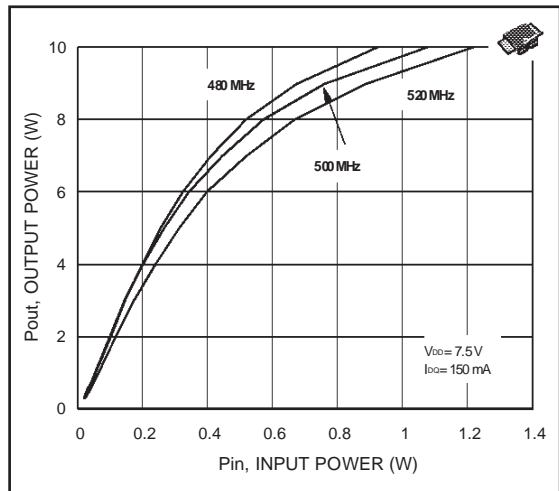


Output Power vs. Gate Bias Voltage

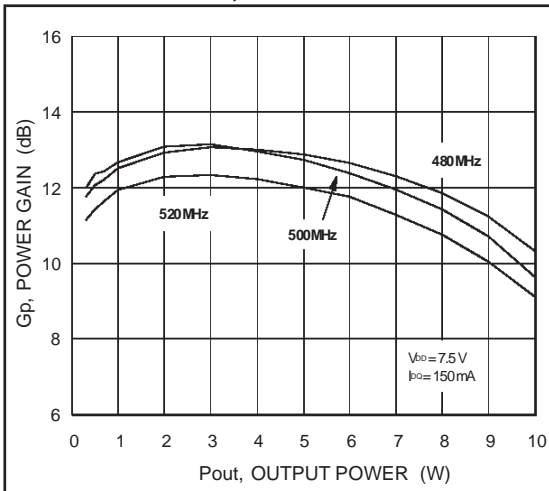


Output Power vs. Input Power

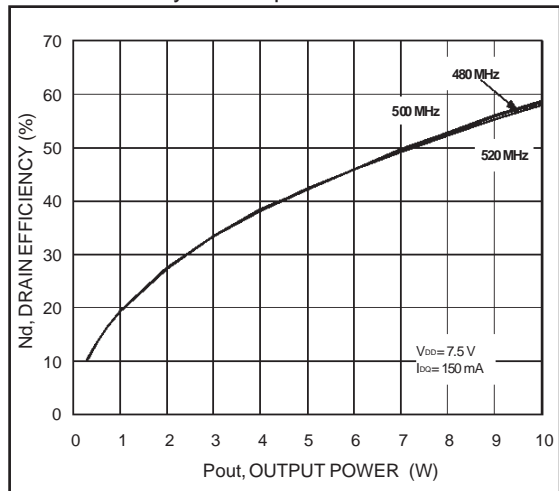
PD54008S



Power Gain vs. Output Power



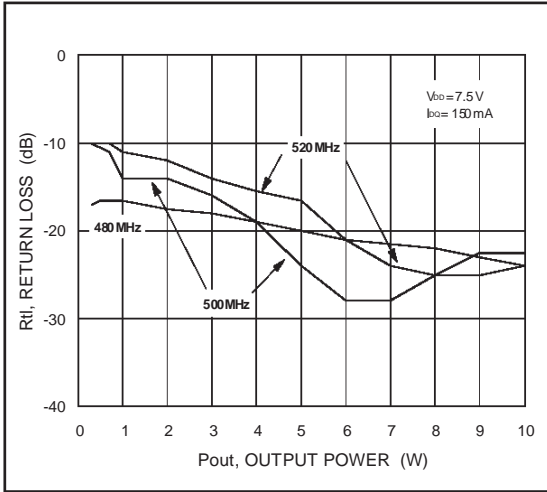
Drain Efficiency vs. Output Power



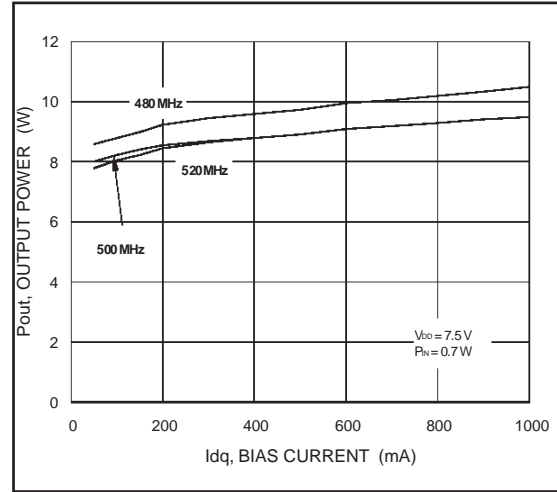
PD54008 - PD54008S

TYPICAL PERFORMANCE

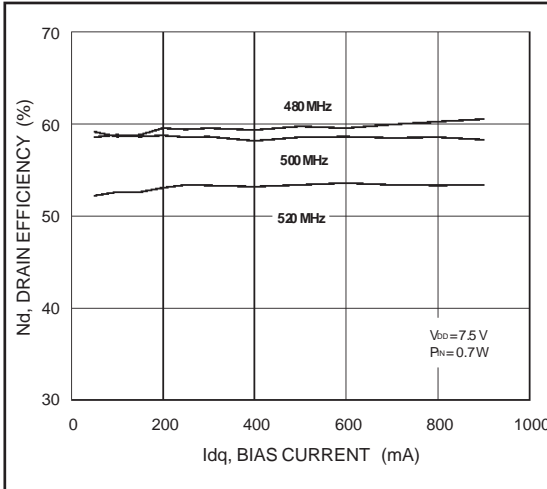
Return Loss vs. Output Power



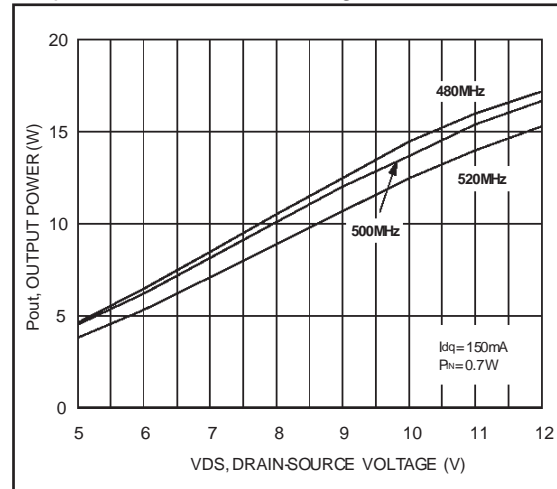
Output Power vs. Bias Current



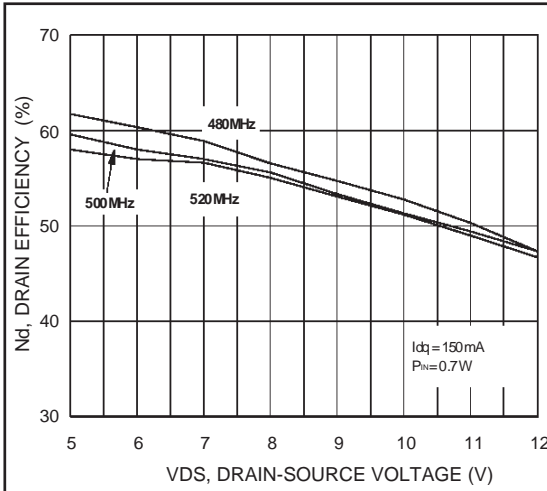
Drain Efficiency vs. Bias Current



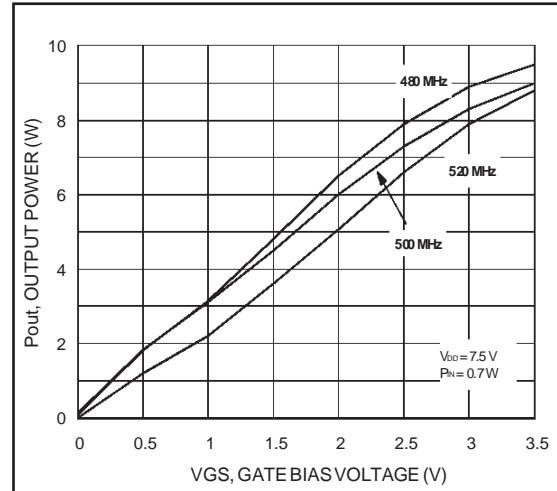
Output Power vs. Drain Voltage



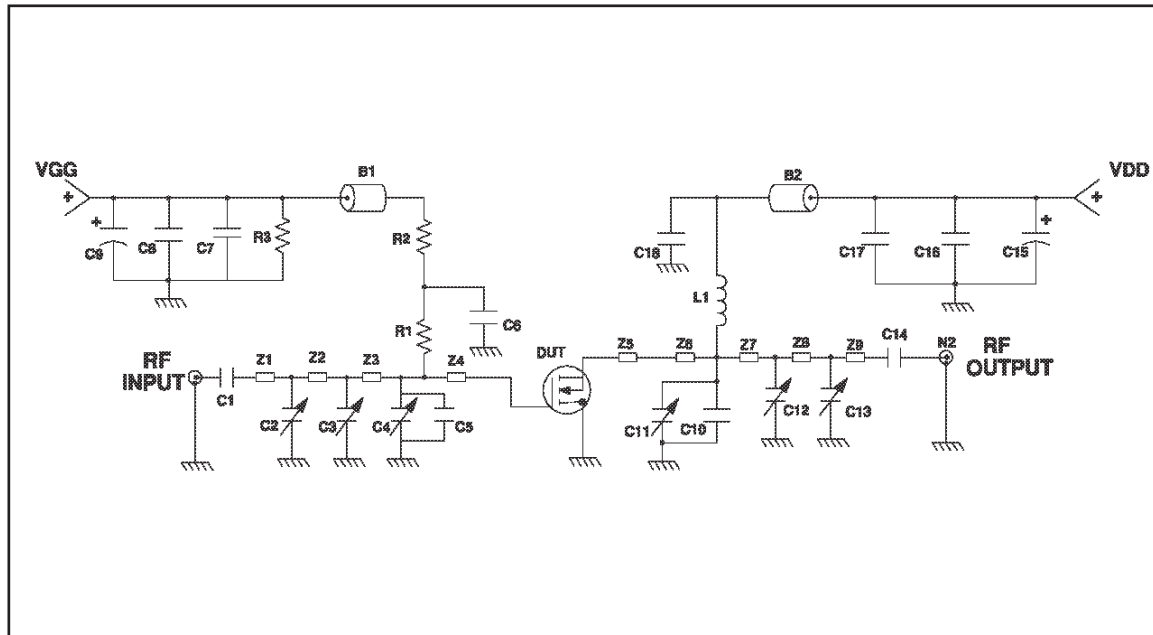
Drain Efficiency vs. Drain Voltage



Output Power vs. Gate Bias Voltage



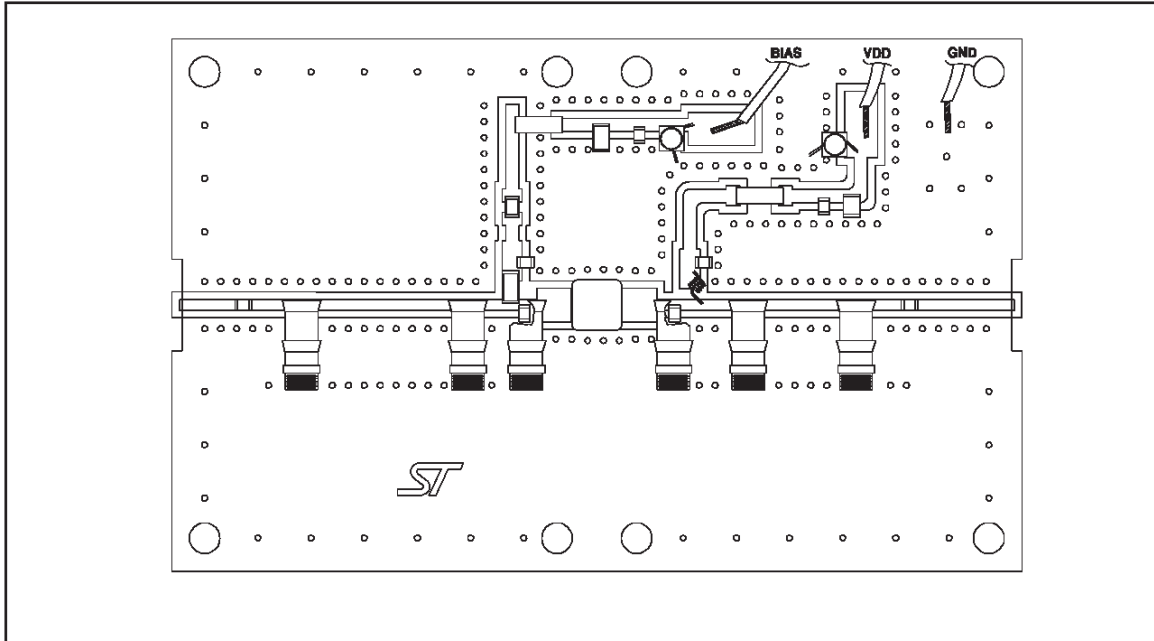
TEST CIRCUIT SCHEMATIC



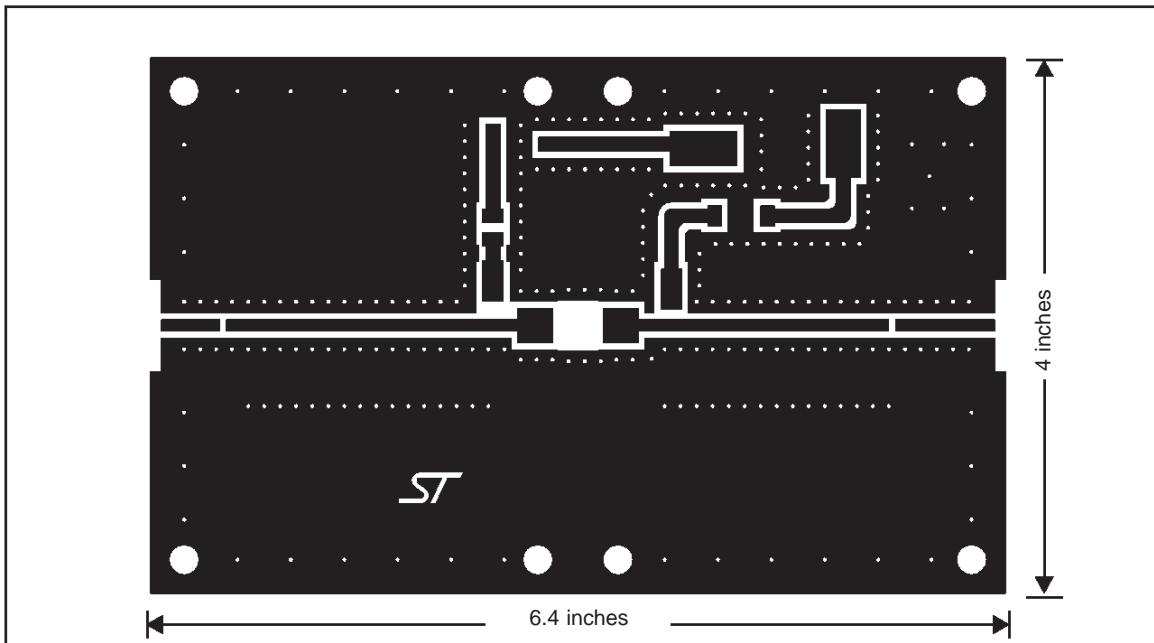
TEST CIRCUIT COMPONENT PART LIST

B1,B2	FERRITE BEAD	R2	1,0k Ω , 1W CHIP RESISTOR
C1,C14	300pF, 100 mil CHIP CAPACITOR	R3	33 k Ω , 1W CHIP RESISTOR
C2,C3,C4,C11, C12,C13	1 TO 20 pF TRIMMER CAPACITOR	Z1	0.471" X 0.080" MICROSTRIP
C6,C18	pF 100 mil CHIP CAP	Z2	1.082" X 0.080" MICROSTRIP
C9,C15	10 μ F, 50V ELECTROLYTIC CAPACITOR	Z3	0.372" X 0.080" MICROSTRIP
C8,C16	0.1mF, 100 mil CHIP CAP	Z4,Z5	0.260" X 0.223" MICROSTRIP
C7,C17	1,000pF 100 mil CHIP CAP	Z6	0.050" X 0.080" MICROSTRIP
C5, C10	33pF, 100 mil CHIP CAP	Z7	0.551" X 0.080" MICROSTRIP
L1	56nH, 7 TURN, COILCRAFT	Z8	0.825" X 0.080" MICROSTRIP
N1,N2	TYPE N FLANGE MOUNT	Z9	0.489" X 0.080" MICROSTRIP
R1	15 Ω , 1W CHIP RESISTOR	BOARD	ROGER, ULTRA LAM 2000 THK 0.030" $\epsilon_r = 2.55$ 2oz ED Cu 2 SIDES

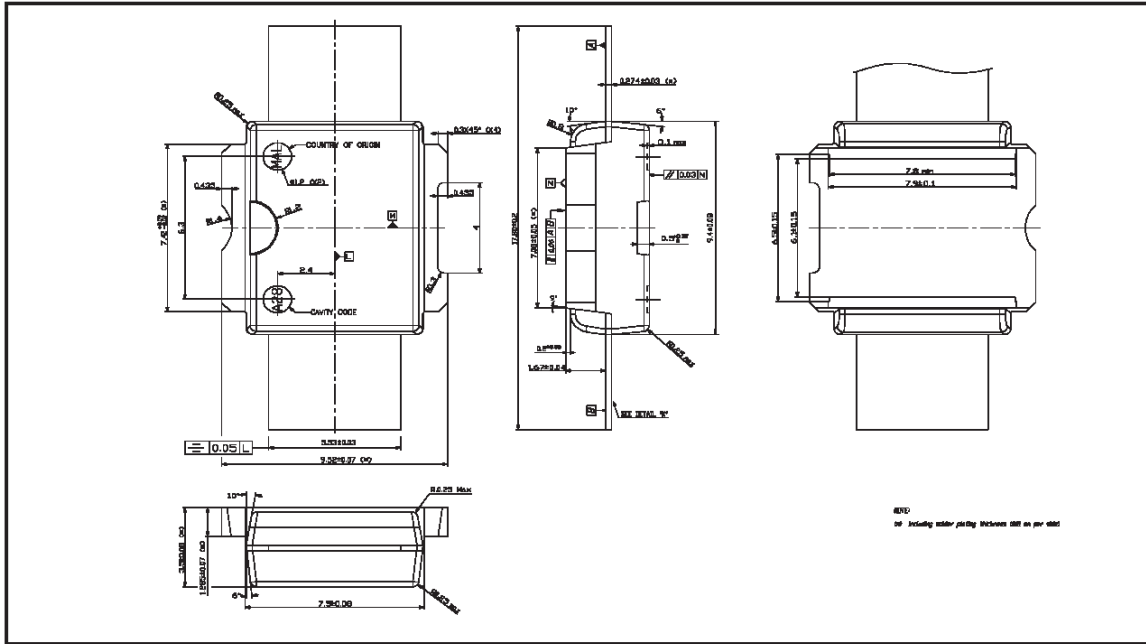
TEST CIRCUIT



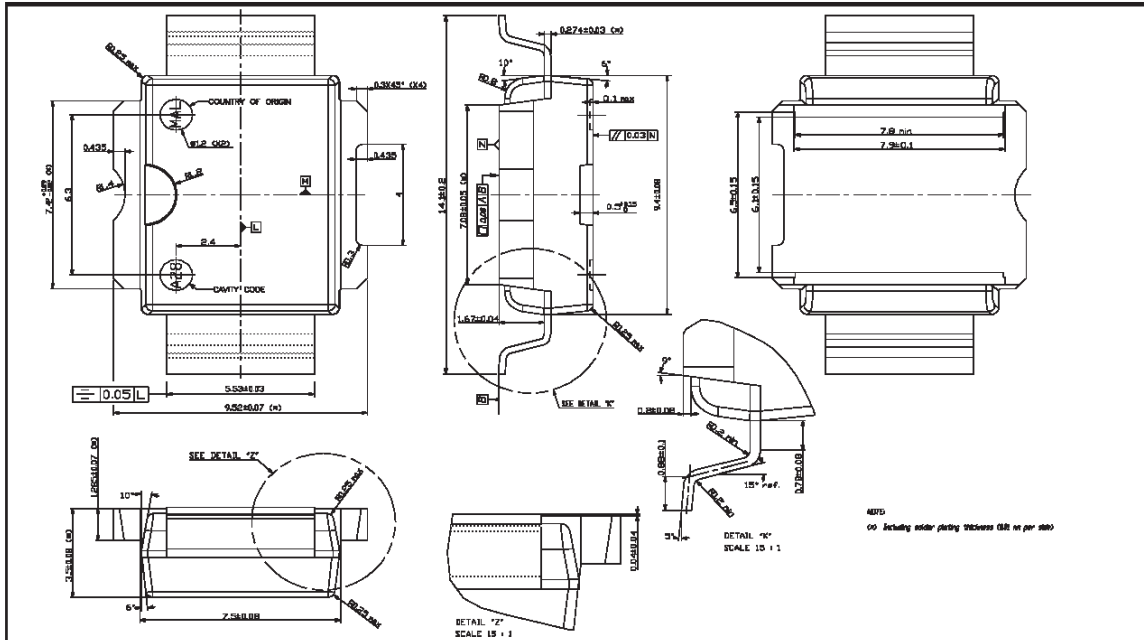
TEST CIRCUIT PHOTOMASTER



PowerSO-10RF (Straight Lead) MECHANICAL DATA



PowerSO-10RF (Formed Lead) MECHANICAL DATA



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