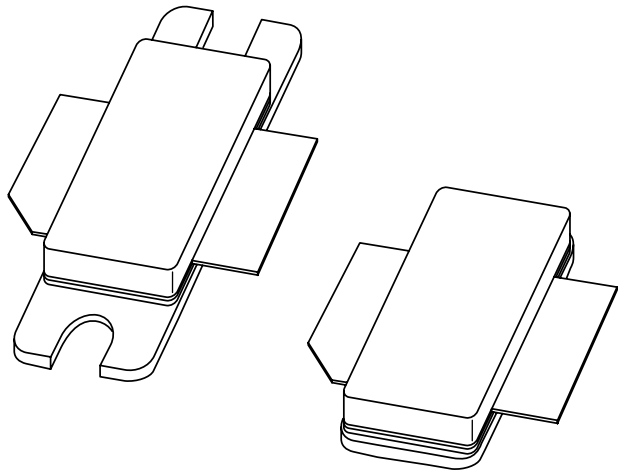
DATA SHEET



BLF0810-90; BLF0810S-90
Base station LDMOS transistors

Product specification
Supersedes data of 2003 May 09

2003 Jun 12

Philips
Semiconductors

Base station LDMOS transistors BLF0810-90; BLF0810S-90

FEATURES

- Typical CDMA IS95 performance at standard settings with a supply voltage of 27 V and I_{DQ} of 560 mA. Adjacent channel bandwidth is 30 kHz, adjacent channel at ± 750 kHz:
  - Output power = 15 W (AV)
  - Gain = 16 dB
  - Efficiency = 27%
  - ACPR = –46 dBc at 750 kHz and BW = 30 kHz
- 70 W CW performance
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 to 1000 MHz)
- Internally matched for ease of use.

APPLICATIONS

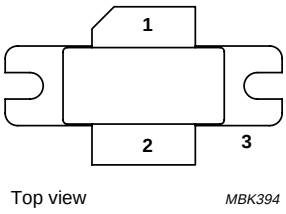
- RF power amplifier for GSM, EDGE and CDMA base stations and multicarrier operations in the 800 to 1000 MHz frequency range.

DESCRIPTION

90 W LDMOS power transistor for base station applications at frequencies from 800 to 1000 MHz.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange

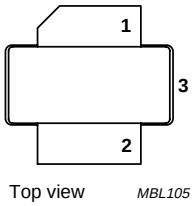


Top view MBK394

Fig.1 Simplified outline SOT502A (BLF0810-90).

PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



Top view MBL105

Fig.2 Simplified outline SOT502B (BLF0810S-90)

QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR 750 (dBc)
Class-AB (2-tone)	f_1 = 890.0; f_2 = 890.1	27	70 (PEP)	16	39	–28	–
CDMA (IS95)	890	27	15 (AV)	16	27	–	–46

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	75	V
V_{GS}	gate-source voltage	–	±15	V
T_{stg}	storage temperature	–65	150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	T_h = 25 °C, P_L = 35 W (AV), note 1	1	K/W
$R_{th\ j\text{-}hs}$	thermal resistance from heatsink to junction	T_h = 25 °C, P_L = 35 W (AV), note 2	1.3	K/W

Notes

1. Thermal resistance is determined under RF operating conditions.
2. Depending on mounting condition in application.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

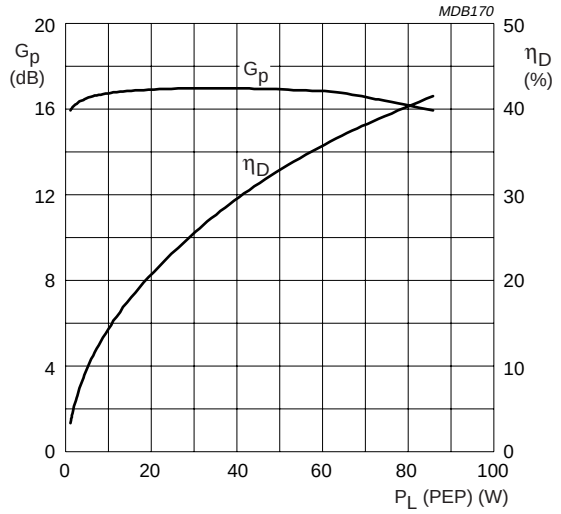
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 36 V	–	–	1.5	µA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	24	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	0.5	µA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	–	4.4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	–	120	–	mΩ

APPLICATION INFORMATION

RF performance in a common source class-AB circuit.

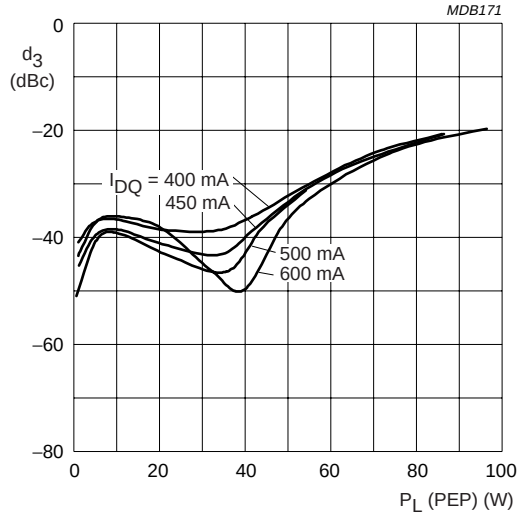
V_{DS} = 27 V; I_{DQ} = 560 mA; f = 890 MHz; T_h = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mode of operation: 2-tone CW, 100 kHz spacing						
G_p	gain power	P_L = 45 W (PEP)	15	16.5	–	dB
η_D	drain efficiency		29	32	–	%
IRL	input return loss		–	–10	–6	dB
d_3	third order intermodulation distortion		–	–40	–	dBc
G_p	gain power	P_L = 63 W (PEP)	–	16.5	–	dB
η_D	drain efficiency		33	38	–	%
d_3	third order intermodulation distortion		–	–32	–27	dBc
	ruggedness	VSWR = 10 : 1 through all phases; P_L = 125 W (PEP)	no degradation in output power			
Mode of operation: CDMA, IS95 (pilot, paging, sync and traffic codes 8 to 13)						
G_p	gain power	P_L = 15 W (AV)	–	16	–	dB
η_D	drain efficiency	P_L = 15 W (AV)	–	27	–	%
ACPR 750	adjacent channel power ratio	at BW = 30 kHz	–	–46	–	dBc



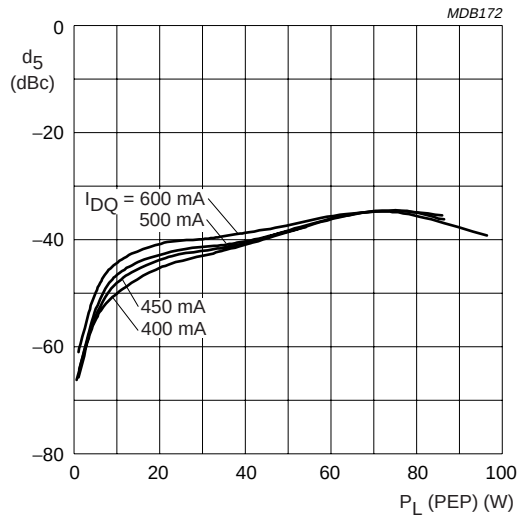
V_{DS} = 27 V; I_{DQ} = 560 mA; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

Fig.3 Power gain and efficiency as functions of peak envelope power, typical values.



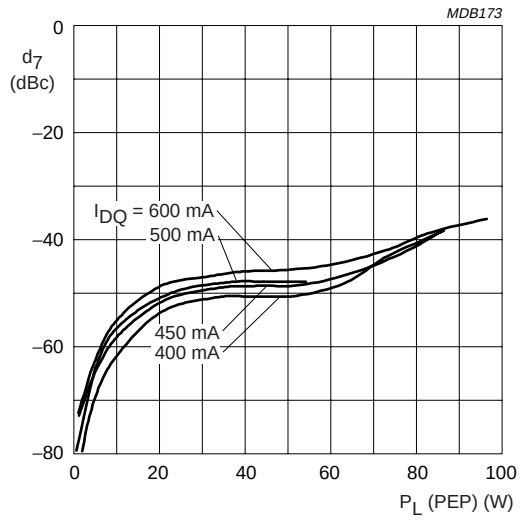
V_{DS} = 27 V; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

Fig.4 Third order intermodulation distortion as a function of peak envelope power, typical values.



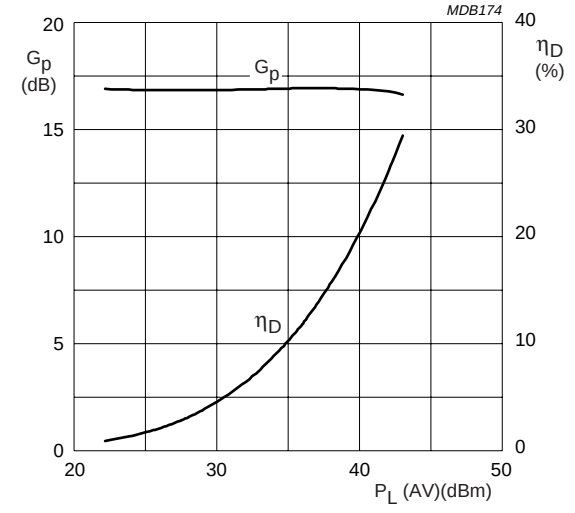
V_{DS} = 27 V; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

Fig.5 Fifth order intermodulation distortion as a function of peak envelope power; typical values.



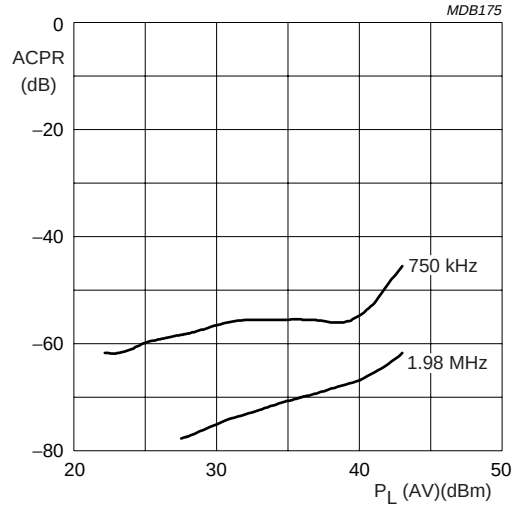
V_{DS} = 27 V; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

Fig.6 Seventh order intermodulation distortion as a function of peak envelope power; typical values.



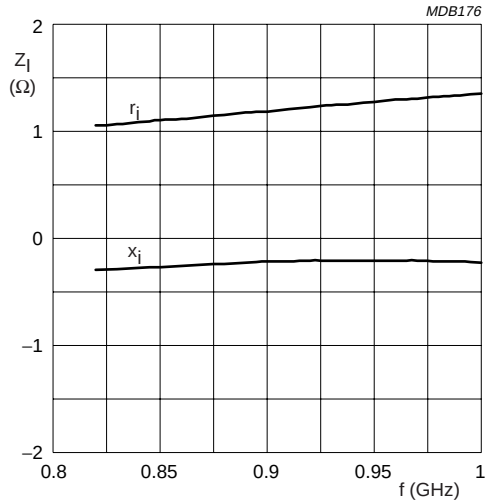
V_{DS} = 27 V; I_{DQ} = 560 mA; f = 890 MHz.
measured under CDMA conditions; test signal standard IS-95.

Fig.7 Power gain and drain efficiency as functions of average load power; typical values.



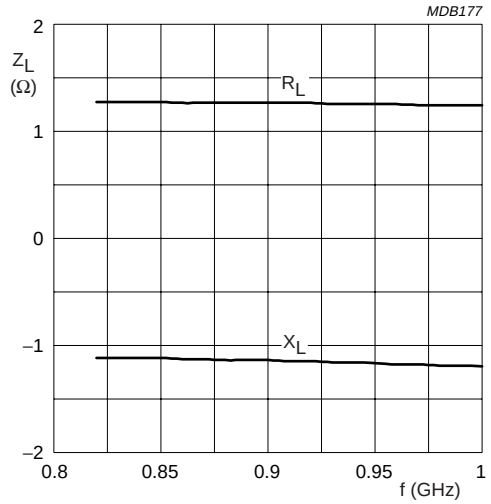
V_{DS} = 27 V; I_{DQ} = 560 mA; f = 890 MHz.
measured under CDMA conditions; test signal standard IS-95.

Fig.8 ACPR as a function of average load power; typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 560 mA; P_L = 18 W.
Values comprised for different parameters.

Fig.9 Input impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 560 mA; P_L = 18 W.
Values comprised for different parameters.

Fig.10 Input impedance as a function of frequency (series components); typical values.

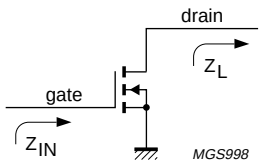


Fig.11 Definition of transistor impedance.

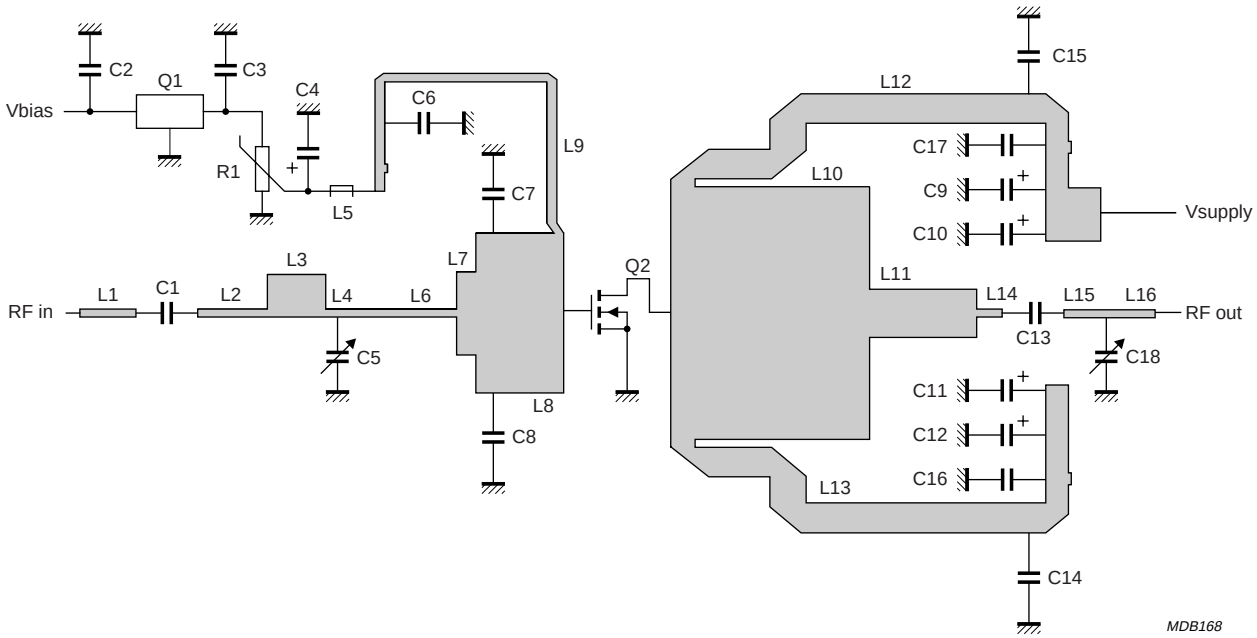
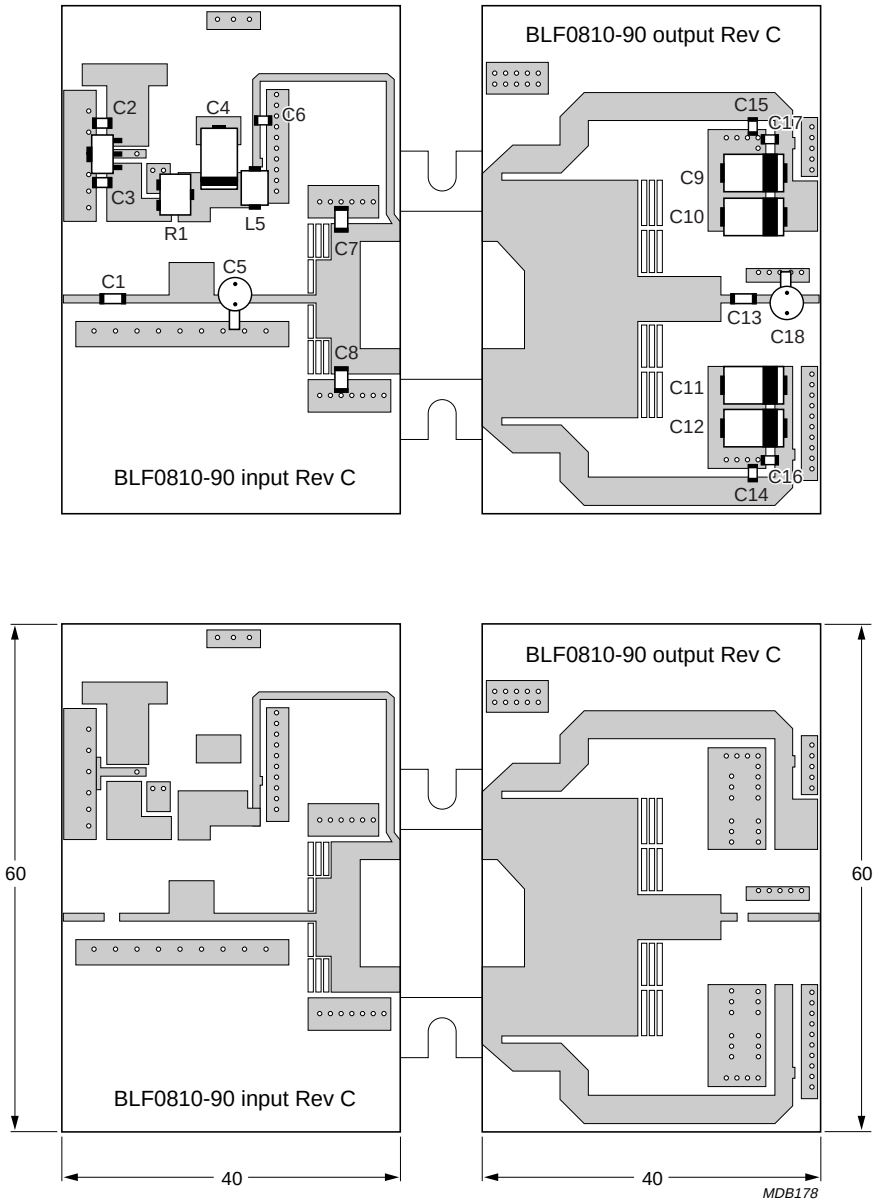


Fig.12 Test circuit for 860 to 900 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 25 mm. The other side is unetched and serves as a ground plane.

Fig.13 Component layout for 860 to 900 MHz test circuit.

List of components (see Figs 12 and 13)

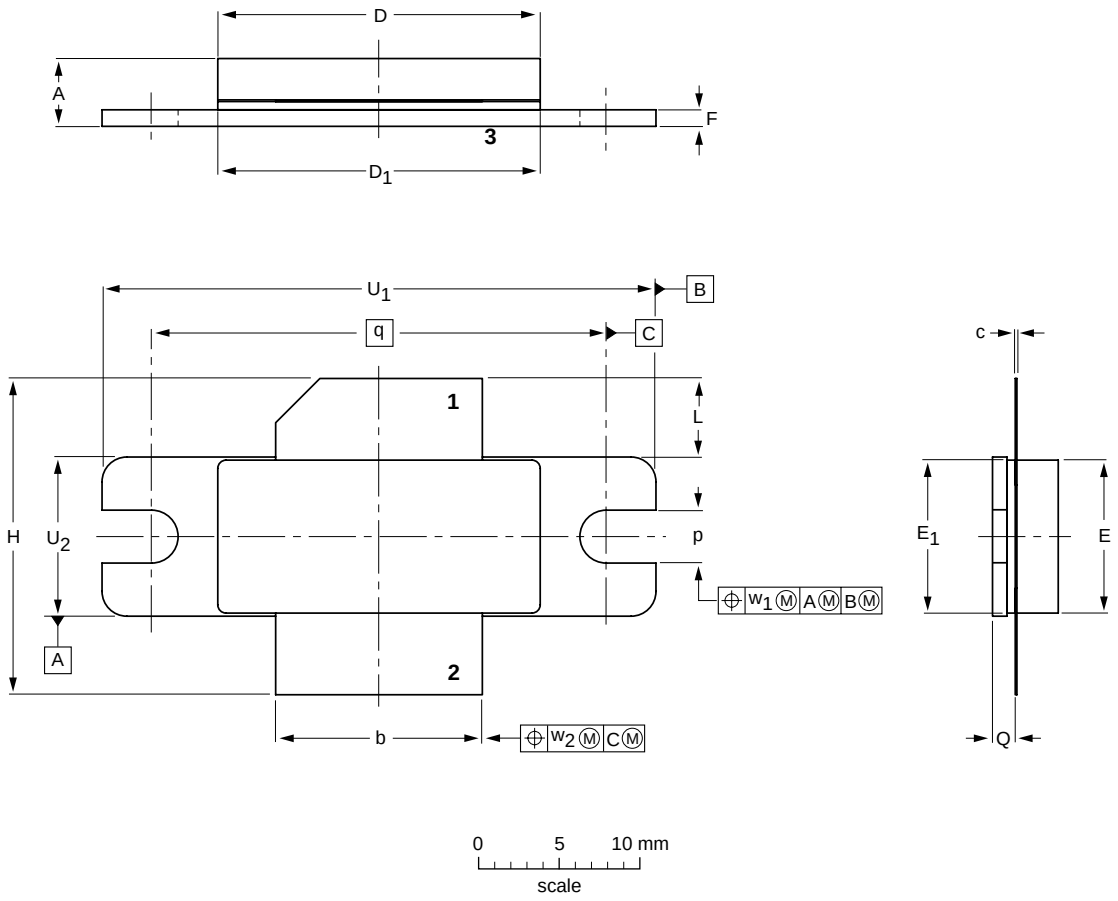
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μF	
C5, C18	air trimmer capacitor	8 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 kΩ	
Q1	7808 voltage regulator		
Q2	BLF0810-90/BLF0810S-90 LDMOS transistor		
L1	stripline; note 2		5.22 × 0.92 mm
L2	stripline; note 2		6.47 × 0.92 mm
L3	stripline; note 2		5.38 × 4.8 mm
L4	stripline; note 2		2.4 × 0.92 mm
L5	ferroxcube		
L6	stripline; note 2		9.73 × 0.92 mm
L7	stripline; note 2		1.82 × 9.3 mm
L8	stripline; note 2		8.15 × 17.9 mm
L9	stripline; note 2		44 × 0.92 mm
L10	stripline; note 2		18.45 × 28.3 mm
L11	stripline; note 2		9.95 × 5.38 mm
L12, L13	stripline; note 2		37.6 × 3.35 mm
L14	stripline; note 2		2.36 × 0.92 mm
L15, L16	stripline; note 2		4.22 × 0.92 mm

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 0.64 mm.

PACKAGE OUTLINES

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**

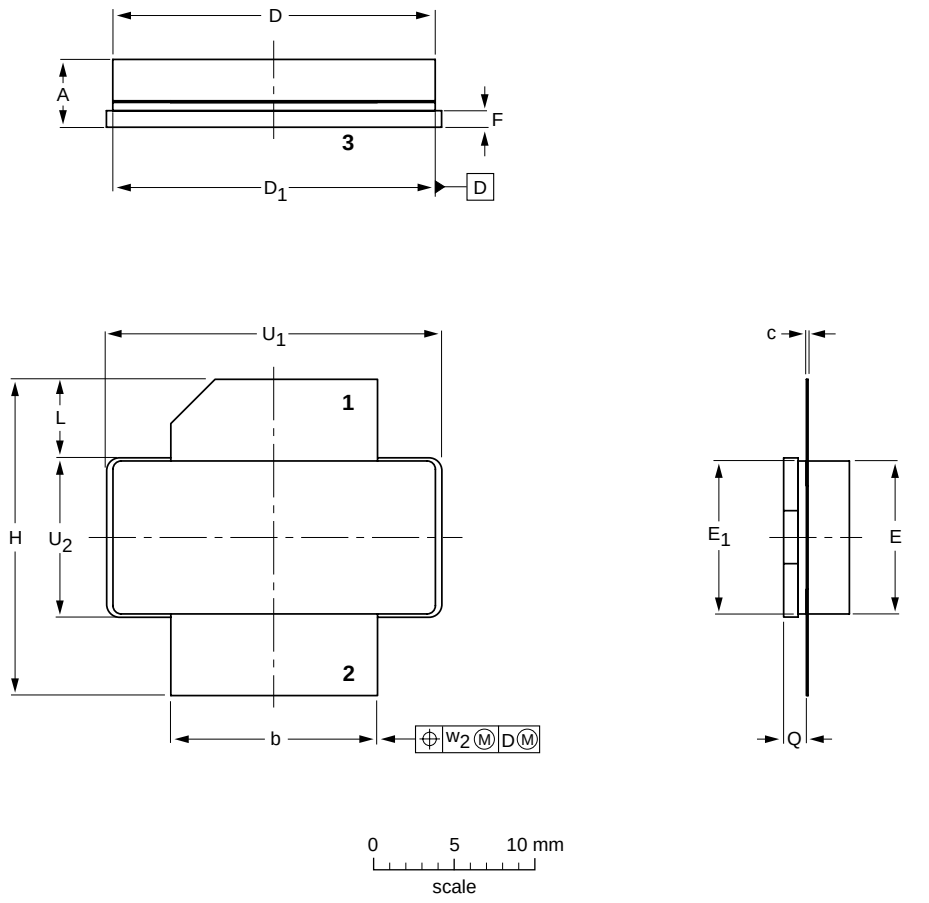


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~99-12-28~~ 03-01-10

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