DATA SHEET

NEC

HETERO JUNCTION FIELD EFFECT TRANSISTOR

NE32400, NE24200

C to Ka BAND SUPER LOW NOISE AMPLIFIER N-CHANNEL HJ-FET CHIP

DESCRIPTION

NE32400 and NE24200 are Hetero Junction FET chip that utilizes the hetero junction between Si-doped AlGaAs and undoped InGaAs to create high mobility electrons. Its excellent low noise and high associated gain make it suitable for commercial systems, industrial and space applications.

FEATURES

- Super Low Noise Figure & High Associated Gain
  NF = 0.6 dB TYP., G_a = 11.0 dB TYP. at f = 12 GHz
- Gate Length: $L_g = 0.25\ \mu m$
- Gate Width : $W_g = 200\ \mu m$

ORDERING INFORMATION

PART NUMBER	QUALITY GRADE	APPLICATIONS
NE32400	Standard (Grade D)	Commercial
NE24200	Grade C and B (B is special order)	Industrial, space

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DS}	4.0	V
Gate to Source Voltage	V_{GS}	–3.0	V
Drain Current	I_D	I_{DSS}	mA
Total Power Dissipation	P_{tot}*	200	mW
Channel Temperature	T_{ch}	175	℃
Storage Temperature	T_{stg}	–65 to +175	℃

* Chip mounted on a Alumina heatsink (size: $3 \times 3 \times 0.6^t$)

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Gate to Source Leak Current	I_{GSO}	–	0.5	10	μA	V_{GS} = –3 V
Saturated Drain Current	I_{DSS}	15	40	70	mA	V_{DS} = 2 V, V_{GS} = 0 V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	–0.2	–0.8	–2.0	V	V_{DS} = 2 V, I_D = 100 μA
Transconductance	g_m	45	60	–	mS	V_{DS} = 2 V, I_D = 10 mA
Thermal Resistance	R_{th}*	–	–	260	°C/W	channel to case
Noise Figure	NF	–	0.6	0.7	dB	V_{DS} = 2 V, I_D = 10 mA, f = 12 GHz
Associated Gain	G_a	10.0	11.0	–	dB	

RF performance is determined by packaging and testing 10 chips per wafer.
Wafer rejection criteria for standard devices is 2 rejects per 10 samples.

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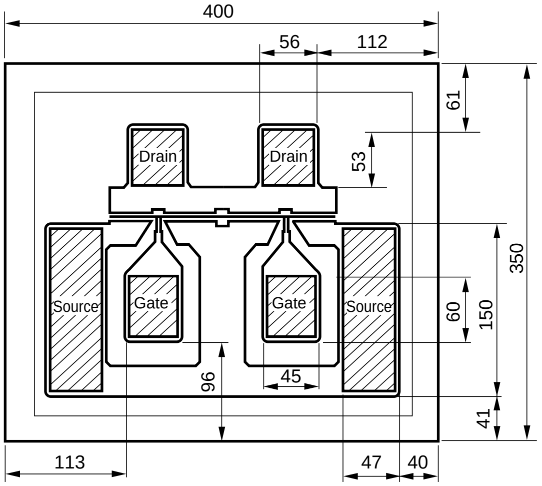
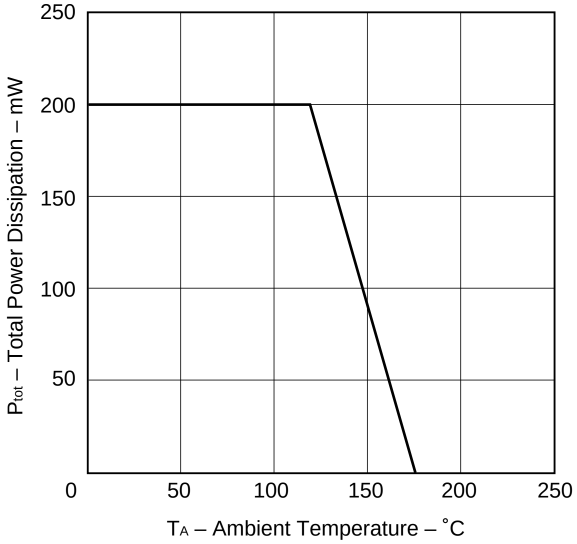
CHIP DIMENSIONS (Unit: μm)

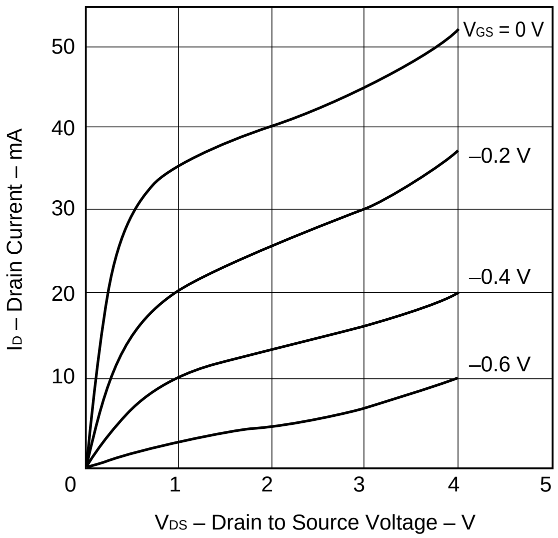


Thickness = 140 μm

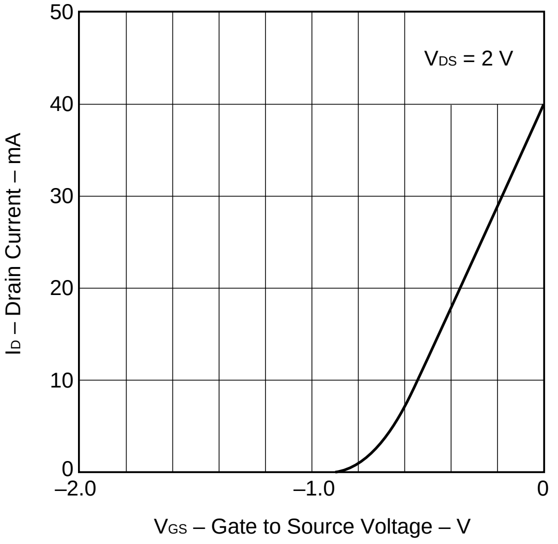
▨ : BONDING AREA

TYPICAL CHARACTERISTICS ($(T_A = 25\ ^\circ C)$)

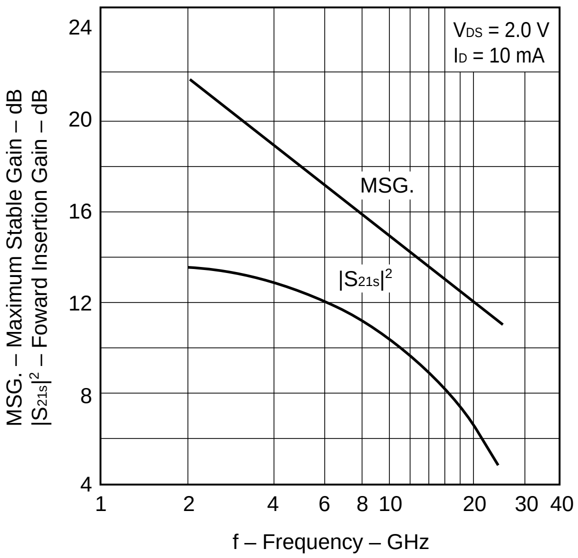

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE



MAXIMUM AVAILABLE GAIN, FORWARD
INSERTION GAIN vs. FREQUENCY

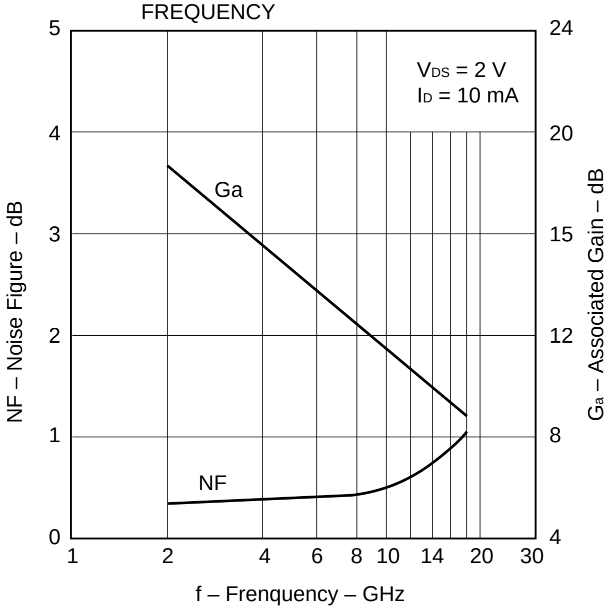


Gain Calculations

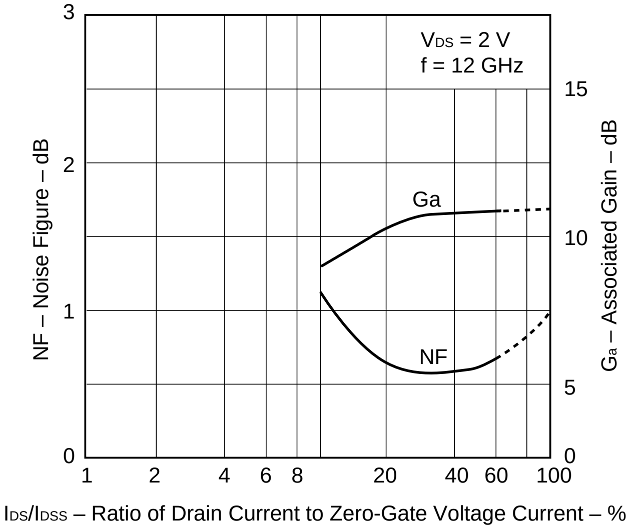
$$\mathrm{MSG.} = \frac{|S_{21}|}{|S_{12}|} \qquad K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}|\,|S_{21}|}$$

$$\mathrm{MAG.} = \frac{|S_{21}|}{|S_{12}|}\left(K \pm \sqrt{K^2 - 1}\right) \qquad \Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$

NOISE FIGURE ASSOCIATED vs.
FREQUENCY



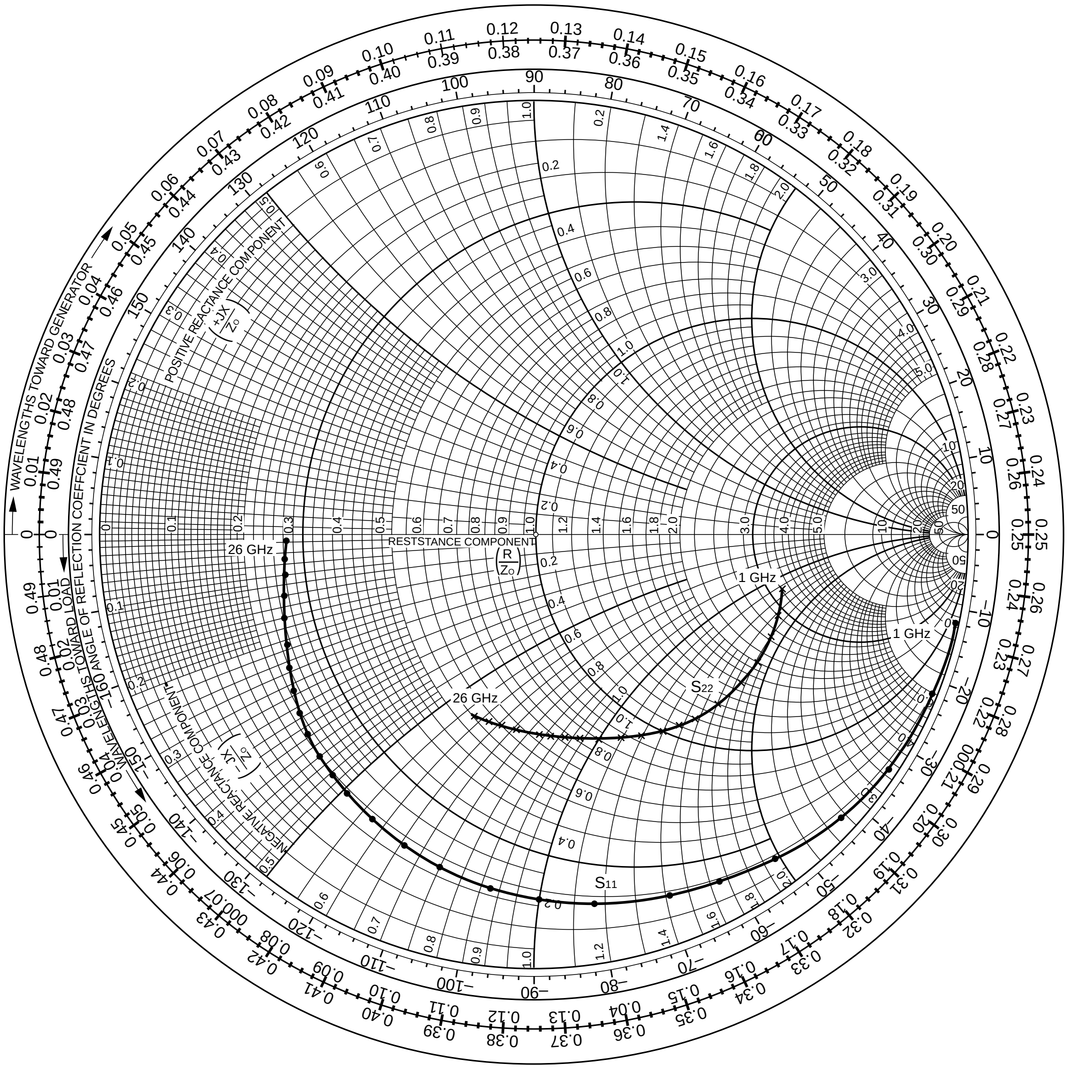
NOISE FIGURE, ASSOCIATED GAIN vs. RATIO
OF DRAIN CURRENT TO ZERO-GATE
VOLTAGE CURRENT



S-PARAMETERS

V_{DS} = 2 V, I_D = 10 mA

START 1 GHz, STOP 26 GHz, STEP 1 GHz



S-PARAMETERS MAG. AND ANG.

V_{DS} = 2 V, I_D = 10 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}		K	MSG/MAG
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.		
(MHz)		(deg.)		(deg.)		(deg.)		(deg.)		(dB)
1000	0.996	–12	4.680	171	0.015	83	0.616	–10	0.05	24.9
2000	0.994	–23	4.603	161	0.032	76	0.613	–16	0.07	21.6
3000	0.979	–34	4.486	152	0.046	70	0.601	–23	0.08	19.9
4000	0.963	–44	4.314	143	0.059	65	0.592	–30	0.10	18.6
5000	0.929	–54	4.118	135	0.071	59	0.580	–36	0.18	17.7
6000	0.904	–62	3.872	127	0.076	55	0.578	–40	0.28	17.1
7000	0.882	–70	3.759	120	0.092	51	0.574	–46	0.30	16.1
8000	0.851	–81	3.632	111	0.097	45	0.557	–52	0.35	15.7
9000	0.836	–89	3.423	104	0.098	40	0.543	–55	0.40	15.5
10000	0.809	–97	3.290	97	0.102	40	0.529	–59	0.42	15.1
11000	0.792	–105	3.179	91	0.107	37	0.523	–62	0.44	14.7
12000	0.774	–112	3.059	84	0.112	35	0.511	–67	0.45	14.4
13000	0.762	–119	2.940	78	0.118	31	0.489	–72	0.46	14.0
14000	0.745	–124	2.807	73	0.121	28	0.479	–77	0.49	13.6
15000	0.729	–128	2.698	68	0.124	26	0.468	–81	0.51	13.4
16000	0.717	–133	2.616	63	0.129	24	0.464	–85	0.54	13.1
17000	0.697	–137	2.526	58	0.134	21	0.462	–90	0.58	12.8
18000	0.685	–141	2.421	54	0.137	19	0.460	–94	0.63	12.5
19000	0.665	–146	2.315	49	0.135	19	0.460	–96	0.68	12.3
20000	0.647	–150	2.220	45	0.136	18	0.460	–98	0.70	12.1
21000	0.625	–156	2.159	40	0.138	18	0.459	–100	0.71	11.9
22000	0.612	–160	2.046	34	0.138	17	0.457	–102	0.72	11.7
23000	0.596	–166	1.892	30	0.139	17	0.455	–103	0.73	11.5
24000	0.592	–170	1.866	27	0.140	16	0.455	–105	0.74	11.3
25000	0.587	–174	1.780	25	0.141	21	0.454	–107	0.74	11.2
26000	0.584	–178	1.751	21	0.141	22	0.453	–108	0.75	11.0

CHIP HANDLING

DIE ATTACHMENT

Die attach operation can be accomplished with Au-Sn (within a 300 ˚C – 10 s) performs in a forming gas environment.

Epoxy die attach is not recommend.

BONDING

Bonding wires should be minimum length, semi hard gold wire (3-8 % elongation) 20 microns in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Bonding time should be kept to minimum.

As a general rule, the bonding operation should be kept within a 280 ˚C, 2 minutes for all bonding wires.

If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

Avoid high static voltage and electric fields, because this device is Hetero Junction field effect transistor with shottky barrier gate.

CAUTION

The Great Care must be taken in dealing with the devices in this guide.
The reason is that the material of the devices is GaAs (Gallium Arsenide), which is designated as harmful substance according to the law concerned.
Keep the Japanese law concerned and so on, especially in case of removal.

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