PRELIMINARY DATA SHEET

SKY65006: 3.3 V, 2.5 GHz Linear Power Amplifier

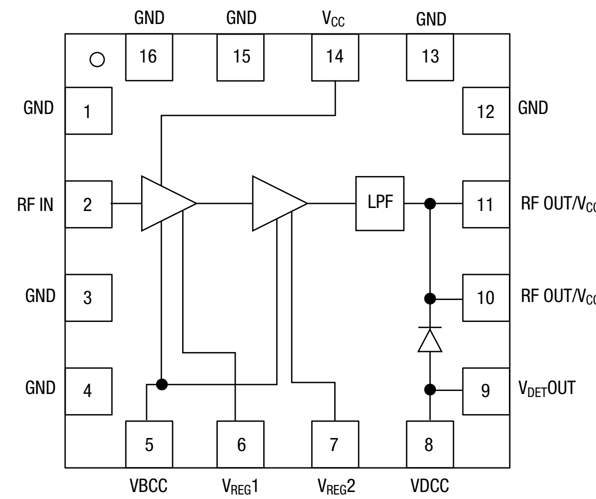
Features

- 2.4–2.5 GHz operation
- Advanced InGaP HBT process
- Integrated output power detector
- Integrated output second harmonic filter
- Low quiescent current: 50 mA
- 28 dB small signal gain
- 802.11g linear power: 18 dBm (includes integrated filter loss)
- 802.11b mask-compliant power: 21 dBm (includes integrated filter loss)
- Low-cost plastic package
- Available on tape and reel

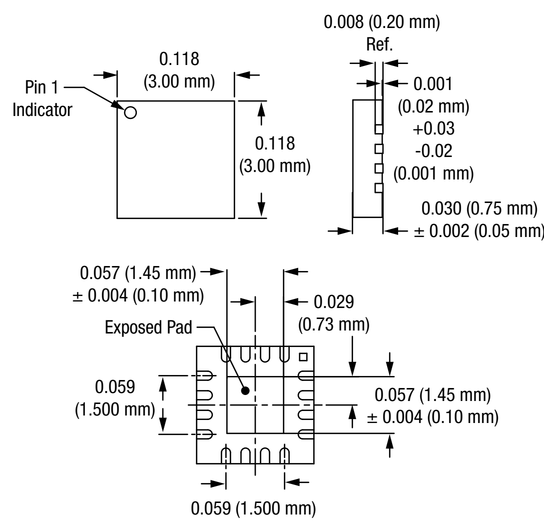
Description

The SKY65006 is a linear, high-gain, two-stage power amplifier with integrated second harmonic filter, designed for low voltage operations. This device is manufactured on our advanced InGap HBT process. It is designed for power amplifier applications in WLAN, in PC and handsets, and spread spectrum systems from 2.4–2.5 GHz. The amplifier is packaged in a QFN-16, 3 x 3 mm package.

Block Diagram



QFN-16 (3 x 3 mm)



Pin Assignments

Pin	Symbol	Description
1, 3, 4, 12, 13, 15, 16	GND	Equipotential point. Connect these pins to the printed circuit board common via the lowest possible impedance.
2	RF IN	RF input
5	VBCC	DC control voltage input that sets bias to the first amplifier stage.
6	$V_{REG}1$	DC control voltage input to regulate the current to the first amplifier stage.
7	$V_{REG}2$	DC control voltage input to regulate the current to the 2nd amplifier stage.
8	VDCC	Reference voltage input to power detector.
9	V_{DETOUT}	Power detector output voltage.
10, 11	RF OUT/V_{CC}	RF outputs and supply voltage inputs to second amplifier stage. These pins must be connected directly together for current sharing.
14	V_{CC}	DC supply voltage input to the first amplifier stage.

DC Voltage Control Table

Mode	V_{CC}	V_{REG}(1)	VBCC	VDCC
RF IN-RF OUT	3.3	3	3.3	3.3

1. V_{REG} refers to V_{REG} on the engineering test board.

Absolute Maximum Ratings

Characteristic	Value
Supply voltage (V_{CC})	5 V
Supply current (VICC)	500 mA
Regulator supply voltage ($V_{REG}1$ & $V_{REG}2$)	< V_{CC} V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +85 °C
RF input power	10 dBm

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

General RF Transmit Electrical Specifications

T_A = 25 °C, V_{CC} = 3.3 V, V_{REG} = 3 V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F		2400		2500	MHz
Gain	$|S_{21}|$	Small signal		27.5		dB
Gain variation over frequency	$|\Delta S_{21}|$	Small signal		0.2		dB
Quiescent current	I_{CQ}	(No RF signal)		50		mA
Input return loss	$|S_{11}|$	Small signal		-21.2		dB
Output return loss	$|S_{22}|$	Small signal		-6.2		dB
Output $P_{1\ dB}$	$P_{1\ dB}$	CW		23.9		dBm
2nd harmonic	F_2	CW at $P_{1\ dB}$		-58.6		dBm
3rd harmonic	F_3	CW at $P_{1\ dB}$		-43.2		dBm
Detector voltage	V_{DET}	CW at P_{OUT} = 0 dBm		0.2		V

802.11g Electrical Specifications

OFDM Modulation, 54 Mbps, T_A = 25 °C, V_{CC} = 3.3 V, V_{REG} = 3 V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Linear power at 2.442 GHz	P_{OUT}	54 Mbps at 3.5% EVM		18.1		dBm
Current consumption	I_{CC}	54 Mbps at linear power		0.129		A
Detector voltage	V_{DET}	54 Mbps at linear power		1		V

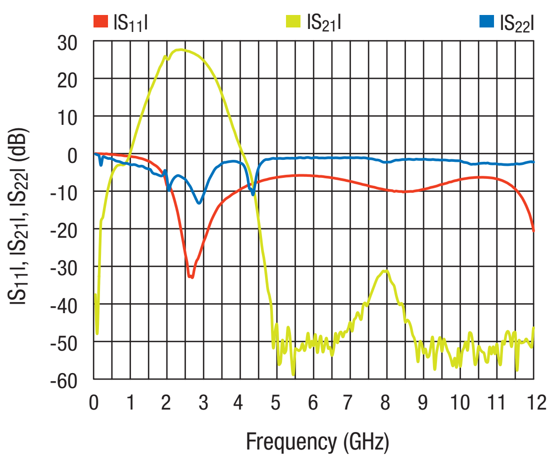
802.11b Electrical Specifications

CCK Modulation, 11 Mbps, T_A = 25 °C, V_{CC} = 3.3 V, V_{REG} = 3 V

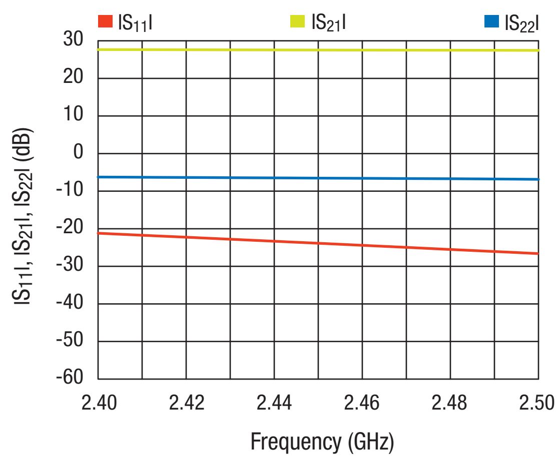
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Compliant power at 2.442 GHz	P_{OUT}	11 Mbps		21.5		dBm
Current consumption	I_{CC}	11 Mbps at compliant power		0.191		A
Detector voltage	V_{DET}	11 Mbps at compliant power		1.4		V

802.11b data is taken with a raised cosine filter and an alpha factor of 0.7.

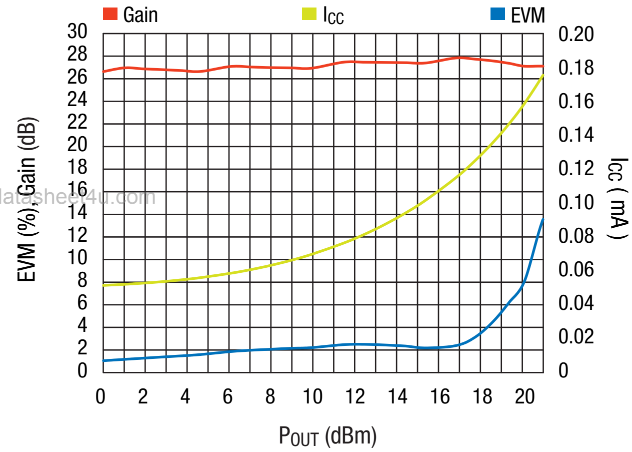
Typical Performance Data



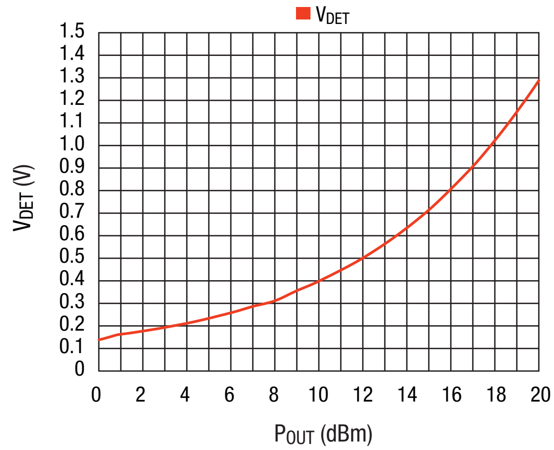
Small Signal Response
Conditions: V_{CC} = 3.3 V, V_{REG} = 3 V, T_A = 25 °C



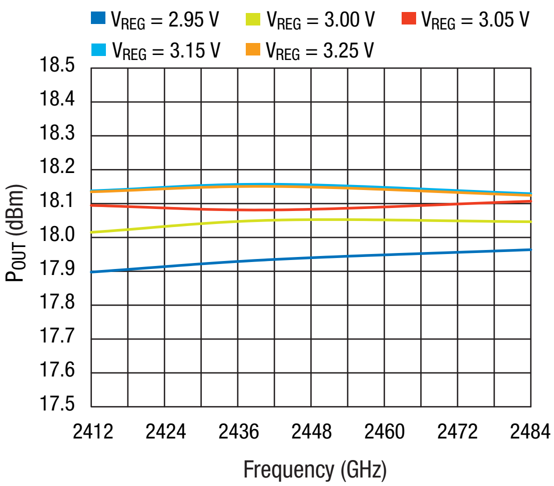
Small Signal Response
Conditions: V_{CC} = 3.3 V, V_{REG} = 3 V, T_A = 25 °C



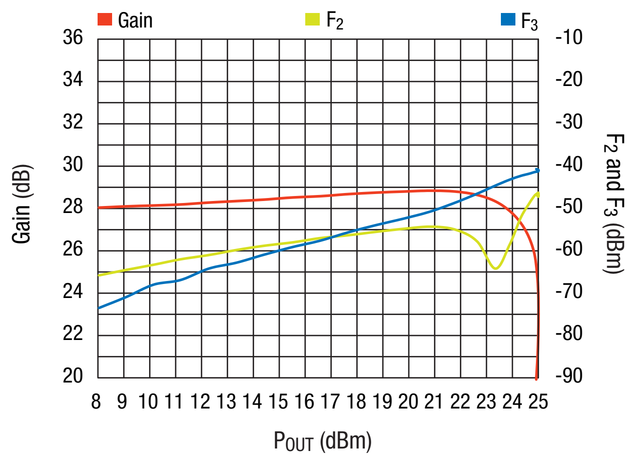
802.11g EVM and I_{CC} vs. P_{OUT}
OFDM Modulation, 54 Mbps, V_{CC} = 3.3 V, V_{REG} = 3 V, F_C = 2.442 GHz, T_A = 25 °C



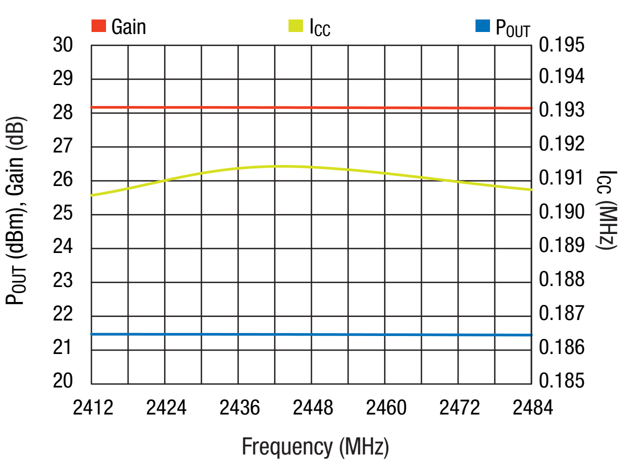
V_{DET} vs. P_{OUT}
OFDM Modulation, 54 Mbps, V_{CC} = 3.3 V, V_{REG} = 3 V, F_C = 2.442 GHz, T_A = 25 °C



V_{REG} vs. P_{OUT}
OFDM Modulation, 54 Mbps, V_{CC} = 3.3 V, T_A = 25 °C

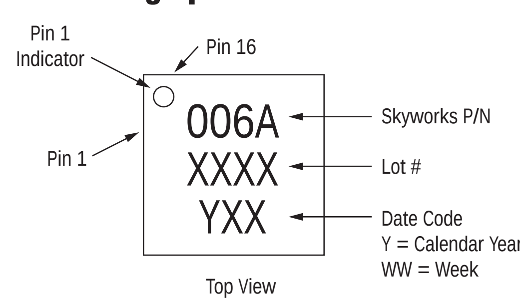


CW, 2F and 3F Harmonics vs. P_{OUT}
V_{CC} = 3.3 V, V_{REG} = 3 V, F_C = 2.442 GHz, T_A = 25 °C

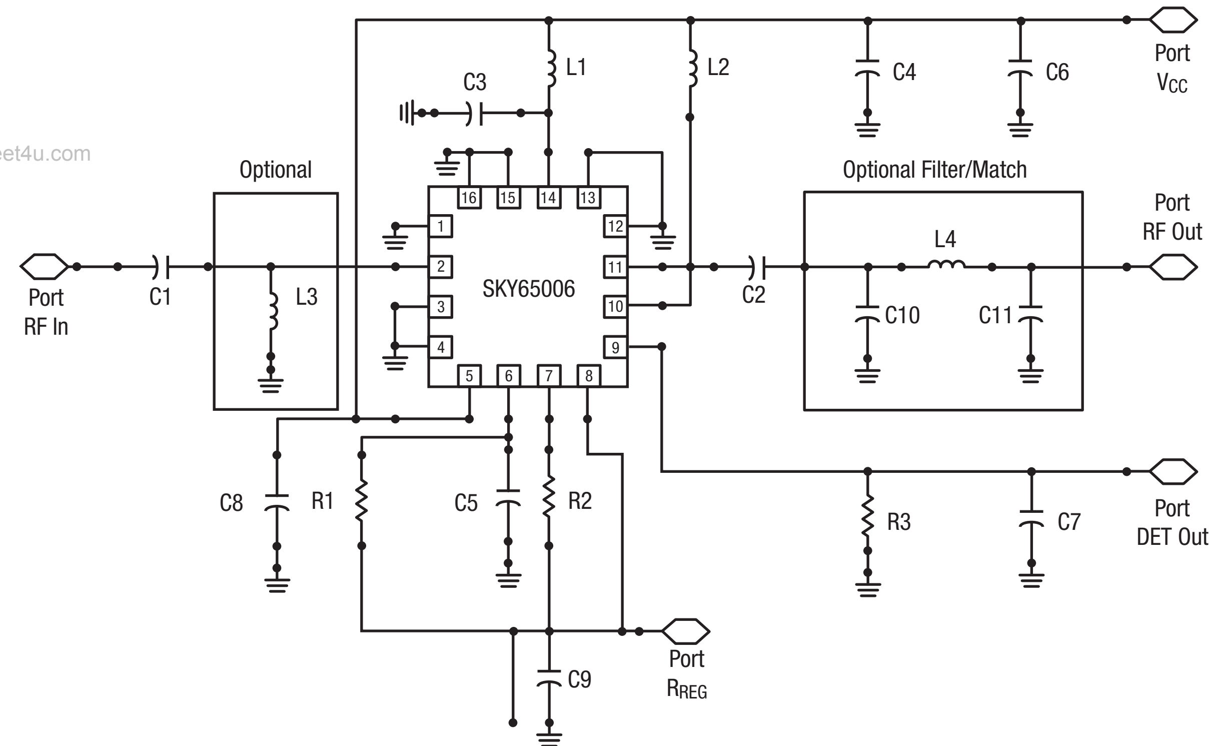


802.11b P_{OUT}, Gain, and I_{CC} vs. Frequency
CCK Modulation, 11 Mbps, V_{CC} = 3.3 V, T_A = 25 °C

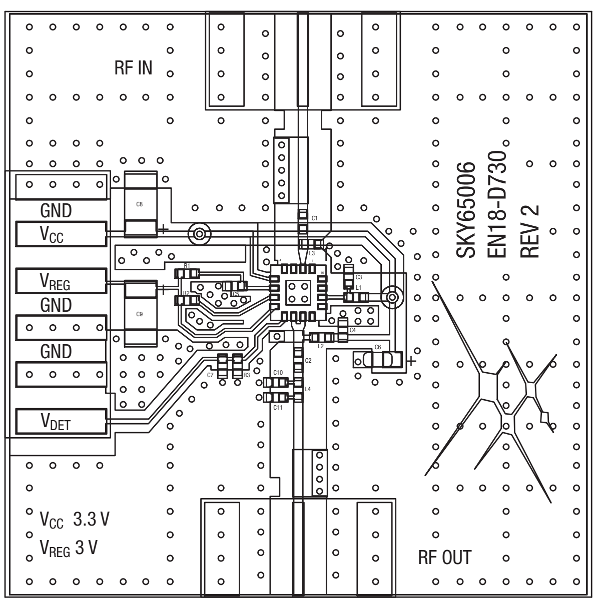
Device Branding Specifications



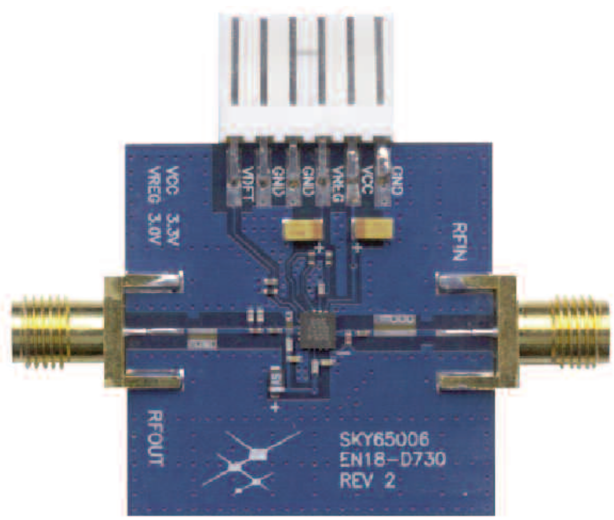
Applications Circuit



Applications Board



Board Layout



Board Photograph

Bill of Material for Applications Board

Part #	ID	Size	Value	Units	Manufacturer	Product Number
1	C_1	0402	6	pF	Murata	GRM1555C1H6R0CZ01E
2	C_2	0402	6	pF	Murata	GRM1555C1H6R0CZ01E
3	C_3	0402	10K	pF	Murata	GRM155R71H102KA01
4	C_4	0402	10K	pF	Murata	GRM155R71H102KA01
5	C_5	0402	1.8	pF	Murata	GRM1555C1H1R8CZ01D
6	C_6	0603	4.7	µF	Murata	GRM188R60J475KE19D
7	C_7	0402	5	pF	Murata	GRM1555C1H5R0CZ01E
8	C_8	0402	10	µF	Murata	GRM1555C1H100JZ01E
9	C_9	0402	10	µF	Murata	GRM1555C1H100JZ01E
10	C_{10}	0402	1	pF	Murata	GRM1555C1H1R0CZ01E
11	C_{11}	0402	1	pF	Murata	GRM1555C1H1R0CZ01E
12	L_1	0402	22	nH	TDK	MLK1005S22NJT000
13	L_2	0402	22	nH	TDK	MLK1005S22NJT000
14	L_3	0402	2.2	nH	TDK	GRM1555C1H2R2CZ01E
15	L4	0402	2.2	nH	TDK	GRM1555C1H2R2CZ01E
16	R_1	0402	180	Ω	Panasonic[1]	ERJ2GEJ181X
17	R_2	0402	240	Ω	Panasonic[1]	ERJ2GEJ241X
18	R_3	0402	51K	Ω	Panasonic[1]	ERJ2GEJ513X
19	PCB				Metro circuits	EN18-D730

1. Panasonic is Skyworks preferred vendor, however any suitable equivalent will do.

Test Board Biasing Procedure

1. Connect the RF input and output ports as labeled on the engineering evaluation board.
2. Set the input power level from the signal generator to approximately -25 dBm.
3. Apply ground connection from DC voltage supply to all GND pins before applying any voltage.
4. Adjust the power supply to 3.3 V and set the current limit to 400 mA. Apply voltage to the pin labeled V_{CC} and note that there is no current draw from the supply. Be sure to apply the voltage to V_{CC} before applying any other voltages to the test board.
5. Adjust a second power supply output to 3.0 V and set the current limit to 30 mA. Apply voltage to the pin labeled V_{REG} and note that the current draw is approximately 10 mA.
6. Observe that the current on the V_{CC} supply is in the range of the quiescent current specification. The SKY65006 should be approximately 50 mA.
7. Observe that the small signal gain is within the range specified. The SKY65006 should be in the range of 27 dB. This should verify the proper working conditions for this device, and further testing can proceed.
8. To observe the detector voltage output, connect a voltmeter or oscilloscope to the V_{DET} pin on the evaluation test board. Set the signal source to CW mode and increase power until the output voltage begins to increase. The nominal offset voltage with low or no signal inputs should be approximately 50–200 mV and should increase monotonically to approximately 700–1000 mV, when driven at an output level of approximately 18 dBm. The evaluation circuit contains an external 51K Ω resistor and an equivalent capacitance of 10 pF to ground.
9. Bias the unit off by first removing the V_{REG} power supply and finally remove the connection to the V_{CC} power supply.

Application Information

The Skyworks SKY65006 is a high-performance 2-stage InGaP power amplifier designed for 2.4–2.5 GHz ISM, IEEE802.11b and 802.11g WLAN band applications. The SKY65006 is a high-efficiency linear amplifier designed for single 3.3 V supply operation, requiring no input and output matching components for 50 Ω operation. This device also includes an internal power detector and integrated harmonic filter for reduced PC board component count. The integrated low pass filter is also highly effective in reducing harmonics at their source by localizing harmonic rejection to a tiny portion of the PA chip. This significantly reduces the risk of radiation from a high order filter design external to the amplifier. Filtering of harmonics in this way may eliminate the need for an external shield over the PA, and reduces overall cost. If additional suppression of harmonics is required, an external low pass function can be added to the output of the amplifier. Refer to data sheet for filter values and response plots.

The SKY65006 requires a nominal V_{CC} supply voltage of 3.3 V and a positive control voltage V_{REG}1, 2 providing bias for the first and second stage amplifiers. Nominal control voltage, V_{REG}, is 2.5–2.6 V resulting from the stack of two emitter-base junctions of about 1.3 V each for typical GaAs HBT device. To insure proper reference currents into V_{REG}1, 2, for normal operation of the RF stages, drop-in resistors could be used between V_{REG}1, 2 and a V_{REG} supply. Bias control would then be set in the range of 2.7–3.5 V allowing added flexibility for both the control voltage value and desired RF stage currents. If additional output power is required, V_{CC} can also be increased 4.0 V. Biasing of each stage consists of an external resistor of 180 Ω (R_1) and 240 Ω (R_2) for the recommended typical bias currents of 15 mA and 35 mA for stage 1 and 2 respectively. In most applications one end of each of the bias resistors is tied to the V_{REG} supply, so both amplifier stages are biased with a single common voltage. Capacitor C_4, 1.8 pF, bypasses the V_{REG} stage 1 control bias pin and is used to improve RF rejection of the bias control lines.

Although there is no need for external matching when operating in a 50 Ω system, an input and output 6 pF decoupling capacitor is shown on the evaluation circuit. This capacitor is only mandatory on the RF output side of the device. The RF input is DC isolated and could be connected to driver circuits directly without the need for additional blocking capacitors. Capacitors of 6 pF were chosen because their self-resonant frequency would not add any unwanted disturbances in the 50 Ω transmission line path. The SKY65006 is unconditionally stable at any frequency and voltage setting as long as it is grounded correctly. It is extremely important to pay special attention to all RF grounding pads especially those directly under the device. Ground pad vias and solder mask patterns are designed in such a way to ensure minimum parasitic inductance to the underlying ground and at each RF bypassing component. To ensure reliable soldering of the device paddle, it is highly recommended that filled vias with a minimal reliable diameter and filling the entire pattern be used. The filled-via technique would remove the possibility of solder migration down via holes, which can cause a large increase in inductance and possible instabilities.

Each amplifier stage is biased through a series choke and shunt capacitor combination which is completely integrated on chip to provide maximum RF isolation and harmonic radiation immunity. To avoid interferences from the low-frequency gain of the amplifier and to insure stability at low out of band frequencies, stage 1 amplifier is biased through inductor L_1. It is also then shunted by a large value capacitance to ensure proper low-frequency bypassing of the amplifier. To avoid a shunting effect on the 50 Ω line, a high-impedance, self-resonating choke L_2 (in the range of 22–33 nH depending on vendor and size) and a large value bypass capacitor are used for biasing the output stage. Capacitor C_7, 4.7 µF, on the V_{CC} line should be placed as close as possible to the biasing network supplying stage 2 or the output stage of the amplifier. Applications with the DC bias being generated strictly from a battery as the voltage source may not require this capacitor, or as large a value as specified in the applications circuit. However, in that case, a smaller ceramic capacitor of at least 0.1 µF should be used and also placed as close as possible to the biasing network supplying stage 2.

Note: Normal operation requires that V_{CC} including VBCC be applied before the application of the V_{REG} voltages biasing stage 1 and 2 bias currents. If V_{CC} and VBCC are not applied prior to the application of the V_{REG} biasing, voltage damage could occur from excessive base current draw through the collector junction of the bias transistor.

The SKY65006 also includes an on-board, compensated power detector providing a single-ended output voltage for measuring power over a wide dynamic range. The detector load and settling time constant are set external to the device. Nominal detector load is 51K Ω and 5 pF, yielding a settling time of approximately 500 ns. Note that there is an internal 5 pF on-chip capacitance, so the net capacitance value is approximately 10 pF. Lower resistor values may be used if necessary with the net impact being a lower output detector voltage over its useful dynamic range. For proper detector operation, a reference voltage must be applied to the V_{DET} line. Any voltage between 2 and 4 V is acceptable for the reference voltage, but it is recommended to supply V_{DET} from the V_{REG} power supply. The benefit in doing this is that the approximate 2 mA of current that the reference circuit consumes will not be wasted with the PA in the "Off" state. There is also the option of not biasing the detector reference at all if the current consumption is of prime importance. The detector will then act as a normal unbiased detector, and sensitivity and accuracy will be degraded.

The application's circuit board was constructed as a four-layer FR4 stack with an overall thickness of 0.062 inches. Top layer dielectric is 0.01-inch thick with 50 Ω transmission line widths of 0.0195 inches. Printed circuit board was constructed using a symmetrical 0.01-inch stack on the top and bottom layers and with a 0.032-inch thick pre-preg core. All components were 0402 in size with the exception of the 4.7 μF and 10 μF Tantalum capacitors. Please note that the 10 μF capacitors were installed to provide low frequency filtering for lab testing. Actual values, if necessary, will be dependent upon layout and circuit environment. All ground vias used were 0.012 inches in diameter and placed as close to the ground ends of by-passing components as possible. Four vias were used under the device to create a low inductance path to ground. If a smaller diameter is to be used, or if the substrate thickness is greater than 0.01 inches, additional vias must be placed under the device to reduce the potential risk of parasitic oscillation.

Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

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