CLA70000 Series
High Density CMOS Gate Arrays

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Recent advances in CMOS processing technology and improvements in design architecture have led to the development of a new generation of array-based ASIC products with vastly improved gate integration densities. This family of CLA70000 1 micron CMOS arrays brings considerable advantages to the design of next generation systems combining high performance and high complexity.

Features

- Low power channelless arrays from 5,000 to 250,000 available gates (5µW / gate / MHz)
- 1 micron (0.8 micron effective) twin well epitaxial process
- Typical gate delays of 400 ps (NAND2 , Fanout=2)
- Comprehensive cell library including DSP, JTAG/BIST and compiled memory cells (ROM blocks to 64K bits and RAM blocks to 16K bits)
- Extensive Range of Plastic and Ceramic Packages for both Surface Mount and Through Board Assembly
- Flexible I/O structure allows user to define power pad locations
- Fully supported on industry standard workstations and in-house software
- High drive output stages with slew rate control
- Supports JTAG and BIST test philosophies (IEEE 1149-1 Test Procedures)
- MIL 883C compliant product available (paragraph 1.2.1)

Overview

The CLA70000 gate array family is Zarlink Semiconductors' sixth generation CMOS gate array product. The family consists of nine arrays implemented on the latest generation (1 micron) twin well epitaxial CMOS process. The process in conjunction with the advanced layout and route software, offers extremely high packing densities.

The array architecture is based upon the earlier well proven CLA60000 series with the emphasis being placed on high speed, high packing density, and provision of comprehensive cell libraries. The cell libraries encompass new DSP and other specialized macros.

Full design support is available for major industry standard ASIC design software tools, as well as Zarlink Semiconductor's proprietary PDS2 design environment. Design support is provided by Zarlink Semiconductor's design centers, each offering a variety of design routes, which may be customized to individual customer requirements.

Product Details

The CLA70000 array series is shown below with typical figures given for usable gates. Actual gate utilization is dependent on circuit structure, giving a range of 40 -70% for two layer metallisation.

DEVICE NUMBER	I/O AND POWER PADS	GATE COMPLEXITY	ESTIMATED USABLE GATES
CLA70000	44	5K	2.5K
CLA71000	68	12K	6K
CLA72000	84	19K	9.5K
CLA73000	100	27K	13.5K
CLA74000	120	39K	17.5K
CLA75000	160	70K	31.5K
CLA76000	200	110K	49.5K
CLA77000	256	182K	82K
CLA78000	304	256K	115K

Core Cell Arrangement

- Supports compact macros
- Allows high density routing

A four transistor group (2 NMOS and 2 PMOS) (fig.1) forms the basic cell of the core array. This array element is repeated in a regular fashion over the complete core area to give an homogenous 'Full Field' (sea of gates) array. This lends itself to hierarchical design, allowing pre-routed user defined subcircuits to be repeated anywhere on the array. The core cell structure together with all associated cell libraries have been carefully designed to maximize the number of nets which may be routed through the cell. This enables optimal routing of both data flow and control signal distribution schemes thus giving very high overall utilization factors. This feature is of particular benefit in designs using highly structured blocks such as memory or arithmetic functions.

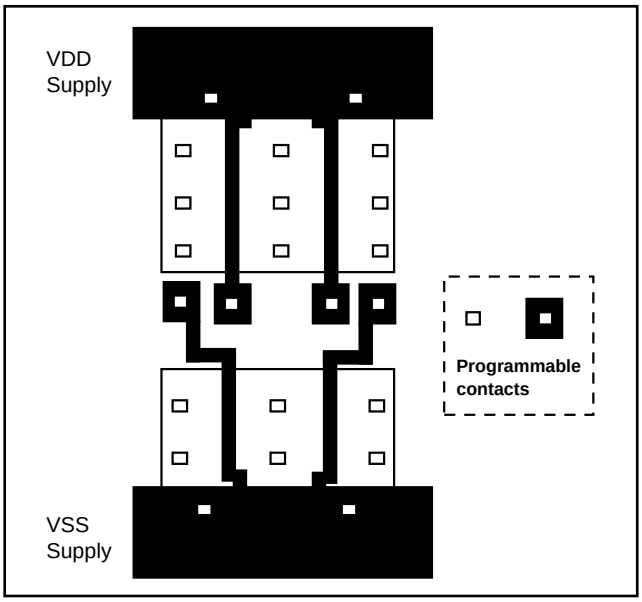

Figure 1 - Diagrammatic representation of Array Core Cell

I/O Buffer Arrangement

- Several hundred different I/O cell combinations
- Programmable Slew rate Control on all Outputs
- Excellent Latchup and ESD immunity

The I/O buffers are the interface to external circuitry and are therefore required to be robust and flexible. Both inputs and outputs incorporate electrostatic discharge (ESD) protection structures which can withstand in excess of 2KV, and are highly resistant to latch-up due to the epitaxial process. In addition the construction concepts used for the I/O cells provide the designer with several hundred different options of I/O cell configuration.

The CLA70000 I/O buffers (fig.2) contain all the components for static protection, CMOS and TTL compatible input stages, and a wide variety of intermediate and output drive configurations. Included are Schmitt triggers, tristate controls, and slew rate controlled output buffers. All I/O buffer locations can be configured as supply pads (VDD and VSS).

Slew rate control of output drivers is a useful feature when multiple high drive outputs need to be switched simultaneously, as may occur on driving capacitive loads such as buses. Using regular output buffers with their inherently fast edge speed can lead to significant power supply noise transients, with possible mis-operation as a result. To overcome this problem. The CLA70000 family includes a set of slew rate controlled output drivers, which use proprietary design techniques to control the turn-on of the output transistors (di/dt). These cells provide a significant benefit in the trade off between switching current magnitude and the number of supply pads required.

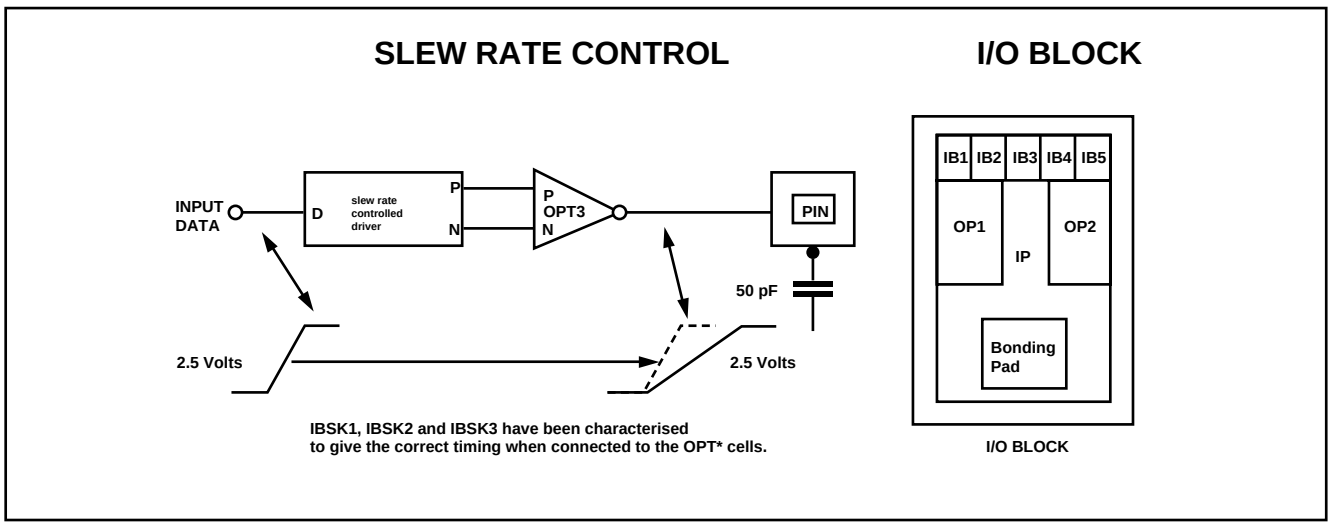

Fig 2. Slew Control & I/O Block

Power Supply Distribution

- Three power rings for good noise immunity
- Optimized for efficient routing
- User defined placement of Power and Ground pads

The power supply distribution scheme for the CLA70000 arrays (fig.3) has the flexibility to meet varying applications needs. Three separate power rings are used, one each for the internal core logic, intermediate buffer cells, and large output driver cells. Noise generated in the low impedance output drivers is isolated from the core logic and buffer areas. The distribution of the supply rails can be automatically positioned by the layout software which allows greater design flexibility and optimisation.

The power supply rings may be connected either to separate pad locations or combined at a single location. All I/O cell pads may be configured as either power or ground, giving complete flexibility to the designer.

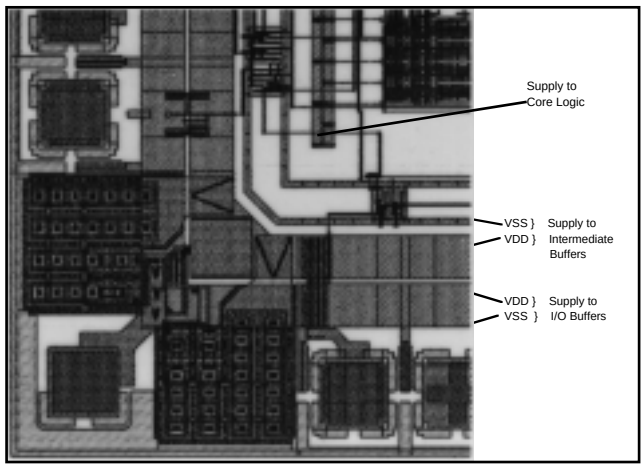

Figure 3 - Power Supply Organisation

Process Technology

- Advanced 1 micron twin well process with epitaxial substrate
- Class 10 six inch wafer fabrication facility
- High density low power process

The CLA70000 arrays are built using the Zarlink Semiconductor 1 micron drawn CMOS process, which is the third generation of our 'V' series process family. Manufacture is at Class10, 6-inch fabrication facility. The process is a twin well, self aligned oxide-isolated technology on an epitaxial substrate, with an effective channel length of 0.8 micron, giving low defect density, high reliability, and inherently low power dissipation. The process has excellent immunity to latchup, and ESD, and exhibits stable performance characteristics ideal for all commercial, industrial and military applications.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	Vdd + 0.5	V
Output Voltage	-0.5	Vdd + 0.5	V
ESD protection	2.0		K Volts
Current per pad		100	mA
Storage Temperature			
Ceramic	-65	150	°C
Plastic	-40	125	°C

Operation outside these absolute maximum ratings may permanently damage device characteristics and may affect

Recommended Maximum Operating Limits

Parameter	Min	Max	Units
Supply Voltage	3.0	5.5	V
Input Voltage	Vss	Vdd	V
Output Voltage	Vss	Vdd	V
Operating Temperature			
Commercial Grade	0	70	°C
Industrial Grade	-40	85*	°C
Military Grade	-55	125**	°C

** 125°C maximum junction temperature for plastic devices.*
***Subject to a maximum junction temperature of 150°C for ceramic devices.*

CLA70000 Series

Manufacturing Facilty

- Computer aided manufacturing
- Digital testers with large pinout capacity
- Vibration free for reliable manufacture

The CLA70000 product is manufactured near Plymouth, England in the latest purpose built facility for sub-micron process geometries. The factory uses the latest automated equipment for 6 inch wafers and Computer Aided Manufacturing techniques to ensure production efficiency. Wafer fabrication is carried out in Class 10, or better, clean room conditions in a vibration free environment to assure the lowest possible defect level. In addition to the world class wafer facility there are excellent probe and final test areas equipped with the latest analog and digital testers capable of handling complex test vectors and large pinouts. This large investment shows Zarlink Semiconductors' commitment to all the market areas needing state-of-the-art CMOS ASICS.

Cell Library

- Comprehensive range of cells
- Specialized DSP and BIST sub-libraries
- Compatible with Megacell and CLA60000

A very comprehensive cell library is available for the CLA70000 series. It contains sub libraries which may be used in specific applications areas such as Digital Signal Processing (DSP) and Built In Self Test (BIST).
More details on these specialized libraries can be found in applications notes or the design manual.

The 1.4 micron (drawn) CMOS array (CLA60000) cell library may be converted to the equivalent cells on the CLA70000 to allow system upgrades. Equivalent cells are also available for the corresponding MVA70000 Megacell to enable an easy transition to a standard cell product to minimize silicon area or to add analog functions.

Cell Library

Logic Array Cells

BUF	Buffer driver
ST1	Schmitt trigger
DELAY	Delay cell
2INV	Dual driver
INV2	Inverter, dual drive
INV4	Inverter, quad drive
INV8	Inverter, octal drive
NAND2	2 input NAND gate
ND3	3 input NAND gate
NAND3	3 input NAND gate + inverter
2NAND3	Dual 3 input NAND gate
NAND4	4 input NAND gate
NAND5	5 input NAND gate
NAND6	6 input NAND gate
NAND8	8 input NAND gate
NOR2	2 input NOR gate
NR3	3 input NOR gate
NOR3	3 input NOR gate + inverter
2NOR3	Dual 3 input NOR gate
NOR4	4 input NOR gate
NOR5	5 input NOR gate
NOR6	6 input NOR gate
NOR8	8 input NOR gate
A2O21	2 input AND to 2 input NOR gate + inverter
O2A21	2 input OR to 2 input NAND gate + inverter
2A2O21	Dual 2 input AND to 2 input NOR gate
2O2A21	Dual 2 input OR to 2 input NAND gate
2ANOR	2 input ANDs to 2 input NOR gate
2ONAND	2 input ORs to 2 input NAND gate
A2O31	2 input AND to 3 input NOR gate
O2A31	2 input OR to 3 NAND gate
A3O21	3 input AND to 2 input NOR gate
O3A21	3 input OR to 2 input NAND gate
A4O21	4-input ANDs to 2 input NOR gate
O4A21	4-input ORs to 2 input NAND gate
A2041	2-input AND to 4 input NOR gate
O2A41	2-input ORs to 4 input NAND gate
3A2O31	3 2-input ANDs to 3 input NOR gate
3O2A31	3 2-input ORs to 3 input NAND gate
O2A2O21	2 input OR to 2 input AND to 2 input NOR gate
A2O2A21	2 input AND to 2 input OR to 2 input NAND gate
EXOR	Exclusive OR gate + NAND gate + inverter
EXNOR	Exclusive NOR gate + NOR gate + inverter
EXOR2	2 input exclusive OR gate
EXNOR2	2 input exclusive NOR gate
EX2	Exclusive OR gate + inverter
EXN2	Exclusive NOR gate + inverter
EXOR3	3 input exclusive OR gate
EXNOR3	3 input exclusive NOR gate
EXPRIM	2 input exclusive OR gate primitive
HADD	Half adder + inverter
SUM	Sum block
SUM2	Sum block
CARRY	Carry block + NOR gate
CARRY2	Carry block + inverter
FADD	Full adder + NOR gate
BMF1	Full adder 1
BMF2	Full adder 2
MUX2TO1	2 to 1 multiplexer
MUX4TO1	4 to 1 multiplexer
MUX8TO1	8 to 1 multiplexer
MUXI2TO1	2 to 1 inverting multiplexer

MUXI4TO1	4 to 1 inverting multiplexer
MUXI8TO 1	8 to 1 inverting multiplexer
CLKA	Basic clock driver
2CLKA	Dual basic clock driver
CLKAP	Basic clock driver + inverter
CLKAM	Basic clock driver + inverter
CLKB	Large clock driver + inverter
CLKBP	Large clock driver + inverter
CLKE1	Clock driver with enable
CLKE2	Clock driver with enable
CLKE3	Clock driver with enable
TM	Buffered transmission gate
2TM	Transmission gate for 2 to 1 multiplexing
BDR	Internal bus driver
DL	Data latch
DL2	Data latch
DLRS	Data latch with set and reset
DLARS	Data latch with set and reset
DF	Master-slave D type flip flop
DFRS	Master-slave D type flip flop with set & reset
MDF	Multiplexed master-slave D type flip flop
MDFRS	Multiplexed master-slave D type flip flop with set & reset
M3DF	Multiplexed m/s D type flip flop
M3DF	Multiplexed m/s D type flip flop with set & reset
JK	J-K flip-flop
JKRS	J-K flip-flop with set & reset
JBARK	JBAR-K flip-flop
JBARKRS	JBAR-K flip-flop with set & reset
BDL	Buffered data latch
BDLRS	Buffered data latch with set & reset
JBARKRS	Buffered data latch with set & reset
BDF	Buffered master-slave D type flip-flop
BDFRS	Buffered master-slave D type flip-flop with set & reset
BMDF	Buffered mux. master-slave D type flip-flop
BMDFRS	Buffered mux. m/s D type with set & reset
BJBARK	Buffered J-K flip-flop
BJBARKRS	Buffered J-K flip-flop with set & reset
TRID	Tristate driver
GND	Ground Cell
VDD	VDD Cell

Intermediate Buffer Cells

IBCCMOS1	CMOS input buffer + large 2 input NAND gate
IBCCMOS2	CMOS input buffer + data latch
IBTTL1	TTL input buffer + large 2 input NAND gate
IBBTL2	TTL input buffer + data latch
IBST1	Input Schmitt buffer with CMOS switching levels
IBST2	Input Schmitt buffer with 2V switching levels
IBGATE	NAND2/NOR2 gates
IBCLKB	Large clock driver
IBDF	Master-slave D type flip flop
IBDFA	Master-slave D type flip flop
IBSK1	Driver with slewed outputs
IBSK2	Driver with slewed outputs
IBSK3	Driver with slewed outputs
IBTRID	Tri-state driver
IBTRID1	Tri-state driver with slewed outputs + 2 inverters
IBTRID2	Tri-state driver with slewed outputs + 2 inverters
IBTRID3	Tri-state driver with slewed outputs + 2 inverters
IB2BD	Dual high powered inverters
DRV3	Clock driver
DRV6	Clock driver

Pad Input Cells

IPNR	Input cell with no pull up or down resistors
IPR1P	Input cell with 1KOhm pull up resistor
IPR1M	Input cell with 1KOhm pull down resistor
IPR2P	Input cell with 2KOhm pull up resistor
IPR2M	Input cell with 2KOhm pull down resistor
IPR3P	Input cell with 4KOhm pull up resistor
IPR3M	Input cell with 4KOhm pull down resistor
IPR4P	Input cell with 75KOhm pull up resistor
IPR4M	Input cell with 75kOhm pull down resistor

Oscillator Cells (crystal)

to be defined

Pad Output Cells

OP1	Smallest drive output cell
OP2	Small drive output cell
OP3	Standard drive output cell
OP6	Medium drive output cell
OP12	Large drive output cell
OP5B	Standard drive non-inverting output cell
OP11B	Large drive non-inverting output cell
OPT1	Smallest drive tri-state output cell
OPT2	Small drive tri-state output cell
OPT3	Standard drive tri-state output cell
OPT6	Medium drive tri-state output cell
OPT12	Large drive tri-state output cell
OP4B	Standard drive non-inverting tri-state output cell
OP10B	Large drive non-inverting tri-state output cell
OPOD1	Smallest drive open-drain output cell
OPOD2	Small drive open-drain output cell
OPOD3	Standard drive open-drain output cell
OPOD6	Medium drive open-drain output cell
OPOD12	Large drive open-drain output cell

OPOD5B	Standard drive non-inverting open-drain output cell
OPOD11B	Large drive non-inverting open-drain output cell
OPOS1	Smallest drive open-source output cell
OPOS2	Small drive open-source output cell
OPOS3	Standard drive open-source output cell
OPOS6	Medium drive open-source output cell
OPOS12	Large drive open-source output cell
OPOS5B	Standard drive non-inverting open-source output cell
OPOS11B	Large drive non-inverting open-source output cell

Power Supply Cells

OPVP	VDD power pad (outputs)
OPVM	GND power pad (outputs)
OPVPB	VDD power pad (outputs) : break in VDD
OPVMB	GND power pad (outputs) : break in GND
OPVPBB	VDD power pad (outputs) : break in VDD & GND
OPVMBB	GND power pad (outputs) : break in VDD & GND
IBVP	VDD power pad (buffers)
IBVM	GND power pad (buffers)
IBVPB	VDD power pad (buffers) : break in VDD
IBVMB	GND power pad (buffers) : break in GND
IBVPBB	VDD power pad (buffers) : break in VDD & GND
IBVMBB	GND power pad (buffers) : break in VDD & GND
LAVP	Power pad for logic array
LAVM	|
LAGND	|
LAVDD	|

CLA70000 PDS-BIST (JTAG/IEEE1149-1) Library

Test Register Cells

JTRDU4,8,16,24,32	4,8,16,24,32 bit Transparent Test registers with Update Latches
JTRDD4,8,16,24,32	4,8,16,24,32 bit Transparent Test registers
JTRCU4,8,16,24,32	4,8,16,24,32 bit Clocked Test registers with Update Latches
JTRCD4,8,16,24,32	4,8,16,24,32 bit Clocked Test Registers

Test Control Cells

JTAP	PDS BIST JTAG Interface Controller
JTCLK	PDS-BIST Clock Gating and Buffer Cell
JTIDREG	PDS-BIST JTAG Identification Register

Test Register Component Cells

JTDUT	Test register data bit (transparent) with update latch
JTDUF	Test register data bit (transparent)] with update latch
JTDDT	Test register data bit (transparent)
JTDDF	Test register data bit (transparent)
JTCUT	Test register data bit (clocked) with update latch
JTCUF	Test register data bit (clocked) with update latch
JTCDT	Test register data bit (clocked)
JTCDF	Test register data bit (clocked)
JTCT	Test register local controller
JTBF16	Test register driver 4-19 databits
JTBF16	Test register driver 20-34 databits

CLA70000 DSP Macrocell Library

Ripple Carry Adders

ADR1	1bit adder
ADR3	4 bit adder
ADR8	8 bit adder
ADR16	16 bit adder
ADR24	24 bit adder
ADR32	32 bit adder

High Speed Carry Select Adders

ADS1	1bit adder
ADS3	4 bit adder
ADS8	8 bit adder
ADS16	16 bit adder
ADS24	24 bit adder
ADS32	32 bit adder

Carry Select Adders (Reduced Area)

ADT8	8 bit adder
ADT16	16 bit adder
ADT24	24 bit adder

ADT32	32 bit adder

Subtractor Blocks

ADSU4	4 bit subtractor add-on
ADSU8	8 bit subtractor add-on
ADSU16	16 bit subtractor add-on
ADSU24	24 bit subtractor add-on
ADSU32	32 bit subtractor add-on

Shifters Arithmetic Right (Padded with MSB)

SHA4	4 stage arithmetic right shifter
SHA8	8 stage arithmetic right shifter
SHA16	16 stage arithmetic right shifter
SHA24	24 stage arithmetic right shifter
SHA32	31 stage arithmetic right shifter

Shifters Barrel Right (Padded with LSB Data Exiting Shifter)

SHB4	4 stage barrel right shifter
SHB8	8 stage barrel right shifter
SHB16	16 stage barrel right shifter
SHB24	24 stage barrel right shifter
SHB32	31 stage barrel right shifter

Shifters Logic Right/Left (Padded with Zero's)

SHL4	4 stage logic right shifter
SHL8	8 stage logic right shifter
SHL16	16 stage logic right shifter
SHL24	24 stage logic right shifter
SHL32	31 stage logic right shifter

Logic Units (8 Function)

FGLO4	4 logic bit unit
FGLO8	8 logic bit unit
FGLO16	16 logic bit unit
FGLO24	24 logic bit unit
FGLO32	32 logic bit unit

Arithmetic Units (8 Function)

FGAR4	4 bit logic unit
FGAR8	8 bit logic unit
FGAR16	16 bit logic unit
FGAR24	24 bit logic unit
FGAR32	32 bit logic unit

CLA70000 DSP Macrocell Library

Multiplers and Associated Cells

BMA8X8	Mixed mode multiplier (8 x 8 bits)
BMA16X16	Mixed mode multiplier (16 x 16 bits)
BMA24X24	Mixed mode multiplier (32 x 32 bits)
BMB16X12	Single pipeline multiplier (16 x 12 bits)
BMC24X24	Mixed mode multiplier (24 x 24 bits)
BTHE1	Booth encoder
BTHD1	Non-Inverting Booth decoder
BTHD2	Inverting Booth decoder

Many of the macro functions perform similar functions to the standard TTL and CMOS logic families. The user is warned, however, that the logic functions may differ slightly and is therefore recommended to refer to the design manual rather than assume an exact functional copy. The PDS simulator uses the constituent microcell models for circuit analysis.

The macrocells are constructed from basic microcells and are placed and routed to give optimum use of chip area.

MACRO	FUNCTION

Adders

ADA4	4 bit binary full adders with fast carry
ADG4	Look ahead carry generator

Counters

CNA4	BCD counter/4 bit latch decoder/driver
CNB4	4 bit counter latch
CNC4	4 bit synchronous counter
CND4	4 bit binary up/down Synchronous counter
CND4A	4 bit binary up/down counter with reset
CNE4	4 bit decade counter
CNF4	4 bit binary synchronous counter
CNG4	4 bit binary counter

Decoders

DRA3T8	3 line to 8 line decoder/demultiplexer
DRA4T16	4 line to 16 line decoder/demultiplexer
DRA4T16A	4 line to 16 line decoder/demultiplexer no enable
DRB3T8	3 line to 8 line decoder/demultiplexer with address registers
DRB3T8	3 line to 8 line decoder/demultiplexer with address latches
DRD2T4	2 line to line decoder
DRF4T10	4 line to 10 line BCD decoder
DRG4T10	4 line to 10 line excess 3 to decimal decoder
DRH4T10	4 line to 10 line excess gray to decimal decoder decoder
DRI10	BCD to decimal decoder/driver
DRJ7	BCD to 7 segment decoder/driver
DRK7	BCD to 7 segment decoder/driver
DRL7	BCD to 7 segment decoder/driver

Encoders

ENA8T3	8 line to 3 line priority encoder
ENB10T4	10 line to 4 line priority encode

Flip-Flop

FFA8	8 bit bistable latches
FFB6	6 bit D-type flip-flop with clear
FFC4	4 bit D-type flip-flop with clear & complimentary outputs
FFD8	Octal D-type flip-flop with clear

ALU/Functional Generator

FGA5	4 bit ALU/function generator

Adders

MCA4	4 bit magnitude comparators

Multiplers

MLA10	Decade rate multiplier
MLB4X4	4 by 4 binary multiplier with tristate outputs
MLW7	7 bit Wallace trees with tristate outputs

Multiplexors

MXA8T1	8 line to 1 line data selector / multiplexer
MXB4T1	Dual 4 line to 1 line data selector / multiplexers
MXB4T1A	Dual 4 line to 1 line data selector / multiplexer with inverted tristate outputs
MXC2T1	Quad 2 to 1 data selector / multiplexers
MXC2T1A	Quad 2 to 1 selector (inverted outputs)
MXD4T1	4 to 1 multiplexor with strobe
MXE4T1	4 to 1 multiplexor with strobe
MXF2T1	2 to 1 multiplexeor with storage

Parity Generator

PGA9	9 bit odd/even parity generator/checker

Shift Registers

SRA2	2 bit POS shift register with clear
SRA4	4 bit POS shift register with clear
SRA8	8 bit SIPO shift register with clear
SRA8A	8 bit SIPO shift register without clear
SRB2	2 bit PISO shift register with clear
SRB4	4 bit PISO shift register with clear
SRB8	2 bit PISO shift register with clear
SRB8A	2 bit PISO shift register without clear
SRC8	8 bit PISO shift register with clear
SRD4	8 bit SIPO shift register with clear
SRE4	4 bit PIPO shift register with JKbar input
SRF8	8 bit shift and store register with tristate outputs
SRG4	4 bit bidirectional universal shift register
SRJ4	4 bit parallel access shift register
SRK5	5 bit shift register

Process Monitor

PERF	Performance monitor

BIST *

RGBIT	Test register (one bit)
RGTBIT	Test register (one monitor bit)
RGDIAG	Diagnostic control unit
RGCTL	Test register controller
RGHOLD	Test register hold circuitry

* (early built in self test cells) see CLA7BIST Library

CLA70000 Paracell Library

Memory Cells

RBRAM	RAM	MAX 16384 bits per block WORDS 2:128, bits 1:128 (min:max)
ROROM	ROM	MAX 65536 bits per block WORDS 2:2048, bits 2:64 (min:max)

Design Support and Interfaces

- Flexible design route approach
- Design center engineer assigned to every customer circuit
- Full turnkey service capability

Design and layout support for CLA70000 arrays is available from various centers worldwide each of which is connected to our Headquarters via high speed data links. A design center engineer is assigned to each customer's circuit, to ensure good communication , and a smooth and efficient design flow. It should be noted that sign-off simulation against the 'golden' simulator is also supported at our local design centers.

Zarlink Semiconductor offers a variety of formal design routes as illustrated in the table below. Differing interface methods allow for varying levels of involvement in a manner which complements individual customer design styles, whilst maintaining our responsibility to ensure first time working devices.

As part of the design process Zarlink Semiconductor operates a thorough design audit procedure to verify compliance with customer specification and to ensure manufacturability. The procedure includes four separate review meetings, with the customer, held at key stages of the design.

Review 1: Held at the beginning of the design cycle

To check and agree on all performance, packaging, specifications and design timescales.

Review 2: Held after Logic Simulation but prior to Layout

Checks to ensure satisfactory functionality, timing performance, and adequate fault coverage.

Review 3: Held after Layout and Post Layout Simulation

Verification of satisfactory design performance after insertion of actual track loads. Final check of all device specifications before prototype manufacture.

Review 4: Held after Prototype Delivery

Confirm that devices meet all specifications and are suitable for full scale production.

Design Tools

The focus of the Zarlink Semiconductor design tool methodology is that of maintaining an open CAD system with all interfaces standardized via EDIF 2.0 . This enables us to provide full support for a variety of 3rd party ASIC design tools and facilitates rapid updating of associated libraries. It also provides an interface to the Zarlink Semiconductor (PDS2)

CAD SUPPORT

Design Routes

	THIRD PARTY SOFTWARE	PDS IN-HOUSE SOFTWARE	TURNKEY SERVICE
OPTIONS			
Design Review 1			
Schematic Capture	CUSTOMER	CUSTOMER	GPS
Logical Design	CUSTOMER	CUSTOMER	GPS
Design Review 2			
Physical Design	GPS	CUSTOMER or GPS	GPS
Design Review 3			
Prototype Manufacturing	GPS	GPS	GPS
Prototype Evaluation	CUSTOMER	CUSTOMER	CUSTOMER
Design Review 4			
Production	GPS	GPS	GPS

design system, which offers a total design environment including behavioral and functional level modelling.

Third Party Software Support

- Design Kits for major industry standard ASIC design software tools
- All libraries include fully detailed timing information
- EDIF 2.0 Interface
- Post layout back annotation available

Zarlink Semiconductor supports a wide range of third party design tools including IKOS, Mentor, Verilog, and Viewlogic at the time of printing. Please check with our Sales Offices for the most recent additions. The design kits offer fully detailed timing information for all cell libraries, netlist extraction utilities, and post layout back annotation capability where applicable. An example of a workstation design flow is shown in fig 5 below. Please contact your local Zarlink Semiconductor's sales office for further information about support of particular tools.

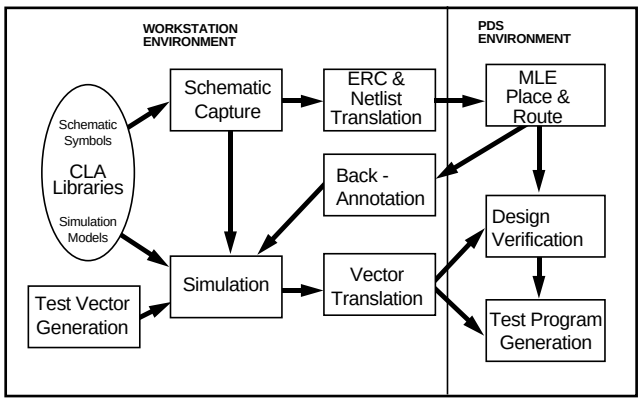

Figure 5 - Workstation Design Flow

PDS2 - The Zarlink Semiconductor ASIC Design System

- Behavioral, Functional, and Gate Level Modelling
- VHDL and Third Party Links
- Supports Hierarchical Design Techniques
- EDIF 2.0 Interface

PDS2 is Zarlink Semiconductor's own proprietary ASIC design system. It provides a fully-integrated, technology independent VLSI design environment for all Zarlink Semiconductor CMOS SemiCustom products.

PDS2 runs on Digital Equipment Computers and is self configuring according to the available machine resources. It comprises design capture (schematic capture or VHDL), testability analysis, logic simulation, fault simulation, auto place and route, and back annotation. The system offers full support for hierarchical design techniques, maintained from design capture through to layout, as well as advanced design management tools. PDS2 may be used either at a Zarlink Semiconductor Design Center or under licence at the customer's premises. A three day training course is available for first time users.

Specifications

Thermal Management

- Lower power CMOS for better thermal management
- Improved reliability
- Power packages available

The increase in speed and density available through CMOS process geometry reduction, results in a corresponding increase in power dissipation. SemiCustom designers now have the ability to design circuits of 100,000 gates and over, and chip power consumption is (or should be) a very important concern.

The logic core of 100K plus gates is the dominant factor in power dissipation at this complexity. It is essential to offer ultra low power core logic to maintain an acceptable overall chip power budget.

To minimize this problem Zarlink Semiconductor's CLA70000 arrays offer low power factors and a selection of power packages. Dissipation of 5 µW per gate per Mhz gate power and 1µW per gate load, is lower than most competitive arrays, with the reduced junction temperatures having the added advantage
of improved performance and reliability.

CLA70000 POWER DISSIPATION CALCULATION

CLA70000 series power dissipation for any array can be estimated by following the example (calculated for the CLA76XXX) below.

Number of available gates	110112
Assume percent gates used	40%
Number of used gates (110102 X 0.4)	44045
Assume 15% of gates switching during. each clock cycle (44045 X 0.15)	6607
Power dissipation/gate/Mhz (gate fanout typically 2 loads)	7µW
Total core dissipation/Mhz (6607 X 0.007)	46.2 mW
Number of available I/O pads	200
Percent of I/O pads used as Outputs	40%
Number of I/O pads used as Outputs	80
Number of output buffers switching each clock cycle (20%)	16
Dissipation/output buffers/Mhz/pF	25µW
Output loading	50 pF
Power/output buffer/Mhz	1.25mW
Total output buffer dissipation/Mhz	20mW
Total Power dissipation/Mhz	66.2mW

Estimated dissipation of the circuit at the frequencies below is

Total Power at 10 Mhz clock rate	0.66W
Total Power at 25Mhz clock rate	1.65W

AC Characteristics for Selected Cells

The CLA70000 technology library contains all the timing information for each cell in the design library. This information is accessible to the simulator, which calculates propagation delays for all signal paths in the circuit design. The simulator can automatically derate timings according to the various factors such as:

Supply voltage variation (from nominal 5V)
Junction temperature
Processing tolerance - manufacturing spreads
Gate fanout - logic loading on gate outputs
Interconnection wiring - net loading on gate outputs

For initial assessments of feasibility, path delay multipliers can be estimated by referring to the following graphs in conjunction with the appropriate delays in the tables.

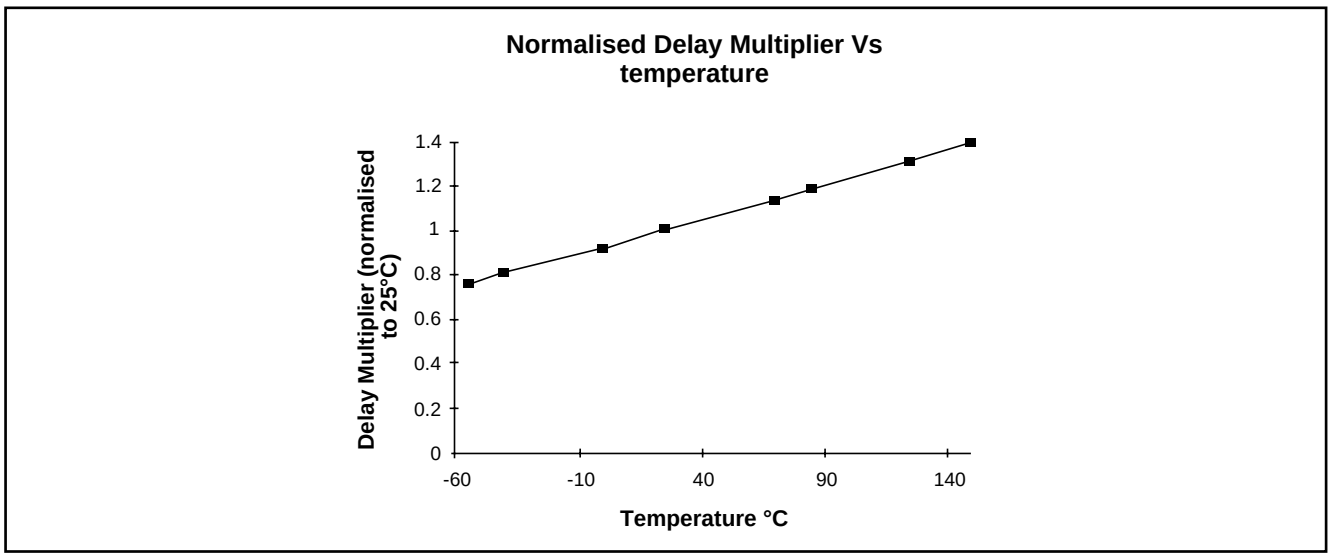

Figure 6

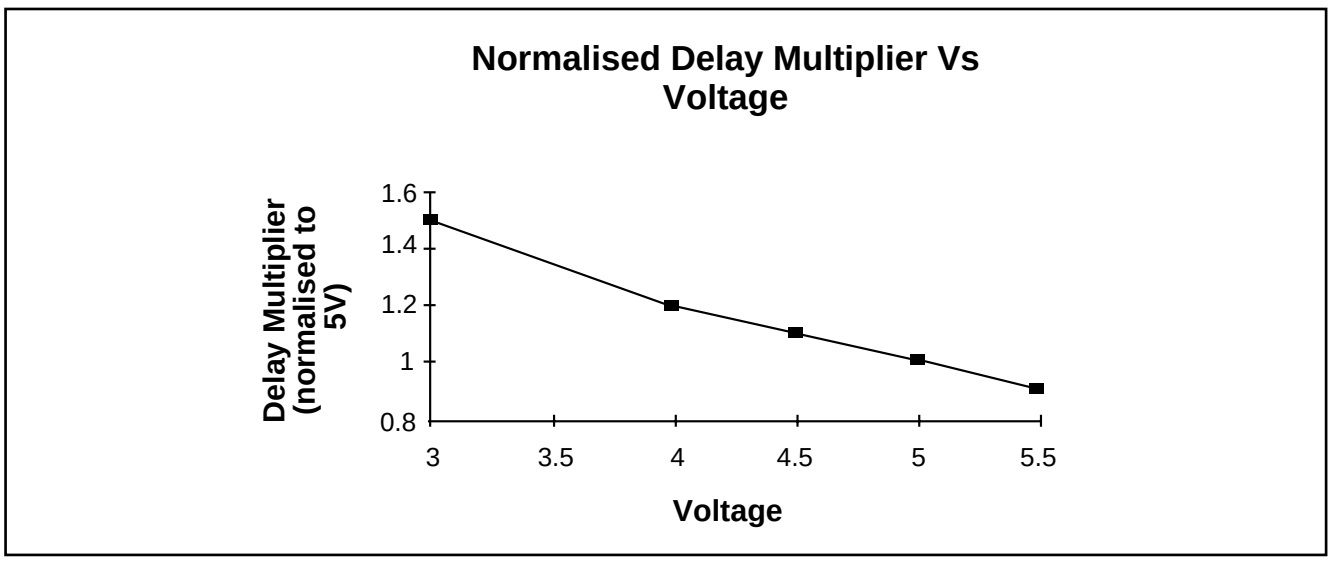

FIgure 7

AC Charcteristics

INTERNAL CORE CELLS				Typical Propagation Delay (ns)	Worst case propagation Delay (ns)			
					Commercial			
Name	Cells	Description	Symbol		Fanout			
				Fanout =2	2	4		
INV2	1	Invertor Dual Drive	tpLH	0.27	0.70	0.84		
			tpHL	0.18	0.47	0.56		
NAND2	1	2-Input NAND Gate	tpLH	0.39	1.01	1.29		
			tpHL	0.30	0.79	1.04		
NOR2	1	2-Input NOR Gate	tpLH	0.50	1.30	1.81		
			tpHL	0.22	0.57	0.80		
DF	1	Master Slave D-Type Flip-Flop	tpLH	0.54	1.40	1.60		
			tpHL	0.55	1.44	1.55		

INTERMEDIATE BUFFER CELLS				Typical Propagation Delay (ns)	Worst case propagation Delay (ns)			
					Commercial			
Name	Cells	Description	Symbol		Fanout			
				Fanout =2	2	4		
IBGATE	-	Large 2 Input NAND Gate +2 Input NOR	tpLH	0.34	0.88	1.02		
			tpHL	0.27	0.71	0.84		
IBDF	-	Master Slave D-type Flip-Flop	tpLH	0.48	1.24	1.44		
			tpHL	0.50	1.31	1.42		
IBCMOS1	-	CMOS input buffer with 2 input NAND gate	tpLH	0.60	1.58	1.68		
			tpLH	0.45	1.17	1.21		

OUTPUT BUFFER CELLS				Typical Propagation Delay (ns)	Worst case propagation Delay (ns)			
					Commercial			
Name	Cells	Description	Symbol		Fanout			
				Fanout =10pF	10pF	50pF	10pF	
OP3	-	Standard Output Buffer	tpLH	0.73	1.90	6.49		
			tpHL	0.49	1.27	4.40		
OP6	-	Medium Output Buffer	tpHL	0.50	1.30	3.59		
			tpLH	0.33	0.85	2.42		
OP12	-	Large Output Buffer	tpLH	0.38	0.99	2.14		
			tpHL	0.25	0.66	1.50		

Note : Commercial worst case is 4.5V, 70°C operating
Industrial worst case is 4.5V, 85°C operating

DC Electrical Characteristics

All characteristics at Commercial Grade voltage and temperature (note1)

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Low Level Input Voltage					V	
TTL Inputs (IBTTL1/IBTTL2)	V_{IL}			0.80		
CMOS Inputs (IBCMOS1/IBCMOS2)				1.00		
High Level Input Voltage					V	
TTL Inputs (IBTTL1/IBTTL2)	V_{IH}	2.00				
CMOS Inputs (IBCMOS1/IBCMOS2)		V_{DD} -1.00				
Input Hysterisis (IBST1) Rising	V_{T+}		3.09		V	V_{IL} to V_{IH}
Falling	V_{T-}		1.89			V_{IH} to V_{IL}
(IBST2) Rising	V_{T+}		1.72			V_{IL} to V_{IH}
Falling	V_{T-}		1.10			V_{IH} to V_{IL}
Input Current CMOS/TTL Inputs	I_{IN}					
(without resistor)		-1.00		+1.00	µA	
Inputs with 1K ohm resistor		±2.20		±11.00	mA	V_{IN}=V_{DD} OR V_{SS}
Inputs with 2K ohm resistor		±1.10	±5.00	±5.50	mA	V_{IN}=V_{DD} OR V_{SS}
Inputs with 4K ohm resistor		±0.56	±2.50	±2.75	mA	V_{IN}=V_{DD} OR V_{SS}
Inputs with 75K ohm resistor		±18.00	±1.25	±275.00	µA	V_{IN}=V_{DD} OR V_{SS}
Resistor values nominal (note2)			±66.00			V_{IN}=V_{DD} OR V_{SS}
High Level Output Voltage					v	
All Outputs	V_{OH}					
Smallest drive cell OP1/OPOS1/OPT1		V_{DD} -1.00	V_{DD} -0.05			I_{OH}=-1.00µA
Low drive cell OP2/OPOS2/OPT2		V_{DD} -1.00	V_{DD} -0.50			I_{OH}=-2.00mA
Standard drive cell OP3/OPOS3/OPT3		V_{DD} -1.00	V_{DD} -0.50			I_{OH}=-4.00mA
Medium drive cell OP6/OPOS6,OPT6		V_{DD} -1.00	V_{DD} -0.50			I_{OH}=-6.00mA
Large drive cell OP12/OPOS12/OPT12		V_{DD} -1.00	V_{DD} -0.50			I_{OH}=-12.00mA
Low Level Output Voltage			V_{DD} -0.50		v	I_{OH}=-24.00mA
All Outputs	V_{OL}					
Smallest drive cell OP1/OPOD1/OPT1			V_{SS}+0.05	0.40		I_{OL}=1.00µA
Low drive cell OP2/OPOD2/OPT2			0.20	0.40		I_{OL}=2.00mA
Standard drive cell OP3/OPOD3/OPT3			0.20	0.40		I_{OL}=4.00mA
Medium drive cell OP6/OPOD6,OPT6			0.20	0.40		I_{OL}=6.00mA
Large drive cell OP12/OPOD12/OPT12			0.20	0.40		I_{OL}=12.00mA
Tristate Output Leakage Current			0.20			I_{OL}=24.00mA
		-1.00		1.00	µA	
Output short Circuit Current	I_{OZ}				mA	V_{OH}=V_{SS} or V_{DD}
Standard output OP3/OPT3/OPOD3	I_{OS}	67.00		270.00		
(Note 3) OP3/OPT3/OPOS3		37.00	135.00	150.00		V_{DD}=MAX V_{out}=V_{DD}
Operating Supply Current (per gate) (note4)			75.00		µA/MHz	V_{DD}=MAX V_{out}=0V
Input Capacitance	I_{DDOP}		1.00		pF	
Output Capcitance	C_I		5.00		pF	Any Inputs (note 5)
Bidirectional Pin Capacitance	C_{OUT}		5.00		pF	Any Outputs (note 5)
	$C_{I/O}$		7.00			Any I/O Pin (note 6)

Notes

1) Commercial grade is 0 - 70 °C, 5V ± 10% power supply voltage
2) Resistor value spreads (Min-Max):
   Low Value (Rtyp 1K) 0.5-2K ohm High Value (Rtyp 4K) 2K-8K ohm
   Low Value (Rtyp 2K) 1.0-4K ohm High Value (Rtyp 75K) 20K-250K ohm
3) Standard driver output OP3 etc. Short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
4) Excluding peripheral buffers.
5) Excludes package leadframe capacitance or bi-directional pins.
6) Excludes package.

PACKAGING

CLA70000 Series

- Wide range of surface mount and through board packages
- Ceramic equivalents to most plastic packages - for fast prototyping
- Ongoing commitment to new package development

Production quantities of the CLA70000 family are available in industry-standard ceramic and plastic packages according the codes shown below. Prototype samples are normally supplied in ceramic only.

DC	DILMON	Dual in Line, Multilayer ceramic. Brazed leads Metal Sealed Lid. Through Board
DG	CERDIP	Dual In Line, Ceramic body, Alloy leadframe, Glass Sealed, Through Board
DP	PLASDIP	Dual In Line, Copper or Alloy leadframe, Plastic Moulded. Through Board
AC	P.G.A.	Pin Grid Array, Multilayer Ceramic. Metal Sealed lid. Through Board
AC (P)	POWER P.G.A.	As above with cavity down and Cu/W heat plate
MP	SMALL OUTLINE (S.O.)	Dual In Line, 'Gullwing' Formed Leads. Plastic Moulded Surface Mount
LC	LCC	Leadless Chip Carrier. Multilayer Ceramic. Metal Sealed Lid. Surface Mount
HC	LEADED CHIP CARRIER	Quad Multilayer Ceramic. Brazed J Formed Leads. Metal Sealed Lid. Surface Mount
GC	LEADED CHIP CARRIER	Quad Multilayer Ceramic. Brazed Leads. Metal Sealed Lid. Surface Mount
GC (P)	POWER LEADED CHIP CARRIER	As above with cavity down, and Cu/W heat plate
HG	QUAD CERPAC	Quad Ceramic Body, 'J' Formed Leads. Glass Sealed. Surface Mount.
GG	CERAMIC QUAD FLATPACK	Quad Ceramic Body, 'Gullwing' Formed Leads. Glass Sealed. Surface Mount.
HP	PLCC	Quad Plastic Leaded Chip Carrier. 'J' Formed Leads. Plastic Moulded. Surface Mount
GP	PQFP	Plastic Quad Flat Pack. 'Gullwing' Formed Leads. Plastic Moulded. Surface Mount

Packaging Options

The package style and pin count information is intended only as a guide. Detailed package specification are available from Zarlink Semiconductor Design Centers on request. Available packages are being continuously updated, so if a particular package is not listed, please enquire through your Zarlink Semiconductor Sales Representative.

CLA70000 Array Package Guide

KEY

- AVAILABLE ARRAY / PACKAGE COMBINATIONS.

- PROTOTYPES ONLY

PLASTIC QUAD FLAT PACK (GP)

	70	71	72	73	74	75	76	77	78
GP44									
GP52									
GP64									
GP80									
GP100									
GP120									
GP144									
GP160									

CERAMIC QUAD FLAT PACK (GG)

	70	71	72	73	74	75	76	77	78
GG44									
GG52									
GG64									
GG80									
GG100									
GG120									
GG144									
GG160									

PLASTIC SMALL OUTLINE (MP)

	70	71	72	73	74	75	76	77	78
MP16L	■								
MP20	■								
MP24	■								
MP28	■								

CERAMIC SMALL OUTLINE (MC)

	70	71	72	73	74	75	76	77	78
MC16	■								
MC20	■								
MC24	■								
MC28	■								

PLASTIC LEADED CHIP CARRIER (HP)

	70	71	72	73	74	75	76	77	78
HP28	■	■							
HP44	■	■	■						
HP68		■	■	■					
HP84			■	■					

CO-FIRED CERAMIC LEADED CHIP CARRIER (HC)

	70	71	72	73	74	75	76	77	78
HC28	■	■							
HC44	■	■	■						
HC68		■	■	■					
HC84			■	■					

GLASS SEALED CERAMIC LEADED CHIP CARRIER (HG)

	70	71	72	73	74	75	76	77	78
HG28	■	■							
HG44	■	■	■						
HG68		■	■	■					
HG84			■	■					

CERAMIC LEADLESS CHIP CARRIER (LC)

	70	71	72	73	74	75	76	77	78
LC28	■	■							
LC44	■	■	■						
LC68			■	■					
LC84			■	■					

CERAMIC LEADED CHIP CARRIER (GC)

	70	71	72	73	74	75	76	77	78
GC132					■	■			
GC172						■	■	■	■
GC196							■	■	■

POWER CERAMIC LEADED CHIP CARRIER (GC)

	70	71	72	73	74	75	76	77	78
GC132						■	■	■	
GC172						■	■	■	■
GC196							■	■	■
GC256								■	■

PLASTIC DUAL IN LINE (DP)

	70	71	72	73	74	75	76	77	78
DP16	■								
DP22	■	■							
DP24	■	■	■						
DP28	■	■	■						
DP40	■	■	■						
DP48	■	■	■						

CERAMIC DUAL IN LINE (DC)

	70	71	72	73	74	75	76	77	78
DC16	■								
DC22	■	■							
DC24	■	■	■						
DC28	■	■	■						
DC40	■	■	■						
DC48	■	■	■						

CLA70000 Series

CERAMIC PIN GRID ARRAY (AC)

	70	71	72	73	74	75	76	77	78
AC68									
AC84									
AC100									
AC120									
AC132									
AC144									
AC180									
AC257									

POWER CERAMIC PIN GRID ARRAY (AC)

	70	71	72	73	74	75	76	77	78
AC84									
AC144									
AC208									

Quality and Reliability

- Statistical process control used in manufacture
- Regular sample screening and reliability testing
- Screening to MIL and Industrial standards available

Quality and reliability are built into the product by statistical control of all processing operations and by minimizing random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures, recording of batch-by-batch data, using traceability procedures and provision of appropriate equipment and facilities to perform sample screening and conformance testing on finished product.

A common information management system is used to monitor the manufacturing of Zarlink CMOS and Bipolar processes. All products benefit from the use of this integrated monitoring system throughout all manufacturing operations leading to high quality standards for all technologies.

ZARLINK SEMICONDUCTOR

http://www.zarlink.com

World Headquarters - Canada
Tel: +1 (613) 592 0200
Fax: +1 (613) 592 1010

North America - West Coast
Tel: (858) 675-3400
Fax: (858) 675-3450

North America - East Coast
Tel: (978) 322-4800
Fax: (978) 322-4888

Asia/Pacific
Tel: +65 333 6193
Fax: +65 333 6192

Europe, Middle East, and Africa (EMEA)
Tel: +44 (0) 1793 518528
Fax: +44 (0) 1793 518581