CLA200 Series

CMOS Gate Arrays

Advance Information

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INTRODUCTION

The CLA200 Series Arrays from Zarlink Semiconductor offer designers the capability to integrate designs of more than 2 million gates. There are 14 fixed arrays optimised for low to medium complexity designs ranging from 11K used gates up to 628K used gates. For larger designs optimised arrays can be built with up to 3 million available gates. Using automated gate array base constructor software, a tailor made optimised gate array can be built to customers requirements which gives designers the ability to specify the optimum die size whilst retaining the benefits of standard gate arrays. Utilising a gate array architecture allows the base arrays to be pre-manufactured enabling gate array prototype lead time to be offered.

Supported with high quality design kits for a range of industry standard CAE tools, the CLA200 Series provide customers with a low risk, low cost solution and fast time to market.

FEATURES

- 0.35µm drawn Channel Length
- Three (CLT) and Four (CLQ) layer metal options
- Automated base array constructor for optimised arrays with up to 3 million gates
- Low Power, 0.4µW/MHz/Gate at 3V (2-input NAND with two loads)
- 135ps gate delay for 2-input NAND with two loads (3V)
- High density staggered pad ring
- Wide range of package options including QFP & BGA
- Characterised for operation from 1.8V to 3.6V
- 2V and 3.3V I/O capability on the same device
- 5V tolerant inputs, outputs and bidirectionals
- Accurate delay modelling for gates and tracks with *sign off quality* CAE design libraries for QuickSim II and Verilog-XL
- VITAL Sign off with Synopsys VSS Simulator
- CAD libraries optimised for synthesis
- Methodologies for low clock skew
- Full set of I/O cells for direct pad synthesis
- Variable output slew rates for low noise
- IDDQ Testing

BENEFITS

- Fast Customer Time To Market
  - Direct sign-off on Industry Standard CAE tools
  - Comprehensive Industry Standard CAE tools
  - SystemBuilder™ megacell libraries
  - World-wide design center support
  - Reliable prototype and production delivery
  - Dual silicon sources
- Cost -effective solutions
  - Optimised silicon architecture for high density silicon utilisation
  - ISO9001 Factory with Statistical process control for optimum yield

FIXED ARRAY SIZES

	Available Pads	Available Gates	Usable Gates TLM	Usable Gates QLM
CLA201	48	17,860	10,700	14,300
CLA202	64	30,012	18,000	24,000
CLA203	80	45,300	27,200	36,200
CLA204	100	68,736	41,200	55,000
CLA205	128	109,980	66,000	88,000
CLA206	144	137,812	82,700	110,200
CLA207	160	168,780	101,300	135,000
CLA208	176	202,884	121,700	162,300
CLA209	208	280,500	168,300	224,400
CLA210	240	370,660	222,400	296,500
CLA211	272	473,364	284,000	378,700
CLA212	304	588,612	353,200	470,900
CLA213	328	683,280	410,000	546,600
CLA214	352	785,004	471,000	628,000

OPTIMISED ARRAYS

The following table illustrates examples of possible compiled array sizes.

	Available Pads	Available Gates	Usable Gates TLM	Usable Gates QLM
CLA2xx	400	989,740	590,000	790,000
CLA2xx	552	1,879,776	1,100,000	1,500,000
CLA2xx	700	3,018,424	1,800,000	2,400,000

ARRAY ARCHITECTURE

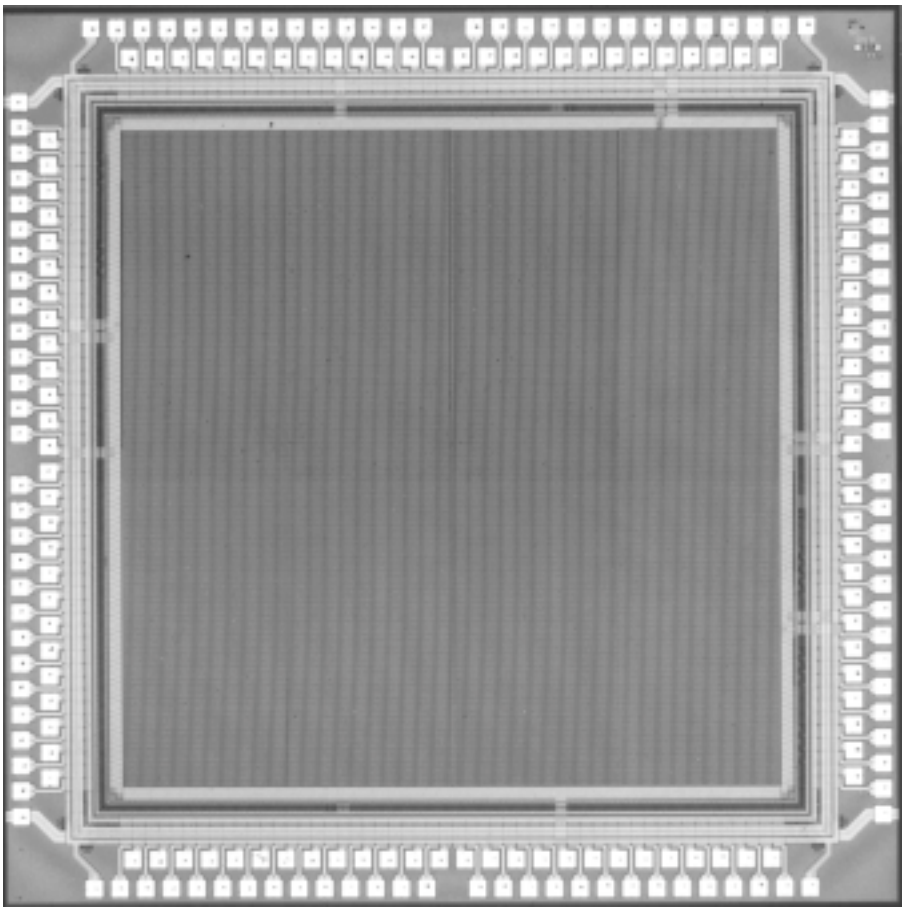
The CLA200 Series gate array family is based on a sea of gates array architecture. The arrays consist of a core of transistors, overlaid with a core power supply grid, ringed by three concentric pairs of VDD and GND supply rail. The OPVDD rail can be split to form an extra VDD rail named split supply VDD (SSVDD) to allow mixed voltages interfaces on the same device. The outermost area of the die has pads for I/O and power supplies.

Each array has a number of preferred pads designated for power supply, This allows the use of a generic probe card to reduce cost and allow rapid prototype turnaround.

Connections within the array are made using three or four layers of metal. Each pad has one I/O location associated with it.

CORE ARCHITECTURE

The core area consists of a dense array of core cells. Each core cell contains four transistors, two NMOS and two PMOS, whose sizes have been optimised for high density and low power. These are built from one structure consisting of a shared central source/drain region with independently available polysilicon gates. This core cell layout has been designed to allow very efficient metal interconnections including over-cell routing resulting in high utilisation. The core architecture also allows highly efficient register file RAM to be implemented.



CELL LIBRARIES

The CLA200 Series is supported by a comprehensive cell library which is optimised for synthesis and includes basic logic gates, oscillators and memories. In addition a range of ready made system Macro functions such as a UART is also available.

Core Microcells

A wide range of core microcells are available including basic logic cells, combinatorial logic, latches and D- Type Flip-Flops. The basic logic cells, such as inverters, NAND and NOR gates are available with a choice of drive strengths allowing designers to make trade-offs between speed, power and silicon area. A range of D-Type flip-flops is also available including versions with multiplexers to facilitate Scan path testing.

I/O Cells

The CLA200 series design libraries contain a wide variety of Input, Output and Bi-directional cells, each of which is available in a number of variants.

CLA200 series I/Os have the following features:

- Cell library contains distinct and complete inputs, outputs and bidirectionals to allow direct pad synthesis
- Selectable I/O output speeds allow the designer to maintain low noise and reduce the number of power supply pins if output speed is not critical
- Choice of Output drive strengths
- Device I/O can run at a higher voltage than the core with no static power consumption while still benefiting from a low voltage, low power core
- All input and output cells are non inverting
- The input TTL and CMOS level detection circuits use low noise power rails
- I/O cells are optimised for 3.3V +/- 10% and are fully functional down to 1.8V with derated current and speed
- Inputs and bidirectionals are available with hold options. The hold option maintains the last value (high or low) when all drive to the pin is withdrawn.
- All inputs have an optional internal pull-up or pull-down resistor which are gated to enable IDDQ testing.
- 5V tolerant inputs and open drain outputs are available for all devices
- Mixed Voltage I/O Capability
- Output currents up to 12mA @ 3.3V supported from a single I/O cell. 24mA current drive available using two output cells

The CLA200 has four separate VDD supply rails and two GND rails, one VDD rail for the core, one for input buffers, and two for output areas of the chip. The intermediate buffer supply rail can be completely isolated for very low noise. This offers the benefit of good noise immunity with multiple supply voltage capability to suit the application. The mixed 2 and 3.3V I/O capability can be used for power saving or interfacing with 2V and 3.3V systems. 5V tolerant input and output cells are also available to offer the advantages of a very low power core whilst interfacing to 5V systems.

Electrostatic discharge (ESD) protection is built into the input and output cells, and is specified to withstand at least 2kV (human body model). The structure and process is also highly resistant to latch-up and able to withstand forward bias currents in excess of 200mA.

SystemBuilder™

The SystemBuilder™ library contains a broad range of macrofunctions designed to improve designers efficiency. All of the SystemBuilder™ macrofunctions are supplied as synthesizable RTL models for both VHDL and Verilog. In addition each macrofunction is fully supported with synthesis scripts, test-benches and full documentation.

The SystemBuilder™ library includes the following function :

- Standard Microprocessor Cores including 8048, 8051 & 8086
- Standard Microprocessor peripherals including DMA controllers, programmable interval timers, real time clock & Programmable interrupt controllers.
- Floppy Disc/Tape functions including controllers and data separators
- Standard Serial Communications controllers including 85C30, 16C450, 8251 & 8250
- Bus interface cores including PCMCIA, Ethernet, IEEE1284, USB and PCI

In addition to the above functional replacements for industry standard devices the SystemBuilder™ library also contains a range of clearly defined functions that are frequently required for Systems Level integration (SLI) ASIC's.
Further functions are continually being added. An up to date list may be obtained from all Zarlink Semiconductor Sales and Design Centers.

Memory Paracells
The standard CLA200 Series gate array architecture has been designed to allow for the implementation of memory within the design. A memory compiler (PMG) is available which allows designers to specify the number of bits and words required. The PMG can automatically create design views for all of the supported CAE tools.
Features of the Gate Array memory include :

- Single and Dual Port memories
- Dual port supports: one read and one write port
- RAM sizes from 16 to 16k bits
- Word length from 2 to 64 bits in steps of 1
- Address range from 8 to 256 words in steps of 2
- Zero static DC power consumption (only intrinsic leakage)
- Separate input and output data busses

Typical Memory speeds for a range of Gate Array RAMs operating at 3.3V , 25ºC are summarised in the table 1 below.

Parameter					**Units**
Size	16	512	512	16K	Bits
No. Words	8	8	256	256	Words
No. Bits	2	64	2	64	Bits
Read Access	1.2	2.1	8.5	9.4	ns
Write Cycle	6.2	6.5	6.5	6.9	ns
Cycle Power	0.37	0.25	3.0	5.8	mW/MHz

Table. 1

CLOCK AND POWER DISTRIBUTION

It is known that large, complex designs working at high speed are vulnerable to problems associated with poor clock and power distribution. Zarlink Semiconductor has published design notes that describe approaches to clock and power distribution.

Clock Distribution
The CLA200 Series supports a number of Clock distribution methodologies which may be implemented depending on the particular design and the CAD tools being used by the designer. For small designs with a light clock load, a single large buffer may be sufficient. For large designs, with large clock loads, a clock grid or clock tree is recommended to avoid clock skew and metal electromigration in the clock network. Clock trees can either be synthesized or manually specified as a clock hierarchy by the designer.

The CLA200 Series clock grid methodology uses up to three stages of buffers, where each stage drives a grid which feeds the next stage cells (figure 1).
The final stage grid is a starting point for routing to the actual clocked inputs. Figure 2 illustrates the layout of each buffer stage, which is done automatically at layout.

Power Distribution
CLA200 can be used from 1.8 to 3.3V, giving great flexibility of supply voltage. Core supply can be chosen from a nominal 2V or 3.3V, with mixed voltage I/O available if the core supply is 2V. I/O cells are available as either CMOS or TTL compatible for all supply configurations.

The CLA200 Series utilises a grid methodology for power distribution. This grid, which is automatically constructed during layout, uses metal layers one and three for horizontal power rails and metal layer two for vertical connections. Metal layer four is also available for vertical connections, which may be useful on some larger arrays. Methods of implementation are available for use with flat layout, manual methods, or hierarchical layout.

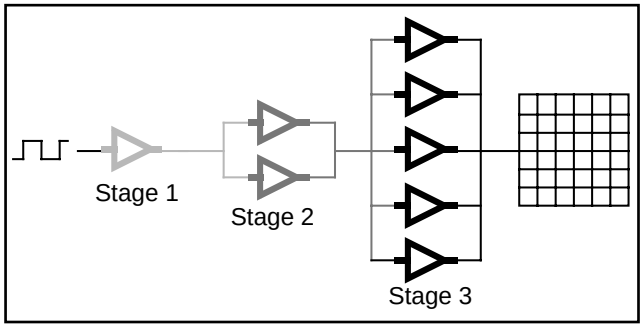


Figure.1

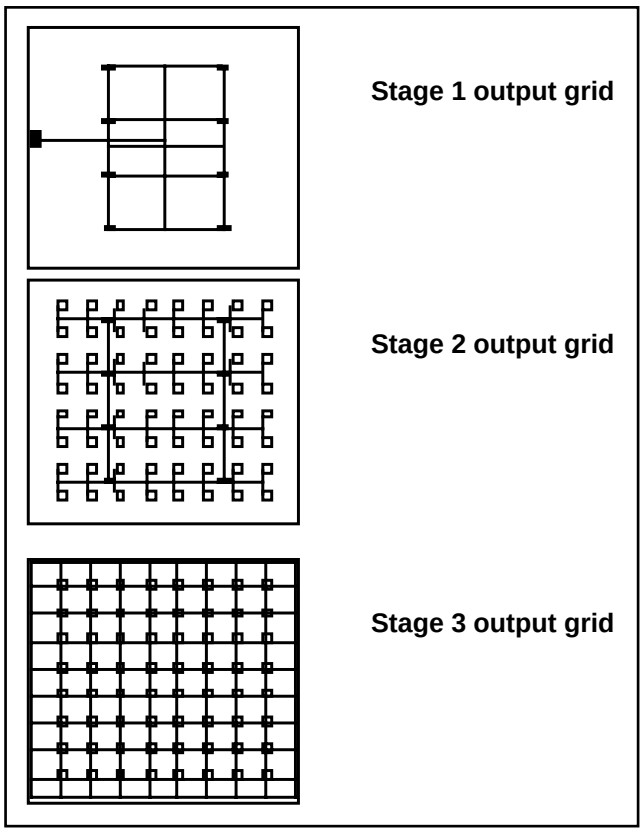


Figure.2

Advanced Delay Modelling
Delay calculation includes the following features:

- Edge speed modelling
- Pin to pin timings
- Non-linear delay modelling
- Accurate delay derating
- Conditional delay modelling

Pin to Pin Delays
Delay models use times between individual input and output pins for both rising and falling delays, as illustrated in figure 3 below.

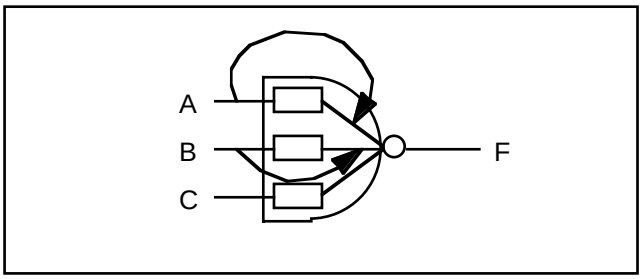


Figure.3

Calculation uses individual pin to pin delays, e.g. A to F and B to F, which improves simulation accuracy by modelling the considerable variation in delay between different input pins. For complex gates (e.g. AND-NOR gates or adders) the variation is up to 40%. For simple NAND and NOR logic gates the typical variation is 20%.

Non-linear Curve Fitting
For fast input edges (0.5ns) delay time increases linearly with the output load, whereas for high output loads delay increases linearly with edge speed. Delays for slow input edges and light input loads do not follow the linear model, so a simple linear model cannot represent delays accurately. A more complex equation, which includes interaction between edge and load factors, is used to model delays.

Thermal Management
The increase in speed and density available through advanced CMOS processes results in a corresponding increase in power dissipation. Designs can now have more than half a million used gates and chip power consumption is an important issue.

The CLA200 series offers the following:

- Lower power CMOS for improved thermal management
- Software constructed power grids for efficient power distribution
- Copper lead frame QFPs for lower thermal resistance
- High pinout power packages available

DESIGN SUPPORT

Zarlink Semiconductor offers fully flexible design support allowing customer a wide choice of design interfaces. Whichever design interface is chosen each customer design is supported full-time by an applications engineer with software support from the Zarlink Semiconductor group that produces the design kits. Four main design interfaces are supported. These are described in table 2 below.

The design process incorporates a design audit procedure to verify compliance and to ensure manufacturability. The procedure includes three design reviews held at key stages of the design process to ensure device performance and timescales.

Design Review 1: Held at the beginning of the design cycle to check and agree on performance, packaging, specification and design time scales

Design Review 2: Held after logic simulation but prior to layout to ensure satisfactory functionality, timing performance and adequate fault coverage

Design Review 3: Held after layout and post layout simulation verification of satisfactory design performance after insertion of actual track loads. This is the final check of all device specifications prior to prototype manufacture

CAE SUPPORT

The CLA200 Series is supported with comprehensive design kits for industry standard design tools including Mentor Graphics, Cadence Design Systems, and Synopsys. A VITAL compliant library is also supported.

Features of design kits include :

- Sign-off simulation with Mentor or Cadence
- VITAL sign off with Synopsys VSS
- Full top down design flow support
- Synthesis with Synopsys, Mentor or Cadence
- Electrical Rule Checks (ERC)
- Paracell Model Generator (PMG)
- VIEWLOGIC VCS simulator supported
- Sunrise ATPG supported
- Advanced Pin to Pin Delay modelling
- Floorplanning with Compass Chipplanner
- Direct routes to layout and test

Use of the design kits for sign-off enable customers to sign-off their design without the need to re-simulate on a golden simulator. This has the benefit of customers not having to learn new tools. There is also no overhead in engineering effort or time taken rechecking simulation results.

Interface	Description
1	Netlist interface. Customer completes logical design and simulation using a design kit. Zarlink Semiconductor performs layout only.
2	Technology mapping. Zarlink Semiconductor converts a customer-supplied netlist created using a non-Zarlink Semiconductor library (e.g., FPGA or other vendor's library) and simulates using customer-supplied test patterns. The production test program is based on these test patterns. Zarlink Semiconductor performs layout.
3	Layout interface. Customer completes logical design and simulation. Customer performs layout.
4	Turnkey. Zarlink Semiconductor completes schematic capture or logic synthesis or both based on a paper schematic or specification or VHDL or Verilog description. Zarlink Semiconductor performs layout.

Table. 2 Zaralink Semiconductor Design interfaces

DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage (VDD)	-0.5	5.0	V
Bias for 5V tolerant cells (VBIAS) (see note 1)	-0.5	7.0	V
Input Voltage	-0.5	VDD + 0.5	V
Output Voltage	-0.5	VDD + 0.5	V
Static Discharge (HBM)		2	KV
Storage Temperature			
Ceramic	-65	150	°C
Plastic	-55	150	°C

Note 1: Only required for 5V tolerant push-pull outputs

Exceeding the absolute maximum ratings may cause permanent damage to the device. Extended exposure at the maximum ratings will affect device reliability.

HBM stands for Human Body Model

NORMAL OPERATING CONDITIONS

Parameter	Min	Max	Units
Supply Voltage (VDD)	1.8	3.6	V
Bias for 5V tolerant cells	4.5	5.5	V
Input Voltage	0.0	VDD	V
Input Voltage on 5V Tolerant I/P's with VDD 2.7V	0.0	VBIAS	V
Output Voltage	0.0	VDD	V
DC Current per Bond Pad	-	30	mA
Junction Temperature	-55	150	°C
Ambient Temperature-			
Commercial	0	70	°C
Industrial	-40	85	°C
Military	-55	125	°C

INPUT DC ELECTRICAL SPECIFICATION

Typical characteristics are taken at a nominal supply voltage of 3.3 volts at 25°C. Min and Max values are defined over all process conditions from -40 to +85°C.

Parameter	Value			Units	
	Min.	Typ.	Max.		
Input Loads					VDD = 3.6V
Input Leakage	-1		+1	µA	No Pull Up/Down Cells
Output (Tristate) Leakage	-1		+1	µA	No Pull Up/Down Cells
Input Capacitance		4		pF	Not including package
Output Capacitance 01, 03, 06		4		pF	Not including package
Output Capacitance 12		8		pF	Not including package
					3.0V < VDD < 3.6V
Weak Pull-Up Current	-16	-30	-50	µA	Input at 0V
Weak Pull-Down Current	13	30	64	µA	Input at VDD
Input Hold Cell - HD					3.0V < VDD < 3.6V
Hold-Up Current	-12	-24	-38	µA	@ 55% of VDD
Hold-Down Current	8	19	38	µA	@ 30% of VDD
Hold Threshold		1.48		V	@ 3.3V
Input Levels					
All Cells Types					
CMOS - Vil			0.3 VDD		1.8V < VDD < 3.6V
CMOS - Vih	0.7 VDD				1.8V < VDD < 3.6V
TTL - Vil			0.8	V	3.0V < VDD < 3.6V
TTL - Vih	2.0			V	3.0V < VDD < 3.6V
Vt-		1.2		V	@ 3.3V
Vt+		1.6		V	@ 3.3V

CMOS and TTL Output Levels

All characteristics are over all process conditions from -40 to +85°C

	Parameter	Min	Typ	Max	Units	Conditions
CMOS	Vol			0.2 VDD	V	1.8V < VDD < 2.2V
	Voh	0.8 VDD				
TTL	Vol			0.4	V	3.0V < VDD < 3.6V
	Voh	0.8 VDD				

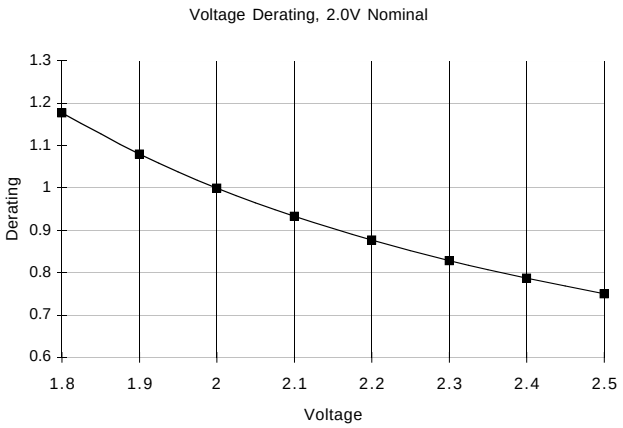
Note: These figures apply for all Output Current Conditions shown below

Output Currents

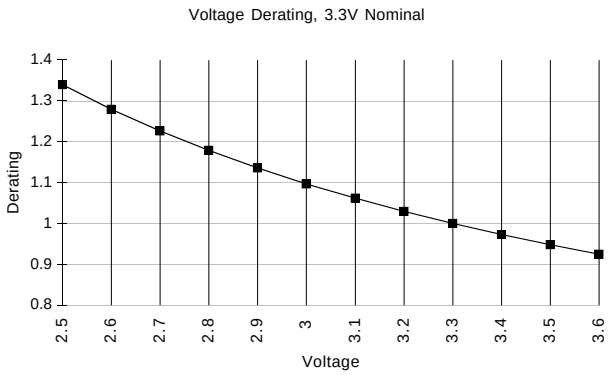
	Drive Strength							
	x01		x03		x06		x12	
Device Voltage	I_{ol}	I_{oh}	I_{ol}	I_{oh}	I_{ol}	I_{oh}	I_{ol}	I_{oh}
1.8V < VDD < 2.2V	1mA	1mA	3mA	1.5mA	6mA	3mA	12mA	6mA
2.2V < VDD < 2.7V	1mA	1mA	4mA	3mA	8mA	6mA	16mA	12mA
2.7V < VDD < 3.3V	2mA	2mA	2mA	2mA	10mA	10mA	20mA	20mA
3.3V < VDD < 3.6V	2mA	2mA	2mA	2mA	12mA	12mA	24mA	24mA

Voltage Derating

Voltage derating is divided into two ranges, one for designs at 2.0V nominal and one for 3.3V nominal. The following figures show how gate delay varies with supply voltage.

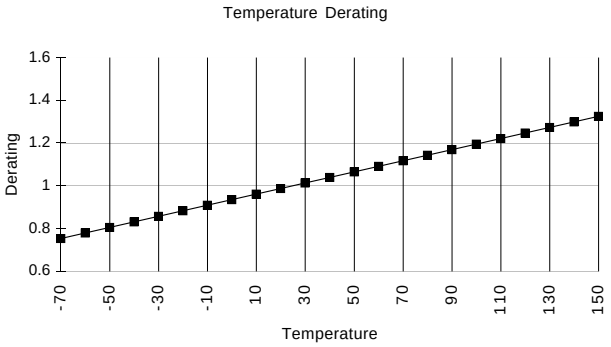


Derating for a 2.0V Supply (2 Volt normalised to 1)



Derating for a 3.3V Supply (3.3 Volt normalised to 1)

Temperature Derating
Note that it is important to use the junction and not the ambient temperature for worst-case simulations.



Process Derating

Speed	Derating Factor
Slow	1.41
Typical	1.00
Fast	0.71

MANUFACTURING

The CLA200 Series product is manufactured in Zarlink Semiconductor advanced wafer fabrication facility near Plymouth, England. This facility is a purpose-built, vibration-free facility equipped with the latest automated technology for 8 inch wafer processing. This equipment utilises mini-environments together with the use of SMIF boxes to achieve ultra clean processing conditions. Computer Aided Manufacture ensures production efficiency. In addition to the world class wafer fabrication facility, the probe and final test areas are equipped with the latest analog and digital testers. Zarlink Semiconductor is committed to continuous investment to provide state-of-the-art CMOS ASICs.

A qualified second source for this silicon process is also available.

QUALITY AND RELIABILITY

At Zarlink Semiconductor, quality and reliability are built into the product by statistical control of all processing operations and by minimising random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures with recording of batch by batch data using computerised WIP tracking systems.
A common information management system is used to monitor the manufacturing of Zarlink Semiconductor CMOS processes and operations. All products benefit from the use of this integrated monitoring systems resulting in the highest quality standards for all technologies.

Further information and reliability results are contained in the Quality MOS brochure, available from Zarlink Semiconductor Sales Offices

PACKAGING

The CLA200 Series is available in a wide range of metric quad flat packages (MQFP) and plastic ball grid array packages (BGA) . The currently supported Die size and Package combinations are shaded. The package style and pin count information is intended only as a guide. Detailed package specifications are available from Zarlink Semiconductor Design Centres on request. Additional packages are being regularly added to this list, so if a particular package is not listed, please enquire through your Zarlink Semiconductor sales representative. A stock is held of the preferred packages to ensure a fast prototype assembly turn around. Alternative array size to package combinations are available, but not always stocked.

CLA200 FAMILY PACKAGE MATRIX **PREFERRED FORMATS**		**ARRAY**		**201**	**202**	**203**	**204**	**205**	**206**	**207**	**208**	**209**	**210**	**211**	**212**	**213**	**214**
		No I/OS		**48**	**64**	**80**	**100**	**128**	**144**	**160**	**176**	**208**	**240**	**272**	**304**	**328**	**352**
Type	Pins	Body Size	Pitch														
MQFP	44	10x10x2.0	0.80	■	■	■	■	■	■	■	■	■					
FQFP	64	10x10x1.4	0.50		■	■	■	■	■	■	■	■					
MQFP	64	10x10x.2.0	0.80		■	■	■	■	■	■	■	■					
MQFP	80	14x14x1.4	0.65			■	■	■	■	■	■	■	■	■			
MQFP	80	14x20x2.8	0.80			■	■	■	■	■	■	■	■	■			
FQFP	100	14x14x1.4	0.50				■	■	■	■	■	■	■	■	■	■	■
MQFP	100	14x20x2.8	0.65				■	■	■	■	■	■	■	■			
MQFP	120	28x28x3.4	0.80					■	■	■	■	■	■	■	■	■	■
MQFP	128	28x28x3.4	0.80					■	■	■	■	■	■	■	■	■	■
FQFP	144	20x20x1.4	0.50						■	■	■	■	■	■	■	■	
MQFP	144	28x28x3.4	0.65						■	■	■	■	■	■	■	■	■
FQFP	160	24x24x1.4	0.50							■	■	■	■	■	■	■	■
MQFP	160	28x28x3.4	0.65							■	■	■	■	■	■	■	■
FQFP	176	24x24x1.4	0.50								■	■	■	■	■	■	■
FQFP	208	28x28x3.4	0.50								■	■	■	■	■	■	■
BGA	169	23x23x1.7	1.50							■	■	■	■	■	■	■	■
BGA	225	27x27x1.7	1.50									■	■	■	■	■	■
BGA	256	27x27x1.7	1.27												■	■	■
BGA	313	35x35x1.7	1.27												■	■	■
BGA	352	35x35x1.7	1.27													■	■

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