240pin Fully Buffered DDR2 SDRAM DIMMs based on 512 Mb F-ver.

This Hynix's Fully Buffered DIMM is a high-bandwidth & large capacity channel solution that has a narrow host interface. Hynix's FB-DIMM features novel architecture including the Advanced Memory Buffer that isolates the DDR2 SDRAMs from the channel. This single component located in the front side center of each DIMM, acts as a repeater and buffer for all signals and commands which are exchanged between the host controller and the DDR2 SDRAMs including data in and output. The AMB communicates with the host controller and adjacent DIMMs on a system board using an industry standard Differential Point to Point Link Interface at 1.5V power.

The AMB also allows buffering of memory traffic to support large memory capacities. All memory control for the DDR2 SDRAM devices resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access and power management. The AMB interface is responsible for handling channel and memory requests to and from the local FBDIMM and for forwarding request to other FBDIMMs on the memory channel.

FEATURES

- 240 pin Fully Buffered ECC dual In-Line DDR2 SDRAM Module
- JEDEC standard Double Data Rate2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8V +/- 0.1V Power Supply
- All inputs and outputs are compatible with SSTL_1.8 interface
- Built with 512Mb DDR2 SDRAMs in 60ball FBGA
- Host interface and AMB component industry standard compliant
- MBIST & IBIST test functions
- 4 Bank architecture
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- Fully differential clock operations (CK & $\overline{CK}$)
- Programmable Burst Length 4 / 8 with both sequential and interleave mode
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms
- Serial presence detect with EEPROM
- 133.35 x 30.35 mm form factor
- RoHS compliant
- Full Module Heat Spreader

This document is a general product description and is subject to change without notice. Hynix Semiconductor does not assume any responsibility for use of circuits described. No patent licenses are implied.

ORDERING INFORMATION

Part Name	Density	Org.	# of DRAMs	# of ranks	AMB		H. S type	Height
					Vendor	Version		
HMP564F7FFP8C-C4/Y5N3	512MB	64Mx72	9	1	Intel	D1	Full Module	30.35mm
HMP564F7FFP8C-C4/Y5/S5/S6D3					IDT	C1		
HMP512F7FFP8C-C4/Y5N3	1GB	128Mx72	18	2	Intel	D1		
HMP512F7FFP8C-C4/Y5/S5/S6D3					IDT	C1		
HMP525F7FFP4C-C4/Y5N3	2GB	256Mx72	36	2	Intel	D1		
HMP525F7FFP4C-C4/Y5D3					IDT	C1		

Note:
*: The 16th and 17th digits stand for AMB vendor and revision.

SPEED GRADE & KEY PARAMETERS

Speed Grade	C4	Y5	S5/6	Unit
DDR2 DRAM Speed Grade	DDR2 533 4-4-4	DDR2 667 5-5-5	DDR2 800 5-5-5 / 6-6-6	
FB-DIMM Speed Grade	PC2 4200	PC2 5300	PC2 6400	
FB-DIMM Peak Channel Throughput	6.4	8.0	9.6	GByte/S
FB-DIMM Link Transfer Rate	3.2	4.0	4.8	GT/s

ADDRESS TABLE

Density	Org.	Ranks	SDRAMs	# of DRAMs	# of row/bank/column Address	Refresh Method
512MB	64M x 72	1	64Mbx8	9	14(A0~A13)/2(BA0~BA1)/10(A0~A9)	8K / 64ms
1GB	128M x 72	2	64Mbx8	18	14(A0~A13)/2(BA0~BA1)/10(A0~A9)	8K / 64ms
2GB	256M x 72	2	128Mbx4	36	14(A0~A13)/2(BA0~BA1) 11(A0~A9,A11)	8K / 64ms

Input/Output Functional Description

Pin Name	type	Polarity	Function Description	Count
SCK	Input	Positive	System clock input	1
$\overline{\text{SCK}}$	Input	Negative	System clock input	1
PN[13:0]	Output	Positive	Primary Northbound Data	14
$\overline{\text{PN}}$[13:0]	Output	Negative	Primary Northbound Data	14
PS[9:0]	Input	Positive	Primary Southbound Data	10
$\overline{\text{PS}}$[9:0]	Input	Negative	Primary Southbound Data	10
SN[13:0]	Output	Positive	Secondary Northbound Data	14
$\overline{\text{SN}}$[13:0]	Output	Negative	Secondary Northbound Data	14
SS[9:0]	Input	Positive	Secondary Southbound Data	10
$\overline{\text{SS}}$[9:0]	Input	Negative	Secondary Southbound Data	10
SCL	Input	-	Serial Presence Detect (SPD) Clock Input	1
SDA	Input / Output	-	SPD Data Input / Output	1
SA[2:0]	Input	-	SPD Address inputs, also used to select the DIMM number in the AMB	3
VID[1:0]	Input	-	Voltage ID: These pins must be unconnected for DDR2-based Fully buffered DIMMs	2
$\overline{\text{RESET}}$	Input	Active Low	AMB reset signal	1
RFU	-	-	Reserved for Future Use	16
VCC	Supply	+1.5V	AMB Core Power and AMB channel Interface Power(1.5volt)	8
VDD	Supply	+1.8V	DRAM Power and AMB DRAM I/O Power	24
VTT	Supply	+0.9V	DRAM Address/Command/Clock Termination Power(VDD/2)	4
VDDSPD	Supply	+3.3V	SPD Power	1
VSS	Supply		Ground	80
DNU/ M_Test	- / Analog	- / 0.9V	The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected(DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.	1
			Total	240

PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	41	PN13	81	VSS	121	VDD	161	SN13	201	VSS
2	VDD	42	VSS	82	PS4	122	VDD	162	VSS	202	SS4
3	VDD	43	VSS	83	PS4	123	VDD	163	VSS	203	SS4
4	VSS	44	RFU*	84	VSS	124	VSS	164	RFU*	204	VSS
5	VDD	45	RFU*	85	VSS	125	VDD	165	RFU*	205	VSS
6	VDD	46	VSS	86	RFU*	126	VDD	166	VSS	206	RFU*
7	VDD	47	VSS	87	RFU*	127	VDD	167	VSS	207	RFU*
8	VSS	48	PN12	88	VSS	128	VSS	168	SN12	208	VSS
9	VCC	49	PN12	89	VSS	129	VCC	169	SN12	209	VSS
10	VCC	50	VSS	90	PS9	130	VCC	170	VSS	210	SS9
11	VSS	51	PN6	91	PS9	131	VSS	171	SN6	211	SS9
12	VTT	52	PN6	92	VSS	132	VCC	172	SN6	212	VSS
13	VCC	53	VSS	93	PS5	133	VCC	173	VSS	213	SS5
14	VSS	54	PN7	94	PS5	134	VSS	174	SN7	214	SS5
15	VTT	55	PN7	95	VSS	135	VTT	175	SN7	215	VSS
16	VID1	56	VSS	96	PS6	136	VID0	176	VSS	216	SS6
17	RESET	57	PN8	97	PS6	137	DNU/M_Test	177	SN8	217	SS6
18	VSS	58	PN8	98	VSS	138	VSS	178	SN8	218	VSS
19	RFU**	59	VSS	99	PS7	139	RFU**	179	VSS	219	SS7
20	RFU**	60	PN9	100	PS7	140	RFU**	180	SN9	220	SS7
21	VSS	61	PN9	101	VSS	141	VSS	181	SN9	221	VSS
22	PN0	62	VSS	102	PS8	142	SN0	182	VSS	222	SS8
23	PN0	63	PN10	103	PS8	143	SN0	183	SN10	223	SS8
24	VSS	64	PN10	104	VSS	144	VSS	184	SN10	224	VSS
25	PN1	65	VSS	105	RFU**	145	SN1	185	VSS	225	RFU*
26	PN1	66	PN11	106	RFU**	146	SN1	186	SN11	226	RFU*
27	VSS	67	PN11	107	VSS	147	VSS	187	SN11	227	VSS
28	PN2	68	VSS	108	VDD	148	SN2	188	VSS	228	SCK
29	PN2	Key		109	VDD	149	SN2	Key		229	SCK
30	VSS	69	VSS	110	VSS	150	VSS	189	VSS	230	VSS
31	PN3	70	PS0	111	VDD	151	SN3	190	SS0	231	VDD
32	PN3	71	PS0	112	VDD	152	SN3	191	SS0	232	VDD
33	VSS	72	VSS	113	VDD	153	VSS	192	VSS	233	VDD
34	PN4	73	PS1	114	VSS	154	SN4	193	SS1	234	VSS
35	PN4	74	PS1	115	VDD	155	SN4	194	SS1	235	VDD
36	VSS	75	VSS	116	VDD	156	VSS	195	VSS	236	VDD
37	PN5	76	PS2	117	VTT	157	SN5	196	SS2	237	VTT
38	PN5	77	PS2	118	SA2	158	SN5	197	SS2	238	VDDSPD
39	VSS	78	VSS	119	SDA	159	VSS	198	VSS	239	SA0
40	PN13	79	PS3	120	SCL	160	SN13	199	SS3	240	SA1
		80	PS3					200	SS3		

NC= No Connect, RFU= Reserved for Future Use.

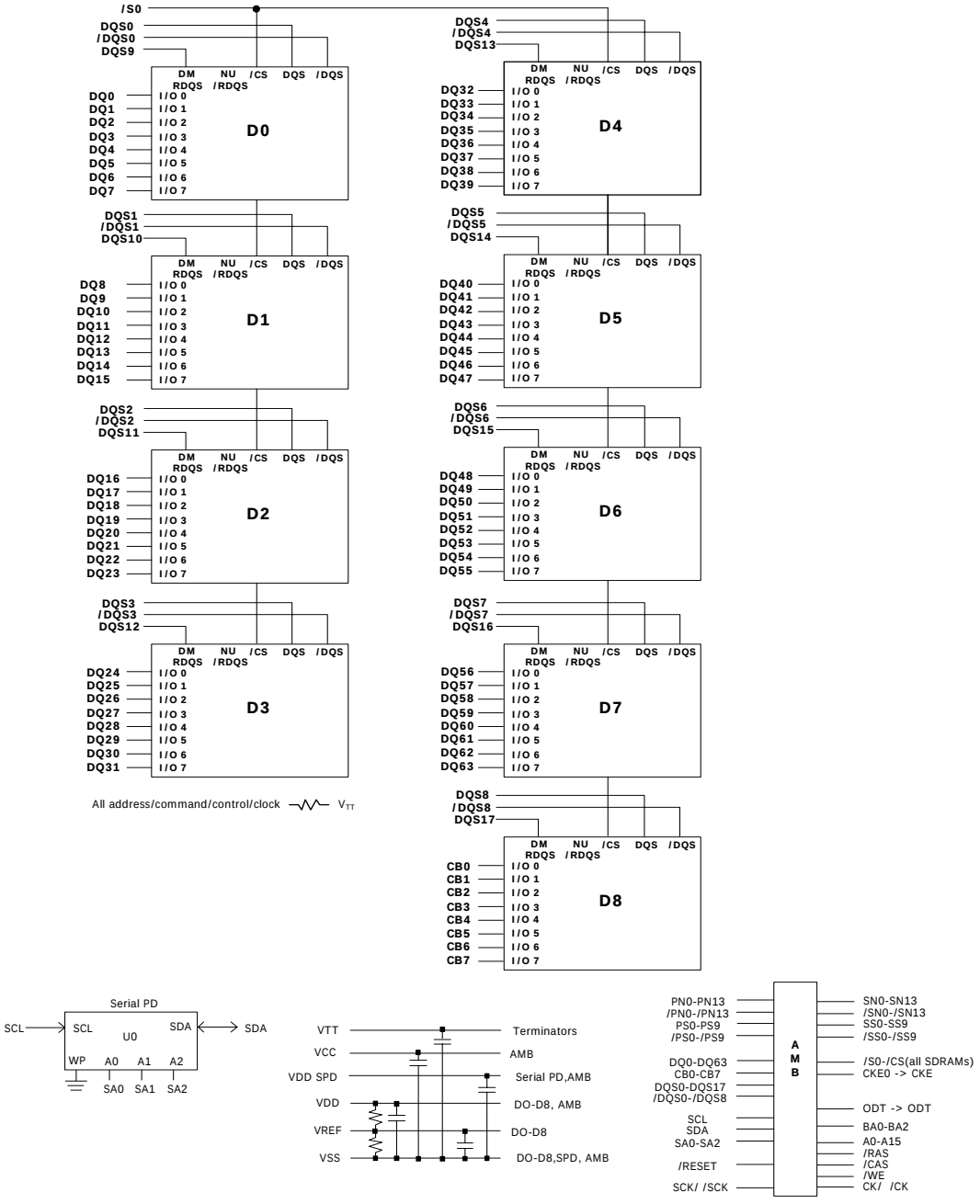
Note:

*: These pin positions are reserved for forwarded clocks to be used in future module implementations

**: These pin positions are reserved for future architecture flexibility

1) The following signals are CRC bits and thus appear out of the normal sequence:
PN12/ PN12, SN12 / SN12, PN13 / PN13, SN13 / SN13,PS9 / PS9, SS9 / SS9

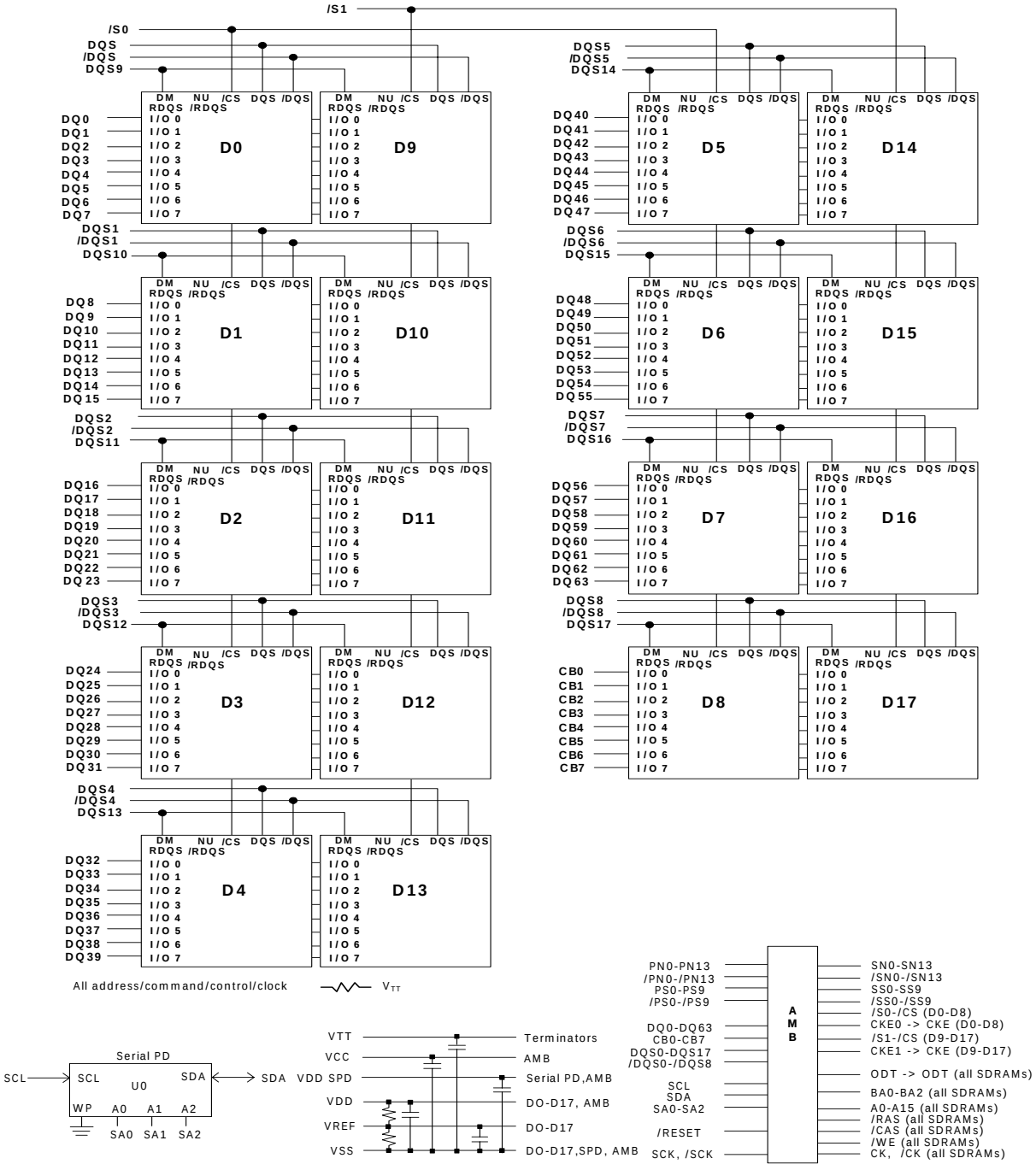
FUNCTIONAL BLOCK DIAGRAM
512MB(64Mbx72) ECC FB-DIMM



Notes :

1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock.

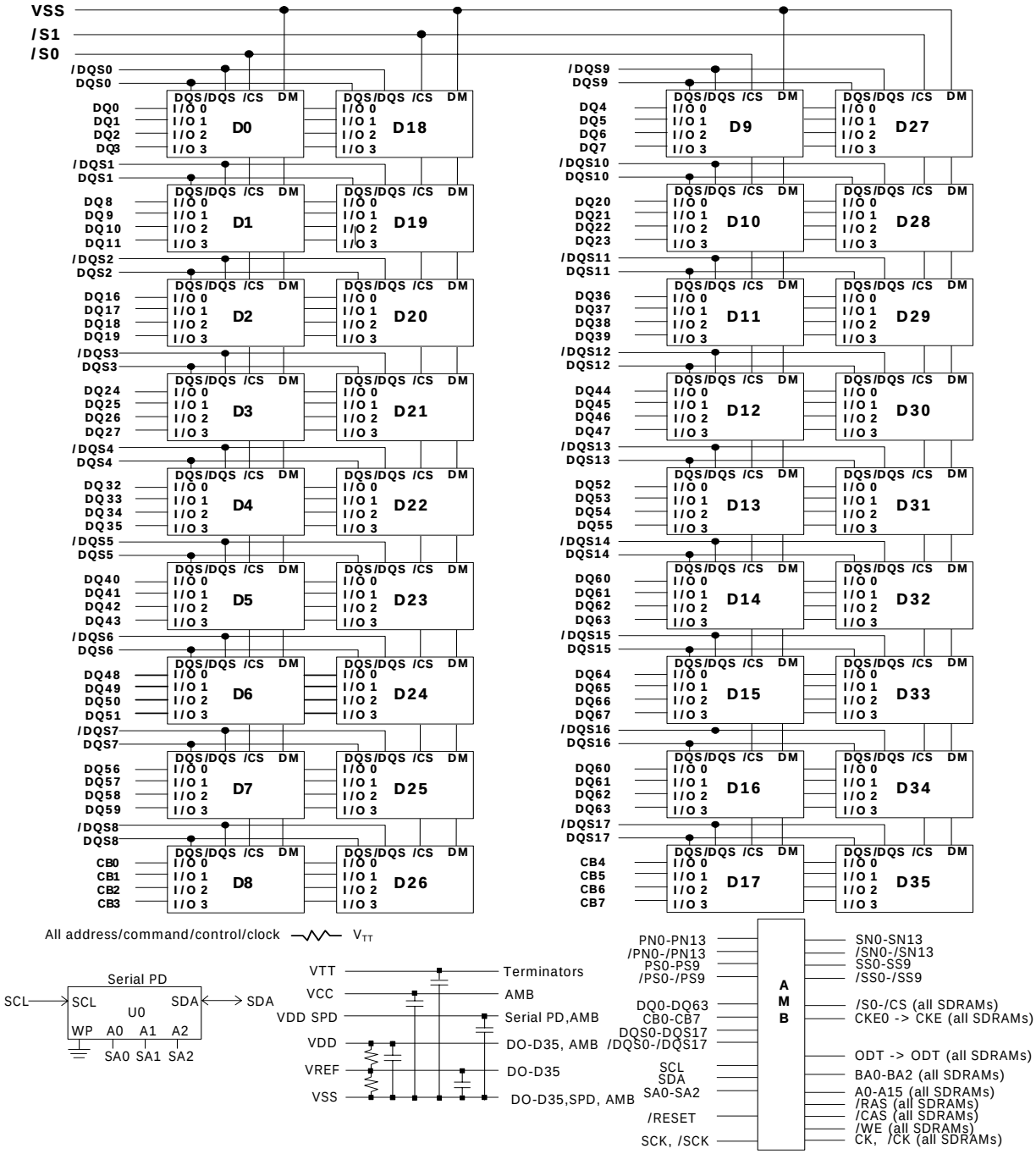
FUNCTIONAL BLOCK DIAGRAM
1GB(128Mbx72) ECC FB-DIMM



Notes :

1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock.

FUNCTIONAL BLOCK DIAGRAM
2GB(256Mbx72) ECC FB-DIMM



Notes :

1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock.

Architecture

Advanced Memory Buffer Pin Description

Pin Name	Pin Description	Count
FB-DIMM Channel Signals		**99**
SCK	System Clock Input, positive line	1
$\overline{\text{SCK}}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{\text{PN}}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{\text{PS}}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{\text{SN}}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{\text{SS}}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1
DDR2 Interface Signals		**175**
DQS[8:0]	Data Strobes, positive lines	9
$\overline{\text{DQS}}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes(x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{\text{DQS}}$[17:9]	Data Strobes(x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A,A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A,BA[2:0]B	Bank Addresses	6
$\overline{\text{RASA}}$,$\overline{\text{RASB}}$	Part of command, with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and $\overline{\text{CS}}$[1:0]	2
$\overline{\text{CASA}}$,$\overline{\text{CASB}}$	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$ and $\overline{\text{CS}}$[1:0]	2
$\overline{\text{WEA}}$,$\overline{\text{WEB}}$	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$ and $\overline{\text{CS}}$[1:0]	2
ODTA,ODTB	On-die Termination Enable	2
CKE[1:0]A,CKE[1:0]B	Clock Enable(one per rank)	4
CS[1:0]A,CS[1:0]B	Chip Select(One per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{\text{CLK}}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to VSS	1
DDRC_C12	DDR Compensation: Resistor connected to VDD	1

Advanced Memory Buffer Pin Description

Pin Name	Pin Description	Count
SPD Bus Interface Signals		**5**
SCL	Serial Presence Detect (SPD) Clock Input	1
$\overline{SDA}$	SPD Data Input / Output	1
SA{2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
Miscellaneous Signals		**163**
PLLTSTO	PLL Clock Observability Output	1
VCCAPLL	Analog VCC for the PLL. Tied with low pass filter to VCC.	1
VSSAPLL	Analog VSS for the PLL. Tied to	1
TEST_pin#	Leave floating on the DIMM	6
TESTLO_pin#	Tie to ground on the DIMM[2]	5
BFUNC	Tie to ground to set functionality as “buffer on DIMM.”	1
$\overline{RESET}$	AMB reset signal	1
NC	No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands.	129
RFU	Reserved for Future Use	18
Power/Ground Signals		**213**
V_{CC}	AMB Core Power(1.5 Volt)	24
V_{CCFBD}	AMB Channel I/O Power(1.5 Volt)	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt)	24
V_{DDSPD}	SPD Power (3.3 Volt)	1
V_{SS}	Ground	156
	Total	**655**

Note:
1. System Clock Signals SCK and $\overline{SCK}$ switch at one half the DRAM CK/ $\overline{CK}$ frequency.
2. TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes on protype DIMMs:
each pin should have a zero ohm resistor pull-down to ground, and an unpopulated resistor pull-up to VCC.
These resistors can be replaced on production DIMMs with a direct connection to ground.

Pin Assignments for the Advanced Memory Buffer(AMB) (Top View) 655-Ball LFBGA 0.8 mm x 0.8 mm pitch

Left Side

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			VSS	DQ26	DQ12	VDD	DQS10	DQ13	VDD	$\overline{DQS1}$	DQ10	VDD	TEST	VDD	VDD
B		VDD	DQS3	$\overline{DQS3}$	VSS	DQ14	$\overline{DQS10}$	VSS	DQ11	DQS1	VSS	DDRC	TESTLO	VDD	VSS
C	VSS	DQS2	DQ18	VSS	DQ4	$\overline{DQS9}$	VSS	DQ15	DQ9	VSS	DQ8	DDRC	VSS	DDRC	DQS17
D	DQ19	$\overline{DQS2}$	VSS	DQ16	DQ24	VSS	DQS9	DQ7	VSS	DQ3	DQS0	VSS	$\overline{DQS8}$	DQS8	VDD
E	DQ21	VSS	DQ17	DQ29	VSS	DQ25	DQ6	VSS	DQ5	DQ1	VSS	DQ0	CB1	VSS	CB2
F	VSS	DQ20	DQ23	VSS	DQ31	DQ27	VSS	TESTLO	TEST	VSS	$\overline{DQS0}$	DQ2	VDD	CB0	CB3
G	$\overline{DQS11}$	DQS11	NC	NC	NC	VSS	DQS12	$\overline{DQS12}$	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	VSS	NC	NC	NC	DQ28	DQ30	VSS	NC	NC	NC	VSS	VDD	VSS	VDD
J	VSS	CLK2	NC	NC	NC	BA1A	VSS	CKE1A	NC	NC	NC	VDD	VSS	VDD	VSS
K	$\overline{CLK2}$	CLK0	NC	NC	NC	VSS	$\overline{WEA}$	$\overline{RASA}$	NC	NC	NC	VSS	VCC	VSS	VCC
L	$\overline{CLK0}$	VSS	NC	NC	NC	A0A	CKE0A	VSS	NC	NC	NC	VCC	VSS	VCC	VSS
M	ODT0A	RFU	NC	NC	NC	$\overline{CASA}$	VSS	BA2A	NC	NC	NC	VSS	VCC	VSS	VCC
N	$\overline{CS1A}$	$\overline{CS0A}$	NC	NC	NC	VSS	BA0A	A10A	NC	NC	NC	VCC	VSS	VCC	VSS
P	A6A	VSS	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	VSS	VCC	VSS	VCC
R	VSS	A8A	NC	NC	NC	A11A	VSS	A5A	NC	NC	NC	VCC	VSS	VCC	VSS
T	A4A	A13A	NC	NC	NC	VSS	A9A	A7A	NC	NC	NC	VSS	VCC	VSS	VCC
U	PN0	$\overline{PN0}$	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	VCCFBD	VSS	VSS
V	PN1	$\overline{PN1}$	VSS	SN0	$\overline{SN0}$	VCCFBD	VSS	VCCFBD	VSS	RFU[a]	RFU[a]	VCCFBD	VSS	VSS	VSS
W	PN2	$\overline{PN2}$	VSS	SN1	$\overline{SN1}$	$\overline{SN3}$	$\overline{SN4}$	$\overline{SN5}$	$\overline{SN13}$	$\overline{SN12}$	$\overline{SN6}$	$\overline{SN7}$	$\overline{SN8}$	$\overline{SN9}$	$\overline{SN10}$
Y	PN3	$\overline{PN3}$	VSS	SN2	$\overline{SN0}$	SN3	SN4	SN6	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	VSS	PN4	$\overline{PN4}$	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB		VSS	$\overline{RESET}$	$\overline{PN5}$	$\overline{PN13}$	RFU[a]	$\overline{PN12}$	$\overline{PN6}$	$\overline{PN7}$	$\overline{PN8}$	$\overline{PN9}$	VSSAPLL	VCCAPLL	$\overline{PN10}$	$\overline{PN11}$
AC			VSS	PN5	PN13	RFU[a]	PN12	PN6	PN7	PN8	PN9	FBDRES	PLLTSTO	PN10	PN11
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

NC= No Connect, RFU= Reserved for Future Use.

Note:
a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

Right Side

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	VDD	TEST	VDD	DQ52	DQS15	VDD	DQ49	DQS6	VDD	DQ48	DQ38	VDD		
B	VDD	TEST	DDRC	VSS	DQS15	DQ53	VSS	DQS6	DQ50	VSS	DQS13	DQS13	VSS	
C	DQS17	VSS	DDRC	DQ54	VSS	DQ55	DQ51	VSS	DQS7	DQ56	VSS	DQ46	DQS14	VDD
D	CB6	CB7	VSS	DQS16	DQ63	VSS	DQ59	DQS7	VSS	DQ36	DQ44	VSS	DQS14	DQ47
E	VSS	CB5	DQS16	VSS	DQ61	DQ57	VSS	DQ58	DQ39	VSS	DQ33	DQ45	VSS	DQ41
F	CB4	VDD	DQ62	DQ60	VSS	TEST	TEST	VSS	DQ37	DQ35	VSS	DQS5	DQ43	VSS
G	TESTLO	RFU	RFU	NC	NC	NC	DQS4	DQS4	VSS	NC	NC	NC	DQS5	DQ40
H	VSS	VDD	VSS	NC	NC	NC	VSS	DQ34	DQ32	NC	NC	NC	VSS	DQ42
J	VDD	VSS	VDD	NC	NC	NC	RASB	VSS	RFU	NC	NC	NC	CLK3	VSS
K	VSS	VCC	VSS	NC	NC	NC	ODT0B	CS1B	VSS	NC	NC	NC	CLK1	CLK3
L	VCC	VSS	VCC	NC	NC	NC	VSS	CASB	WEB	NC	NC	NC	VSS	CLK1
M	VSS	VCC	VSS	NC	NC	NC	CS0B	VSS	BA1B	NC	NC	NC	CKE0B	VSS
N	VCC	VSS	VCC	NC	NC	NC	A0B	A2B	VSS	NC	NC	NC	BA0B	BA2B
P	VSS	VCC	VSS	NC	NC	NC	VSS	A4B	A1B	NC	NC	NC	VSS	CKE1B
R	VCC	VSS	VCC	NC	NC	NC	A6B	VSS	A10B	NC	NC	NC	A3B	VSS
T	VSS	VCC	VSS	NC	NC	NC	A11B	A9B	VSS	NC	NC	NC	A7B	A5B
U	VSS	VCCFBD	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	PS8	PS8
V	VCCFBD	VSS	VCCFBD	VSS	VCCFBD	RFU[a]	RFU[a]	VSS	A13B	A12B	SA2	SA1	PS7	PS7
W	VSS	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	VSS	PS6	PS6
Y	VSS	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	VSS	PS5	PS5
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PS9	PS9	VSS
AB	VSS	SN11	VSS	SCK	TESTLO	PS0	PS1	PS2	PS3	PS4	RFU[a]	VDDSPD	VSS	
AC	RFU	SN11	VSS	SCK	TESTLO	PS0	PS1	PS2	PS3	PS4	RFU[a]	VSS		
	16	17	18	19	20	21	22	23	24	25	26	27	28	29

NC= No Connect, RFU= Reserved for Future Use.

Note:

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

Advanced Memory Buffer(AMB) DRAM Interface Specifications

Please refer to the AMB Specification for all technical requirements

The following specifications for the AMB constitute the subset which is critical for proper operation of the DDR2 SDRAM interface.

Note:
This list is not complete, more information will follow in later revisions of this specification.

Critical AMB Specifications

Symbol	Parameter	Type	VDDQ =1.8V +/-0.1V		Units	Notes
			Min	Max		
tSU	DQ to DQS, DQS setup time (read)	Input		245	ps	1
tH	DQ to DQS, $\overline{DQS}$ hold time (read)	Input		245	ps	1
tDVBamb	AMB Data Valid Before DQS	Output	470		ps	1
tDVAamb	AMB Data Valid After DQS	Output	470		ps	1
tCVBamb	C/A/CNTL Valid Before Clock	Output	1030		ps	1
tCVAamb	C/A/CNTL Valid After Clock	Output	890		ps	1
tDQSCKamb	DQS/$\overline{DQS}$-to-CK/$\overline{CK}$ output skew	Output	-240	240	ps	1
C_{IN}	Input Capacitance(DQ/DQS/$\overline{DQS}$)		2.0	2.5	pF	1

Note 1:
The timing numbers are for example only. Design should be based on the latest component specifications

Basic Functionality

1. Advanced Memory Buffer Overview

The Advanced Memory Buffer reference design complies with the JEDEC FB-DIMM Architecture and Protocol
Specification.

2. Advanced Memory Buffer Functionality

2.1 Advanced Memory Buffer

- Supports channel initialization procedures as defined in the initialization chapter of the FB-DIMM Architecture and Protocol Specification to align the clocks and the frame boundaries verify channel connectivity and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Acts as DRAM memory buffer for all read, write and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FBD Links.

2.2 Transparent Mode for DRAM Test Support

In this mode, the Advanced Memory Buffer will provide lower speed tester access to DRAM pins through the FB-DIMM I/O pins. This allows the tester to send and arbitrary test pattern to the DRAMs. Transparent mode only supports a maximum DRAM frequency equivalent to DDR2 400.

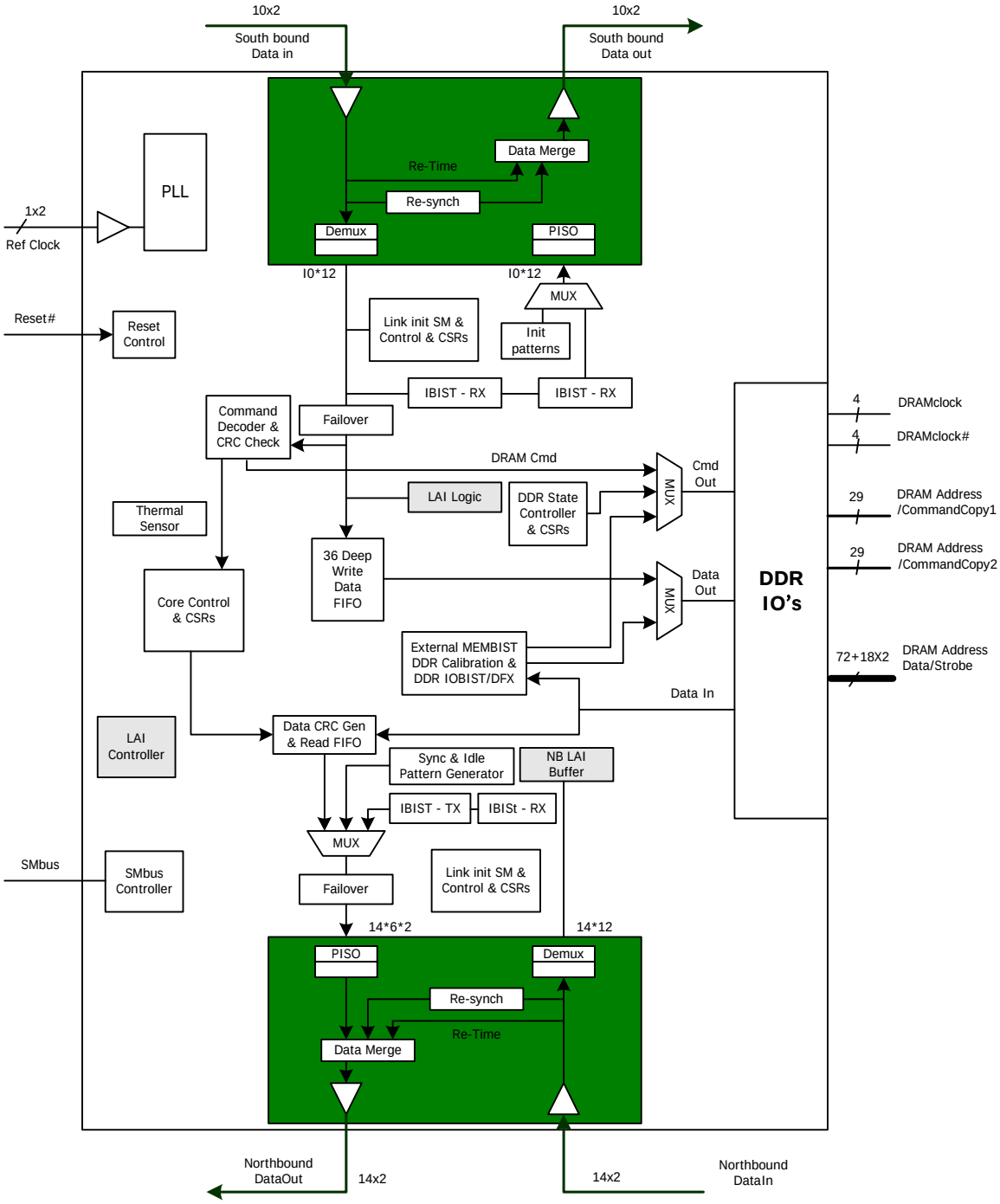
Transparent mode functionality:

- Reconfigure FB-DIMM inputs from differential high speed link receivers to two single ended lower speed receivers(~200 Mhz)
- These inputs directly control DDR2 Command/Address and input data that is replicated to all DRAMs
- Used low speed direct drive FB-DIMM outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

2.3 DDR2 SDRAM

- Supports DDR2 at speeds of 533,667 and 800 MT/s
- Supports 512Mb devices in x4 and x8 configurations
- 72 bit DDR2 SDRAM memory array

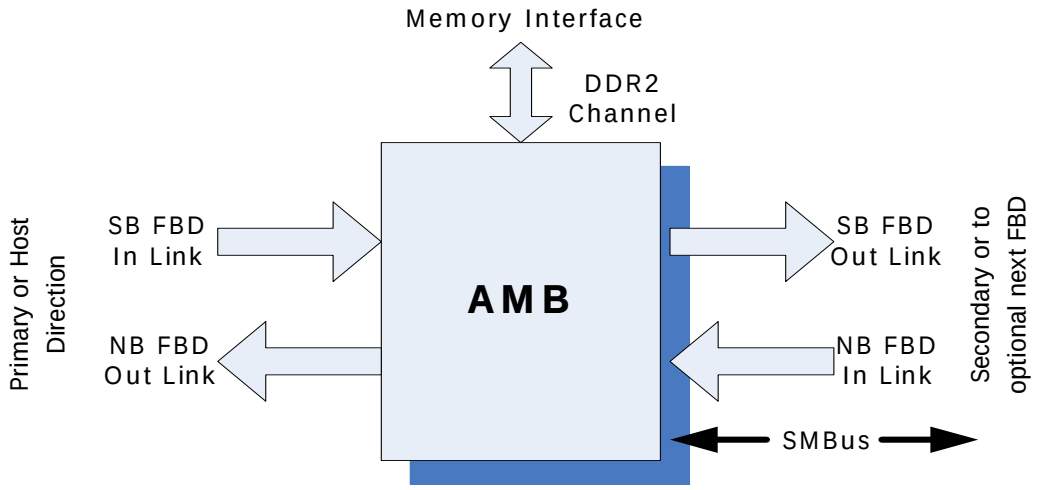
3. Advanced Memory Buffer Block Diagram



Advanced Memory Buffer Block Diagram

4. Interfaces

Below Figure illustrates the AMB and all of its interfaces.They consists of two FB-DIMM links, one DDR2 channel and an SMBus interface. Each FB-DIMM link connects the AMB to a host memory controller or an adjacent FB-DIMM. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM.



Advanced Memory Buffer Interfaces

4.1 FBD High-Speed Differential Point-to-Point Link (at 1.5V) Interfaces

The Advanced Memory Buffer supports one FBD channel consisting of two bidirectional link interfaces using high speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wid and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBD.

The northbound input link is 13 to 14 lanes wide and carries read return data or status information from the next FB-DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

4.2 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals.
There are two copies of address and command signals to support DIMM routing and electrical requirements.
Four transfer bursts are driven on the data and check-bit lines at 800 MHz. Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error. Hardware aligns the read data and check-bits to a single core clock. The Advanced Memory Buffer provides four copies of the command clock phase references(CLK[3:0]) and write data/check-bit strobes(DQSs) for each DRAM nibble.

4.3 SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FB-DIMM link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz. SMBus access to the Advanced Memory Buffer may be a requirement to boot and to set link strength, frequency and other parameters needed to insure robust configurations. It is also required for diagnostic support when the link is down. The SMBus address straps located on the DIMM connector are used by the unique ID.

4.4 FBD Channel Latency

FB-DIMM channel latency is measured from the time a read request is driven on the FB-DIMM channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller. When not using the Variable Read Latency capability, the latency for a specific DIMM on a channel is always equal to the latency for any other DIMM on that channel. However, the latency for each DIMM in a specific configuration with some number of DIMMs installed. As more DIMMs are added to the channel, additional latency is required to read from each DIMM on the channel. Because the channel is based on the point to point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a 4 DIMM channel configuration will have greater idle read latency compared to a 1DIMM channel configuration.The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host. The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

4.5 Peak Theoretical Throughput

An FB-DIMM channel transfers read completion data on the FBD Northbound data connection. 144 bits of data are transferred for every FBD Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lock stepped channels provides a total of 72 bytes of data(64 bytes plus 8 bytes ECC)

The FBD frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FBD channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput as a single DRAM channel.For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.276 GB/sec.

Write data is transferred on the FBD Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every FBD Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of and ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data(64 bytes plus & bytes ECC)

When the FBD frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec.

The total peak theoretical throughput for a single FBD channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the FBD frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a DDR2 533 channel would be 4.267 GB/sec, while the peak theoretical throughput of and FBD -/+533 channel would be 6.4 GB/sec.

5 Hot-add

The FB-DIMM channel does not provide a mechanism to automatically detect and report the addition of a new DIMM south of the currently active last DIMM. It is assumed the system will be notified through some means of the addition of one or more new DIMMs so that specific commands can be sent to the host controller to initialize the newly added DIMM(s) and perform a Hot-add Reset to bring them into the channel timing domain. It should be noted that the power to the DIMM socket must be removed before a “hot-add” DIMM is inserted or removed. Applying or removing the power to a DIMM socket is a system platform function.

6 Hot-remove

In order to accomplish removal of DIMMs the host must perform a Fast Reset sequence targeted at the last DIMM that will be retained on the channel. The Fast Reset re-establish the appropriate last DIMM so that the Southbound
Tx outputs of the last DIMM and the Southbound and Northbound outputs of the DIMMs beyond the last active DIMM are disabled. Once the appropriate outputs are disabled the system can coordinate the procedure to remove power in preparation for physical removal of the DIMM if needed.
It should be noted that the power to the DIMM socket must be removed before a “hot-add” DIMM is inserted or removed. Applying or removing the power to a DIMM socket is a system platform function.

7 Hot-replace

Hot replace of DIMM is accomplished through combing th Hot-Remove and Hot-Add process.

Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Voltage on any pins relative to Vss	V_{IN}, V_{OUT}	- 0.3 V ~ 1.75 V	V	1
Voltage on V_{CC} relative to Vss	V_{CC}	- 0.3 V ~ 1.75 V	V	1
Voltage on V_{DD} relative to Vss	V_{DD}	- 0.5 V ~ 2.3 V	V	1
Voltage on V_{TT} relative to Vss	V_{TT}	- 0.5 V ~ 2.3 V	V	1
Storage Temperature range	T_{STG}	- 55 ^{o}C ~ 100 ^{o}C	^{o}C	1

Note:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING TEMPERATURE RANGE

Parameter	Symbol	Rating	Units	Notes
AMB Component Case temperature Range	T_{CASE}	0 ~ + 110	^{o}C	
DRAM Component Case Temperature Range	T_{CASE}	0 ~ + 95	^{o}C	1,2

Note:

1. Within the DRAM component Case Temperature range all DRAM specification will be supported.
2. If the DRAM case temperature is Above 85^{o}C, the Auto-Refresh command interval has to be reduced from 7.8us of tREFI to 3.9us.

Supply Voltage Levels and DC Operating Conditions.

Parameter	Symbol	Min	Nom	Max	Unit	Note
AMB Supply Voltage	V_{CC}	1.455	1.5	1.575	V	
DRAM Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Termination Voltage	V_{TT}	0.48 x V_{DD}	0.50 x V_{DD}	0.52 x V_{DD}	V	
EEPROM Supply Voltage	V_{DDSPD}	3.0	3.3	3.6	V	
DC Input Logic High(SPD)	V_{IH}(DC)	2.1	-	V_{DDSPD}	V	1
DC Input Logic Low(SPD)	V_{IL}(DC)	-	-	0.8	V	1
DC Input Logic High(RESET)	V_{IH}(DC)	1.0	-	-	V	2
DC Input Logic Low(RESET)	V_{IL}(DC)	-	-	+0.5	V	2
Leakage Current (RESET)	IL	-90	-	+90	uA	2
Leakage Current (Link)	IL	-5	-	+5	uA	3

Note:

1. Applies for SMB and SPD bus Signals.
2. Applies for AMB CMOS Signal RESET.
3. for all other AMB related DC parameters, please refer to the High Speed Differential Link Interface Specifications

Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note
EI Assertion Pass-Thru Timing	tEI Propagad		-	4	clks	-
EI Deassertion Pass-Thru Timing	tEID			bit lock	clks	-
EI Assertion Duration	tEI	100			clks	1
Bit Lock Interval	tBitLock			119	frames	1
Frame Lock Interval	tFrameLock			154	frames	1

Note:
1. Defined in FB-DIMM Architecture and Protocol Spec.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		1
H_{OPR}	Operating humidity(relative)	10 to 90	%	2
T_{STG}	Storage temperature	-50 to +100	^{o}C	2
H_{STG}	Storage humidity(without condensation)	5 to 95	%	2
P_{BAR}	Barometric pressure(operating)	3050	m	2
P_{BAR}	Barometric pressure (storage)	15240	m	2

Note:

1. The designer must meet the case temperature specifications for individual module components.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods

IDD Specification and Conditions

I_{DD} Measurement Conditions

Symbol	Conditions
Idle_0	Idle Current, single or last DIMML0 state, idle (0 BW)Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.
Idle_1	Idle Current, first DIMML0 state, idle (0 BW)Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.
Idle_2	Idle Current, DRAM power downL0 state, idle (0 BW)Primary and Secondary channels enabledCKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.
Active_1	Active PowerL0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.
Active_2	Active Power, data pass throughL0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.
L0s	Channel Standby Average power over 42 frames where the channel enters and exits L0sDRAMs Idle (0 BW). CKE low. Command and address lines floated. Dram clocks active, ODE and CKE driven low.
Training (for AMB spec, not in SPD)	Training Primary and Secondary channels enabled.100% toggle on all channels lanes.DRAMs idle (0 BW).CKE high. Command and address lines stable.DRAM clock active.

IDD Power Supply Currents Specifications.

SAC Timing Parameters by Speed Grade

Power Supply	512MB(HMP564F7FFP8C)			1GB(HMP512F7FFP8C)			2GB(HMP525F7FFP4C)		Unit	Note1)
	Intel	IDT	IDT	Intel	IDT	IDT	Intel	IDT		
	Y5		S5	Y5		S5	Y5			
Icc_Idle_0 @1.5V	2400	2400	3000	2400	2400	3000	2400	2400	mA	
Idd_Idle_0 @1.8V	315	315	315	630	630	630	1260	1260	mA	
Idle_0 Total Power	4.167	4.167	5.067	4.734	4.734	5.634	5.868	5.868	W	
Icc_Idle_1 @1.5V	3100	3100	3875	3100	3100	3875	3100	3100	mA	
Idd_Idle_1 @1.8V	315	315	315	630	630	630	1260	1260	mA	
Idle_1 Total Power	5.217	5.217	6.380	5.784	5.784	6.947	6.918	6.918	W	
Icc_Active_1 @1.5V	3600	3600	4500	3600	3600	4500	3600	3600	mA	
Idd_Active_1 @1.8V	900	900	1035	1800	1800	2070	3600	3600	mA	
Active_1 Total Power	7.020	7.020	8.613	8.640	8.640	10.476	11.880	11.880	W	
Icc_Active_2 @1.5V	3300	3300	4125	3300	3300	4125	3300	3300	mA	
Idd_Active_2 @1.8V	900	900	1035	1800	1800	2070	3600	3600	mA	
Active_2 Total Power	6.570	6.570	8.051	8.190	8.190	9.914	11.430	11.430	W	
Icc_Training @1.5V	4000	4000	5000	4000	4000	5000	4000	4000	mA	
Idd_Training @1.8V	900	900	1035	1800	1800	2070	3600	3600	mA	
Training Total Power	7.620	7.620	9.363	9.240	9.240	11.226	11.480	11.480	W	

Note:

1) Assure that Primary channel Drive strength at 100% with De-emphasis at -6.5dB Secondary channel drive strength at 60% with De-emphasis at -3dB when enabled. Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transferBL=4.10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

SPD specific assumption:Number of devices on the specific DIMM assumed.Termination of command, address, and control is actual value used on the DIMM. ECC or non-ECC as per the specific DIMM.

SPD specifies Delta TAMB power spec specific assumptions: Dual rank x8 ECC DIMM assumed (18 DRAM devices present on DIMM)
Modeled with 27 ohm termination for command, address, and clocks, and 47 ohm termination for control.

ECC DIMM assumed (72 bit data, 14 lanes northbound). AMB specification specifies current for each rail.

Termination Current

Internal signals are terminated on the DIMM through resistors to an external power supply VTT = VDD / 2. Modeled with 30 Ohm termination for clocks, 39 ohm for command / address and 47 ohm for control.

The VTT power supply must be able to source and sink these currents:

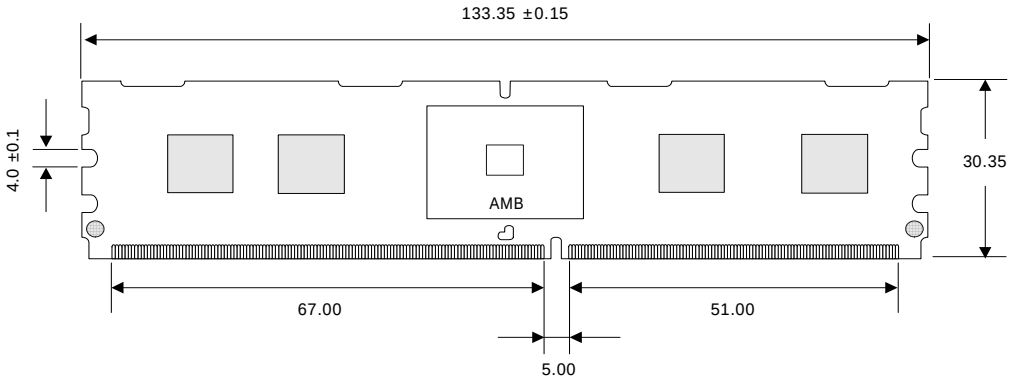
VTT Currents table

Description	Symbol	Typ	Max	Unit
Idle Current, DRAM Power Down (Conditions TBD)	I_{TT1}	-	700	mA
Active Power, 50% DRAM BW (conditions TBD)	I_{TT2}	-	700	mA

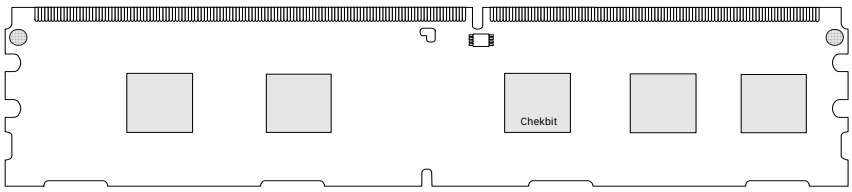
PACKAGE OUTLINE

64Mx72, 512MB Module (1 rank of x8 based DDR2 SDRAMs)
HMP564F7FFP8C

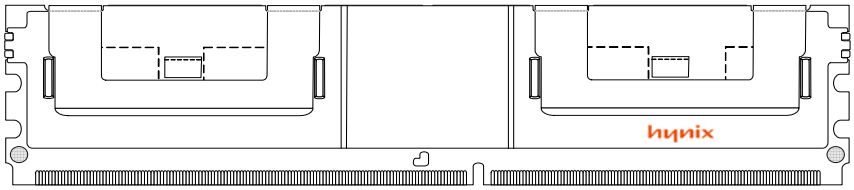
FRONT VIEW



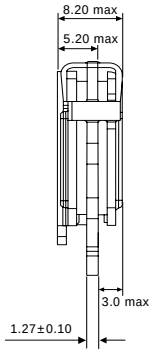
BACK VIEW



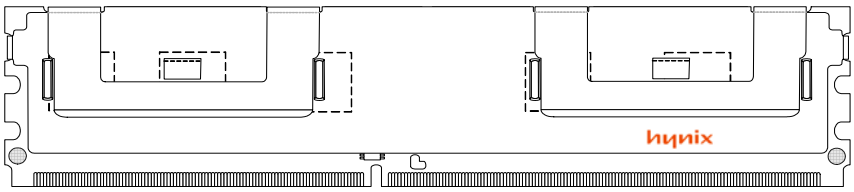
FRONT VIEW WITH HEAT SPREADER



Side



BACK VIEW WITH HEAT SPREADER



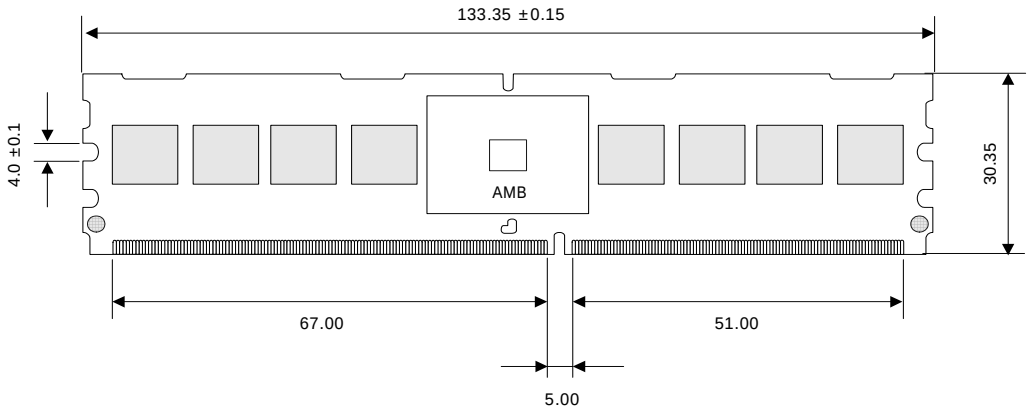
Note 1: All dimensions are typical millimeter scale unless otherwise stated.

PACKAGE OUTLINE

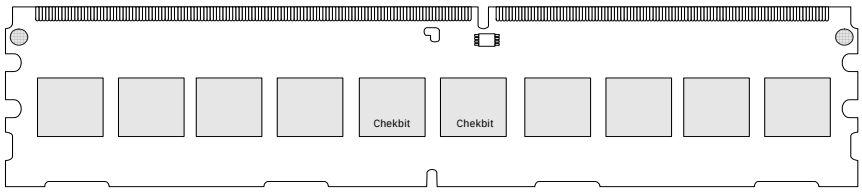
128Mx72, 1GB Module (2 ranks of x8 based DDR2 SDRAMs)

HMP512F7FFP8C

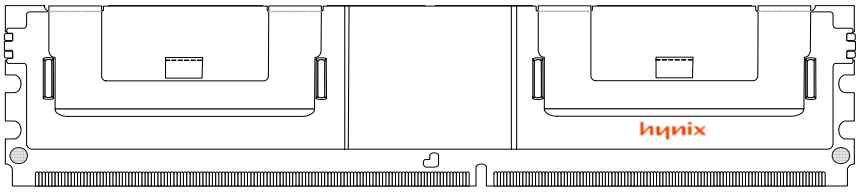
FRONT VIEW



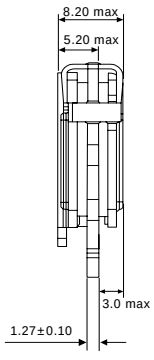
BACK VIEW



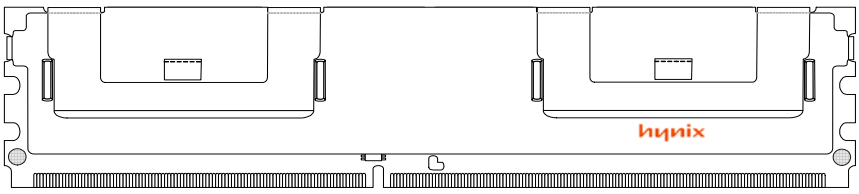
FRONT VIEW WITH HEAT SPREADER



Side



BACK VIEW WITH HEAT SPREADER

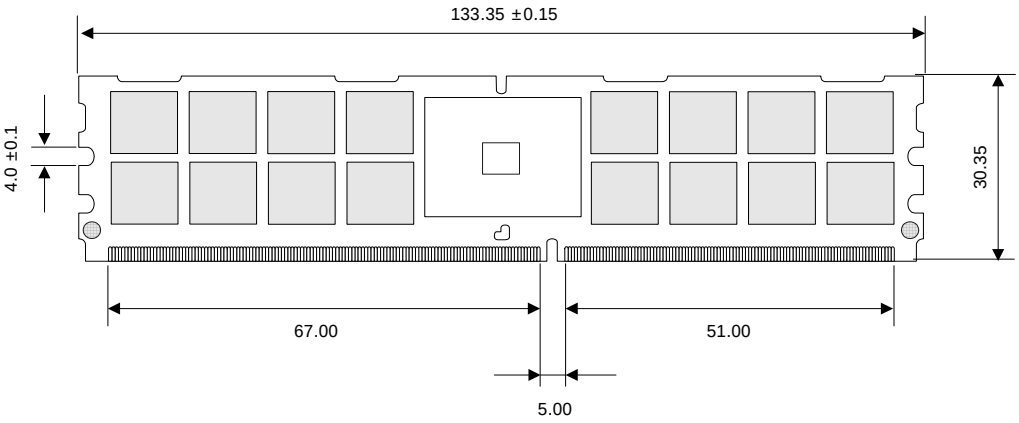


Note 1: All dimensions are typical millimeter scale unless otherwise stated.

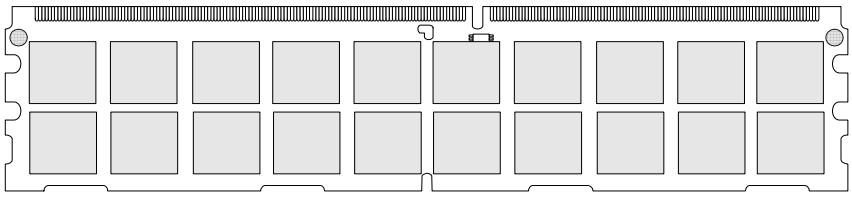
PACKAGE OUTLINE

256Mx72, 2GB Module (2 ranks of x4 based DDR2 SDRAMs)
HMP525F7FFP4C

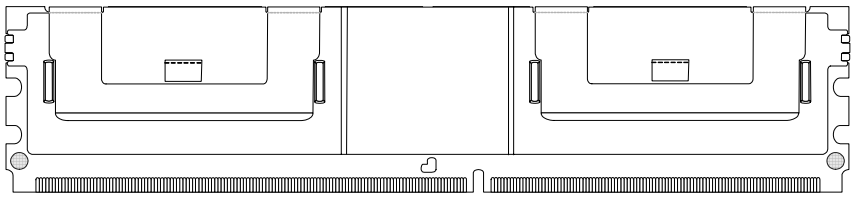
FRONT VIEW



BACK VIEW



FRONT VIEW WITH HEAT SPREADER



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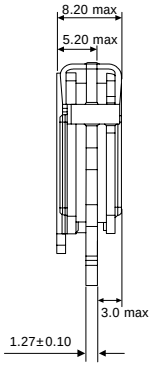
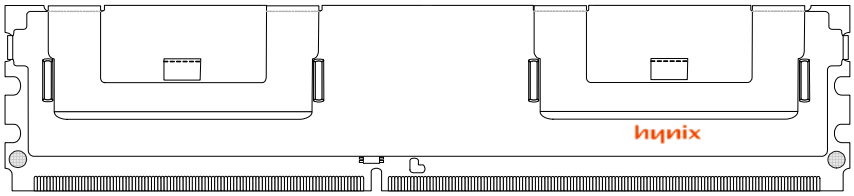


BACK VIEW WITH HEAT SPREADER



Note 1: All dimensions are typical millimeter scale unless otherwise stated.

REVISION HISTORY

Revision	History	Date	Remark
1.0	First Version Release	July. 2008	
1.1	Orddering Info. table revised	Sep. 2008	
1.2	IDD Power spec added	Feb. 2009	