ANALOG DEVICES

LF to 2.7GHz Dual 60dB TruPwr Detector

PRELIMINARY TECHNICAL DATA

AD8364

FEATURES

RMS Measurement of High Crest-Factor Signals
Dual Channel and Difference Outputs ports
Integrated accurately scaled Temperature Sensor
Wide Dynamic Range ±1 dB over 60 dB @2.2 GHz
±0.5 dB Temperature-Stable Linear-in-dB Response
Low log conformance ripple
+5V Operation at 70 mA, –40°C to +85°C
Small footprint 5x5 mm LFCSP Package

APPLICATIONS

Wireless Infrastructure Power Amplifier Linearization/Control
Antenna VSWR Monitor Devices
Gain Control and Measurement
Transmitter Signal Strength Indication (TSSI)
Dual-Channel Wireless Infrastructure Radios

FUNCTIONAL BLOCK DIAGRAM

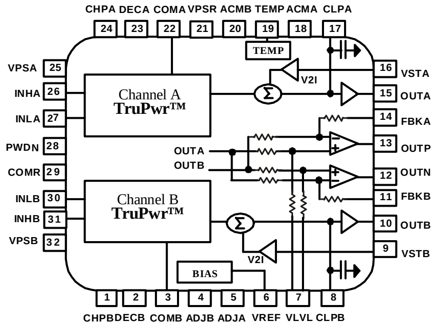


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8364 is a true RMS responding dual channel RF power measurement subsystem for the precise measurement and control of signal power. The flexibility of the AD8364 allows communications systems and instrumentation, such as RF power amplifiers and radio transceiver AGC circuits, to be monitored and controlled with ease. Operating on a single 5V supply, each channel is fully specified for operation up to 2.7GHz, over a dynamic range of 60dB. The AD8364 provides accurately scaled, independent, RMS outputs of both RF measurement channels. A useful measurement difference between the two channels is also made available. On chip channel matching makes the RMS difference output extremely stable with temperature and process variations. The device also includes a useful temperature sensor with an accurately scaled voltage proportional to temperature, specified over the device operating temperature range. The AD8364 can be used with input signals having RMS values from -55dBm to +5dBm, Re: 50Ω and large crest factors with no accuracy degradation.

Integrated in the AD8364 are two well-matched AD8362 channels (*see AD8362 data sheet for more info*). Enhancements include improved temperature performance and reduced log-conformance ripple versus the AD8362. On chip wide bandwidth op-amps are connected to accommodate flexible configurations that support many system solutions.

The device can easily be configured to provide three RMS measurements simultaneously. Linear-in-dB RMS measurements are supplied at **OUTA** and **OUTB**, with conveniently scaled slope of 50mV/dB. The RMS difference between **OUTA** and **OUTB** is available differentially or single-ended at **OUTP** and **OUTN**. An optional voltage applied to **VLVL** provides a common mode reference level to offset **OUTP** and **OUTN** above ground.

Each channel of the AD8364 can independently be used to control separate gain control feedback loops using **VSTA** and **VSTB**. The difference outputs also provide feedback control while providing improved temperature stability through matched channels. Flexibility exists to use either channel as a reference while the other channel is slaved through a feedback loop. RF power amplifier control, VSWR measurements, and transceiver AGC circuits benefit from this feature. In control modes, the opposite polarities of the **OUTP** and **OUTN** outputs allow proportional or complementary gain-control functions, eliminating the need for a board-level sign-inverting amplifier. Feedback pins **FBKA** and **FBKB** allow custom loop regulation in special control system applications and log-slope adjust flexibility. When one channel is slaved off the other, controlling the voltage at **VLVL** will adjust the slaved channel's RMS value, if a power level offset is desired.

The AD8364 is supplied in a 32-lead 5x5mm LFCSP package, for the operating temperature of –40°C to +85°C.

Rev. PrC 1/20/2005

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

AD8364-SPECIFICATIONS

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input *f* ≤ 2.7GHz unless otherwise noted)

Table I.

Parameters	**Conditions**	**Min**	**Typ**	**Max**	**Units**
OVERALL FUNCTION	Channel A and Channel B, CW sine wave input				
SIGNAL INPUT INTERFACE	**INH[A,B]** (Pins 26, 31) **INL[A,B]** (Pins 27, 30)				
Specified Frequency Range		LF		2.7	GHz
DC Common-Mode Voltage			2.5		V
SIGNAL OUTPUT INTERFACE	**OUT[A,B]** (Pins 15,10)				
Small Signal Bandwidth	$C_{LPA} = C_{LPB} \le 300pF$		TBD		MHz
Slew Rate	$C_{LPA} = C_{LPB} \le 300pF$		TBD		V/µS
Settling Time	10%-100% response of -45 dBm to 0 dBm modulated pulse, C_{LPA}=C_{LPB}=Open		TBD		µS
	100%-10% response of 0 dBm to -45 dBm modulated pulse, C_{LPA}=C_{LPB}=Open,		TBD		nS
Wideband Noise	**CLPF** = 1000pF, $f_{SPOT} \le$ 100KHz		TBD		nV/√Hz
MEASUREMENT MODE **450 MHz OPERATION**	**ADJA** = **ADJB** = 0 V, Error Referred to Best Fit Line using Linear Regression @ $P_{INH[A,B]} =$ -40dBm & -20dBm, T_A = 25ºC, Balun = M/A-Com MABAES0054				
± 1 dB Dynamic Range	Pins **OUT[A,B]**		67		dB
	-40ºC < T_A < +85ºC		65		dB
±0.5 dB Dynamic Range	-40ºC < T_A < +85ºC		30		dB
Maximum Input Level	±1dB Error		+15		dBm
Minimum Input Level	±1dB Error		-52		dBm
Slope			50		mV/dB
Intercept			-55		dBm
Output Voltage – High Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -10dBm	TBD	2.2	TBD	V
Output Voltage – Low Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -40dBm	TBD	0.7	TBD	V
Temperature Sensitivity	Deviation from **OUT[A,B]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -40dBm		+/- 0.5		dB
	Deviation from **OUT[P,N]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm, -10dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm, -30dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm, -40dBm		+/- 0.3		dB
Deviation from CW Response	5.5dB Peak-to-RMS Ratio (WCDMA 1 Channel)		TBD		dB
	12dB Peak-to-RMS Ratio (WCDMA 3 Channels)		TBD		dB
	18dB Peak-to-RMS Ratio (WCDMA 4 Channels)		TBD		dB

AD8364-SPECIFICATIONS

Table I.

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input $f \leq$ 2.7GHz unless otherwise noted)

Parameters	Conditions	Min	Typ	Max	Units
InputA to InputB Isolation			30		dB
InputA to OUTB isolation	P_{INHB} = -50dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		TBD		dB
InputB to OUTA isolation (Note 1)	P_{INHA} = -50dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB				
Input Impedance	INHA/INLA, INHB/INLB Differential Drive		210||0.1		Ω||pF
	INHA/INLA, INHB/INLB Single-ended Drive		TBD||TBD		Ω||pF
Input Return Loss	With Recommended Balun		TBD		
MEASUREMENT MODE **880MHz OPERATION**	**ADJA** = **ADJB** = 0 V, Error Referred to Best Fit Line using Linear Regression @ $P_{INH[A,B]}$ = -40dBm & -20dBm, T_A = 25°C, Balun = M/A-Com ETC 1.6-4-2-3				
± 1 dB Dynamic Range	Pins **OUT[A,B]**		59		dB
	-40°C < T_A < +85°C		54		dB
±0.5 dB Dynamic Range	-40°C < T_A < +85°C		49		dB
Maximum Input Level	±1dB Error		-2		dBm
Minimum Input Level	±1dB Error		-61		dBm
Slope			50		mV/dB
Intercept			-61		dBm
Output Voltage – High Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -10dBm	TBD	2.75	TBD	V
Output Voltage – Low Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -40dBm	TBD	1.1	TBD	V
Temperature Sensitivity	Deviation from **OUT[A,B]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -40dBm		+/- 0.5		dB
	Deviation from **OUT[P,N]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -10dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -25dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -40dBm		+/- 0.3		dB
Deviation from CW Response	5.5dB Peak-to-RMS Ratio (WCDMA 1 Channel)		0.2		dB
	12dB Peak-to-RMS Ratio (WCDMA 3 Channels)		0.3		dB
	18dB Peak-to-RMS Ratio (WCDMA 4 Channels)		0.3		dB
InputA to InputB Isolation					dB
InputA to OUTB isolation	P_{INHB} = -50dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		TBD		dB
InputB to OUTA isolation (Note 1)	P_{INHA} = -50dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB				
Input Impedance	INHA/INLA, INHB/INLB Differential Drive		200||0.3		Ω||pF
	INHA/INLA, INHB/INLB Single-ended Drive		TBD||TBD		Ω||pF
Input Return Loss	With Recommended Balun		TBD		

AD8364-SPECIFICATIONS

Table I.

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input $f \leq$ 2.7GHz unless otherwise noted)

Parameters	Conditions	Min	Typ	Max	Units
MEASUREMENT MODE **1880 MHz OPERATION**	**ADJA** = **ADJB** = 0.75 V, Error Referred to Best Fit Line using Linear Regression @ $P_{INH[A,B]}$ = -40dBm & -20dBm, T_A = 25ºC, Balun = M/A-Com ETC 1.6-4-2-3				
± 1 dB Dynamic Range	Pins **OUT[A,B]**		57		dB
	-40ºC < T_A < +85ºC		52		dB
±0.5 dB Dynamic Range	-40ºC < T_A < +85ºC		49		dB
Maximum Input Level	±1dB Error		-5		dBm
Minimum Input Level	±1dB Error		-62		dBm
Slope			50		mV/dB
Intercept			-62		dBm
Output Voltage – High Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -10dBm	TBD	2.5	TBD	V
Output Voltage – Low Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -40dBm	TBD	1.0	TBD	V
Temperature Sensitivity	Deviation from **OUT[A,B]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -40dBm		+/- 0.5		dB
	Deviation from **OUT[P,N]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -10dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -25dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -40dBm		+/- 0.3		dB
Deviation from CW Response	5.5dB Peak-to-RMS Ratio (WCDMA 1 Channel)		TBD		dB
	12dB Peak-to-RMS Ratio (WCDMA 3 Channels)		TBD		dB
	18dB Peak-to-RMS Ratio (WCDMA 4 Channels)		TBD		dB
InputA to InputB Isolation					dB
InputA to OUTB isolation	P_{INHB} = -50dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		TBD		dB
InputB to OUTA isolation (Note 1)	P_{INHA} = -50dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB				
Input Impedance	INHA/INLA, INHB/INLB Differential Drive		167||0.14		Ω||pF
	INHA/INLA, INHB/INLB Single-ended Drive		TBD||TBD		Ω||pF
Input Return Loss	With Recommended Balun		TBD		
MEASUREMENT MODE **2.14 GHz OPERATION**	**ADJA** = **ADJB** = 1.02 V, Error Referred to Best Fit Line using Linear Regression @ $P_{INH[A,B]}$ = -40dBm & -20dBm, T_A = 25ºC, Balun = M/A-Com ETC 1.6-4-2-3				
± 1 dB Dynamic Range	Pins **OUT[A,B]**		56		dB
	-40ºC < T_A < +85ºC		51		dB
±0.5 dB Dynamic Range	-40ºC < T_A < +85ºC		45		dB
Maximum Input Level	±1dB Error		-2		dBm
Minimum Input Level	±1dB Error		-58		dBm

AD8364-SPECIFICATIONS

Table I.

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input *f* ≤ 2.7GHz unless otherwise noted)

Parameters	Conditions	Min	Typ	Max	Units
Slope			50		mV/dB
Intercept			-58		dBm
Output Voltage – High Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -10dBm	TBD	2.3	TBD	V
Output Voltage – Low Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -40dBm	TBD	0.85	TBD	V
Temperature Sensitivity	Deviation from **OUT[A,B]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -40dBm		+/- 0.5		dB
	Deviation from **OUT[P,N]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -10dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -25dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -40dBm		+/- 0.3		dB
Deviation from CW Response	5.5dB Peak-to-RMS Ratio (WCDMA 1 Channel)		0.2		dB
	12dB Peak-to-RMS Ratio (WCDMA 3 Channels)		0.3		dB
	18dB Peak-to-RMS Ratio (WCDMA 4 Channels)		0.3		dB
InputA to InputB Isolation					dB
InputA to OUTB isolation	P_{INHB} = -50dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		TBD		dB
InputB to OUTA isolation (Note 1)	P_{INHA} = -50dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB				
Input Impedance	INHA/INLA, INHB/INLB Differential Drive		150||1.9		Ω||pF
	INHA/INLA, INHB/INLB Single-ended Drive		TBD||TBD		Ω||pF
Input Return Loss	With Recommended Balun		TBD		
MEASUREMENT MODE **2.5 GHz OPERATION**	**ADJA** = **ADJB** = 1.14 V, Error Referred to Best Fit Line using Linear Regression @ $P_{INH[A,B]}$ = -40dBm & -20dBm, T_A = 25°C, Balun = M/A-Com ETC 1.6-4-2-3				
± 1 dB Dynamic Range	Pins **OUT[A,B]**		58		dB
	-40°C < T_A < +85°C		52		dB
±0.5 dB Dynamic Range	-40°C < T_A < +85°C		42		dB
Maximum Input Level	±1dB Error		5		dBm
Minimum Input Level	±1dB Error		-53		dBm
Slope			50		mV/dB
Intercept			-53		dBm
Output Voltage – High Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -10dBm	TBD	2.1	TBD	V
Output Voltage – Low Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -40dBm	TBD	0.65	TBD	V

AD8364-SPECIFICATIONS

Table I.

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input *f* ≤ 2.7GHz unless otherwise noted)

Parameters	Conditions	Min	Typ	Max	Units
Temperature Sensitivity	Deviation from **OUT[A,B]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -40dBm		+/- 0.5		dB
	Deviation from **OUT[P,N]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -10dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -25dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -40dBm		+/- 0.3		dB
Deviation from CW Response	5.5dB Peak-to-RMS Ratio (WCDMA 1 Channel)		TBD		dB
	12dB Peak-to-RMS Ratio (WCDMA 3 Channels)		TBD		dB
	18dB Peak-to-RMS Ratio (WCDMA 4 Channels)		TBD		dB
InputA to InputB Isolation					dB
InputA to OUTB isolation	P_{INHB} = -50dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		TBD		dB
InputB to OUTA isolation (Note 1)	P_{INHA} = -50dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB				
Input Impedance	INHA/INLA, INHB/INLB Differential Drive		150||1.7		Ω||pF
	INHA/INLA, INHB/INLB Single-ended Drive		TBD||TBD		Ω||pF
Input Return Loss	With Recommended Balun		TBD		
MEASUREMENT MODE **2.7 GHz OPERATION**	**ADJA** = **ADJB** = 1.18 V, Error Referred to Best Fit Line using Linear Regression @ $P_{INH[A,B]}$ = -40dBm & -20dBm, T_A = 25ºC, Balun = M/A-Com ETC 1.6-4-2-3				
± 1 dB Dynamic Range	Pins **OUT[A,B]**		60		dB
	-40ºC < T_A < +85ºC		55		dB
±0.5 dB Dynamic Range	-40ºC < T_A < +85ºC		45		dB
Maximum Input Level	±1dB Error		10		dBm
Minimum Input Level	±1dB Error		-50		dBm
Slope			49		mV/dB
Intercept			-51		dBm
Output Voltage – High Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -10dBm	TBD	2.0	TBD	V
Output Voltage – Low Power In	Pins **OUT[A,B]** @ $P_{INH[A,B]}$ = -40dBm	TBD	0.5	TBD	V
Temperature Sensitivity	Deviation from **OUT[A,B]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -10dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm		+/- 0.5		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -40dBm		+/- 0.5		dB

AD8364-SPECIFICATIONS

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input $f \le$ 2.7GHz unless otherwise noted)

Table I.

Parameters	**Conditions**	**Min**	**Typ**	**Max**	**Units**
	Deviation from **OUT[P,N]** @ 25°C				
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -10dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -25dBm		+/- 0.3		dB
	-40°C<T_A<85°C; $P_{INH[A,B]}$ = -25dBm, -40dBm		+/- 0.3		dB
Deviation from CW Response	5.5dB Peak-to-RMS Ratio (WCDMA 1 Channel)		TBD		dB
	12dB Peak-to-RMS Ratio (WCDMA 3 Channels)		TBD		dB
	18dB Peak-to-RMS Ratio (WCDMA 4 Channels)		TBD		dB
InputA to InputB Isolation			TBD		dB
InputA to OUTB isolation	P_{INHB} = -50dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		TBD		dB
InputB to OUTA isolation (Note 1)	P_{INHA} = -50dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB				
Input Impedance	INHA/INLA, INHB/INLB Differential Drive		200||0.08		Ω||pF
	INHA/INLA, INHB/INLB Single-ended Drive		TBD||TBD		Ω||pF
Input Return Loss	With Recommended Balun		TBD		
OUTPUT INTERFACE	Pin **OUTA** and **OUTB**				
Voltage Range Min	$R_L \ge 200\Omega$ to ground		0.09		V
Voltage Range Max	$R_L \ge 200\Omega$ to ground		V_S-0.05		V
Source/Sink Current	**OUTA** & **OUTB** held at V_S/2, to 1% change		70		mA
SET-POINT INPUT	Pin **VSTA** and **VSTB**				
Voltage Range	Law conformance error ≤ ±1dB	0.5		3.75	V
Input Resistance			68		KΩ
Logarithmic Scale Factor	f = 450MHz??, -40°C ≤ T_A ≤ +85°C		50		mV/dB
Logarithmic Intercept	f = 450MHz??, -40°C ≤ T_A ≤ +85°C, Re: 50Ω		-55		dBm
Temperature Sensitivity	Pin = -10dBm, slope and intercept errors combined		TBD		dB/°C
DIFFERENCE OUTPUT	Pin **OUTP** and **OUTN**				
Voltage Range Min	$R_L \ge 200\Omega$ to ground		0.1		V
Voltage Range Max	$R_L \ge 200\Omega$ to ground		V_S-0.15		V
Source/Sink Current	**OUTP** and **OUTN** held at V_S/2, to 1% change		70		mA
Small Signal Bandwidth	$C_L \le$ 300pF		TBD		MHz
Slew Rate	$C_L \le$ 300pF		TBD		V/µS
Wideband Noise	**CLPF** = 1000pF, $f_{SPOT} \le$ 100KHz		TBD		nV/√Hz
Offset	**OUTB**=**OUTA**=open, **OUTP**=**FBKA**=open, **VLVL**=open		TBD		mV
DIFFERENCE LEVEL ADJUST	Pin **VLVL**				
Voltage Range	**OUT[P,N]**=**FBK[A,B}** (through Cap)	0		TBD	V
OUT[P,N] Voltage Range	**OUT[P,N]**=**FBK[A,B}** (through Cap)	0		TBD	V
Input Resistance			1		KΩ

AD8364-SPECIFICATIONS

Table I.

(V_S =VPSA=VPSB=VPSR =5V, T_A=25°C, Chan A_{FREQ} = Chan B_{FREQ}, VLVL = VREF, VST[A,B] = OUT[A,B], OUT[P,N] = FBK[A,B], differential input via Balun[1], CW input $f \leq$ 2.7GHz unless otherwise noted)

Parameters	Conditions	Min	Typ	Max	Units
TEMPERATURE COMPENSATION	Pin **ADJA** and **ADJB**				
Input Voltage Range		0		2.5	V
Input Resistance			<1		MΩ
VOLTAGE REFERENCE	Pin **VREF**				
Output Voltage	RF in = -55 dBm		2.5		V
Temperature Sensitivity	$-40°C \leq T_A \leq +85°C$		0.22		mV/°C
Current Limit Source/Sink	Into a grounded load /to 1% change		18/6		mA
TEMPERATURE REFERENCE	Pin **TEMP**				
Output Voltage	T_A=25°C, R_L=10KΩ		0.6		V
Temperature Slope	$-40°C \leq T_A \leq +85°C$, R_L=10KΩ		2		mV/°C
Current Source/Sink	T_A=25°C to 1% change		1.6/2		mA
POWER DOWN INTERFACE	Pin **PWDN**				
Logic Level to Enable	Logic LO enables			1	V
Logic Level to Disable	Logic HI disables	3			V
Input Current	Logic HI **PWDN** = 5V		100		µA
	Logic LO **PWDN** = 0V		<1		µA
Enable Time	**PWDN** LO to **OUTA/OUTB** at 100% final value, $C_{LPA/B}$=Open, $C_{HPA/B}$=10nF RF in = 0 dBm		2		µS
Disable Time	**PWDN** HI to **OUTA/OUTB** at 10% final value, $C_{LPA/B}$=Open, $C_{HPA/B}$=10nF, RF in = 0 dBm		1.6		µS
POWER INTERFACE	Pin **VPS[A,B], VPSR**				
Supply Voltage		4.5		5.5	V
Quiescent Current	RF in = -55 dBm, Vs =5V		72	TBD	mA
Supply Current	**PWDN** enabled, Vs =5V		500		µA

Notes (not complete)

1. See Figure/TPC X for a plot of isolation versus frequency for a ± 1 dB error
2. See Figure/TPC X
3. Best Fit Line, Linear Regression

ABSOLUTE MAXIMUM RATINGS

Table 2. ADL5306 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage **VPSA**, **VPSB**, **VPSR**	5.5V
PWDN, **VSTA**, **VSTB**, **ADJA**, **ADJB**	0V, 5.5V
Input power (Re: 50Ω)	TBD dBm
Internal Power Dissipation	TBDmW
θ_{JA}	TBD C/W
Maximum Junction Temperature	+125° C.
Operating Temperature Range	-40° C to +85° C
Storage Temperature Range	-65° C to +150° C
Lead Temperature Range (Soldering 60 sec	+300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

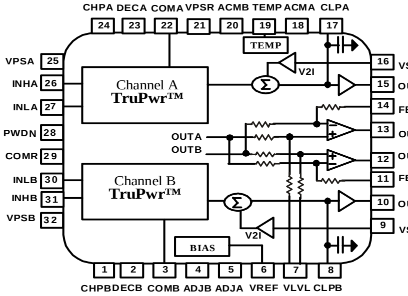


Figure 2. AD8364 Pinout

Table 3. Pin Function Descriptions

Pin	Name	Description	Equiv. Circuit
1	**CHPB**	Connect to common via a capacitor to determine 3 dB point of Channel B input signal high-pass filter.	
2,23	**DECA, DECB**	Decoupling terminals for **INHA/INLA and INHB/INLB**. Connect to common via a large capacitance to complete input circuit.	
3, 22, 29	**COMB, COMA COMR**	Input system common connection. Connect via low impedance to system common.	
4, 5	**ADJB, ADJA**	Temperature compensation for Channel B and Channel A. An external voltage is connected to these pins to improve temperature drift. This voltage can be derived from Vref, that is, connect a resistor from Vref to ADJ[A,B] and another resistor from ADJ[A,B] to ground. The value of these resistors will change with frequency.	
6	**VREF**	General-purpose reference voltage output of 2.5V.	
7	**VLVL**	Reference level input for **OUTP** and **OUTN**. (Usually connected to **VREF** through a voltage divider or left open).	
8, 17	**CLPB, CLPA**	Channel B and Channel A connection for loop filter integration (averaging) capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to improve loop stability and response time.	
9	**VSTB**	The voltage applied to this pin sets the decibel value of the required RF input voltage to Channel B that results in zero current out of the loop integrating capacitor pin, **CLPB**.	
10	**OUTB**	Channel B output of error amplifier. In measurement mode, normally connected directly to **VSTB**.	
11	**FBKB**	Feedback through 1KΩ to the negative terminal of the integrated op-amp driving **OUTN**.	
12	**OUTN**	Output of differencing op-amp. In measurement mode, normally connected directly to **FBKB**.	
13	**OUTP**	Output of differencing op-amp. In measurement mode, normally connected directly to **FBKA**.	
14	**FBKA**	Feedback through 1KΩ to the negative terminal of the integrated op-amp driving **OUTP**.	
15	**OUTA**	Channel A output of error amplifier. In measurement mode, normally connected directly to **VSTA**.	
16	**VSTA**	The voltage applied to this pin sets the decibel value of the required RF input voltage to Channel A that results in zero current out of the loop integrating capacitor pin, **CLPA**.	
18, 20	**ACMA, ACMB**	Analog common for channel A &B. Connect via low impedance to common.	
21,25,32	**VPSR, VPSA VPSB**	Supply for the input system of channel A & B. Supply for the internal references. Connect to +5 V power supply.	
19	**TEMP**	Temperature sensor output.	
24	**CHPA**	Connect to common via a capacitor to determine 3 dB point of Channel A input signal high-pass filter.	
26, 27	**INHA, INLA**	Channel A “High” and “Low” RF signal input terminal.	Circuit A
28	**PWDN**	Disable/Enable control input. Apply logic high voltage to shut AD8364 down.	
30, 31	**INLB, INHB**	Channel B “Low” and “High” RF signal input terminal.	Circuit A
Under Package	**Exposed Paddle**	The exposed paddle on the under side of the package should be soldered to a low thermal and electrical impedance ground plane.	

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V, T = +25°C, −40°C, +85°C; $C_{LPA/B}$ = OPEN. Colors: +25°C → Black; −40°C → Blue; +85°C → Red

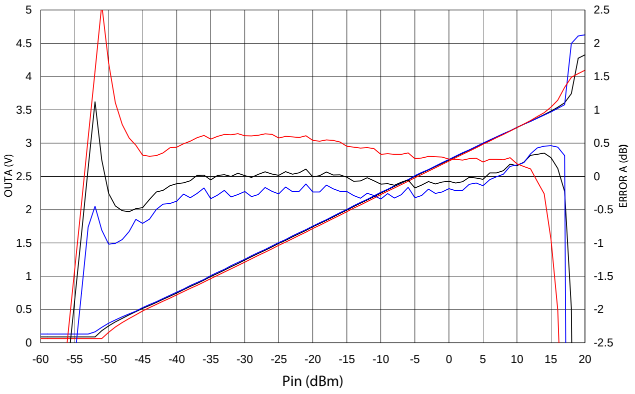


*Figure 3.**OUT[A,B]** V_{OUT} and Log Conformance vs. Input Amplitude at 450 MHz, Typical Device, $T_{ADJA/B}$ = 0V, Sine Wave, Differential Drive*

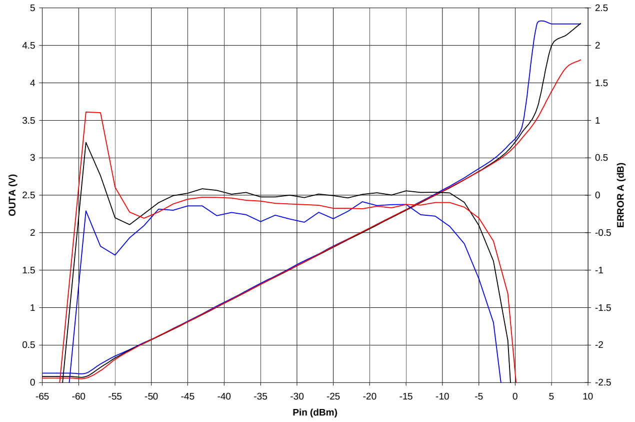


*Figure 4. **OUT[A,B]** V_{OUT} and Log Conformance vs. Input Amplitude at 880 MHz, Typical Device, $T_{ADJA/B}$ = 0V, Sine Wave, Differential Drive*

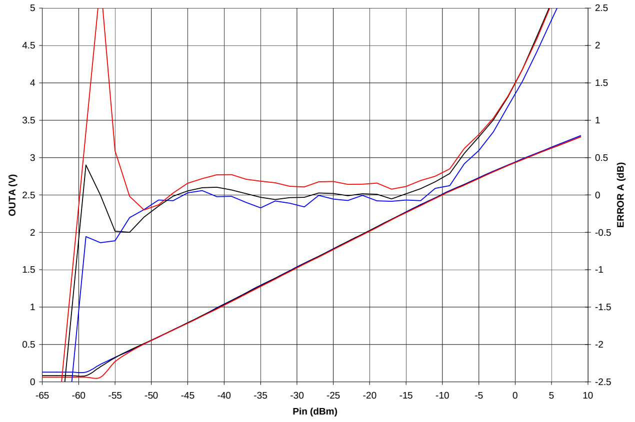


*Figure 5. **OUT[A,B]** V_{OUT} and Log Conformance vs. Input Amplitude at 1.88 GHz, Typical Device, $T_{ADJA/B}$ = 0.75V , Sine Wave, Differential Drive*

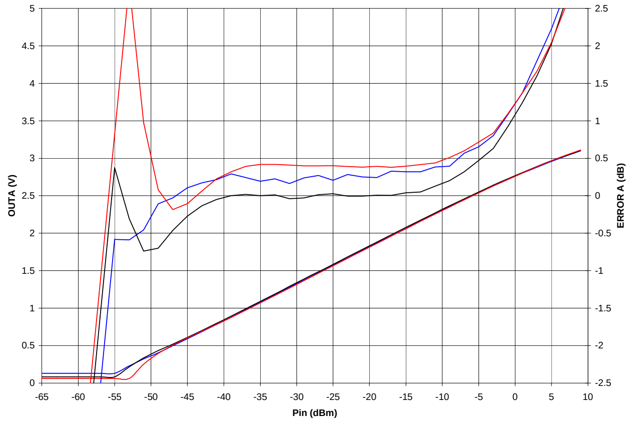


*Figure 6. **OUT[A,B]** V_{OUT} and Log Conformance vs. Input Amplitude at 2.14 GHz, Typical Device, $T_{ADJA/B}$ =1.02V , Sine Wave, Differential Drive*

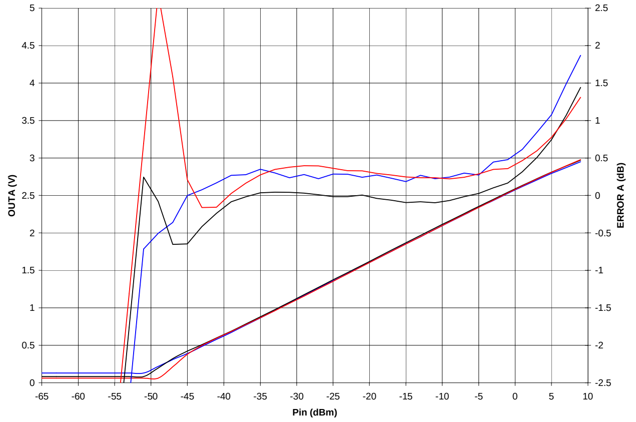


*Figure 7. **OUT[A,B]** V_{OUT} and Log Conformance vs. Input Amplitude at 2.5 GHz, Typical Device, $T_{ADJA/B}$ =1.14V , Sine Wave, Differential Drive*

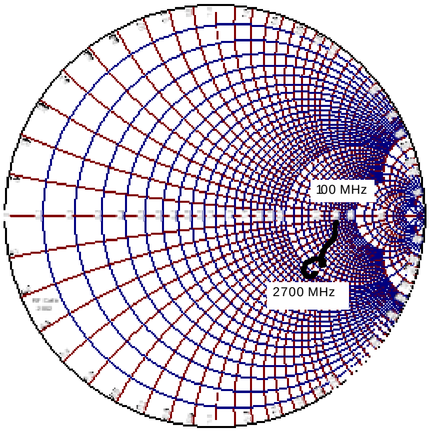


Figure 8. Differential Input Impedance (S11) vs. Frequency; Zo = 50Ω

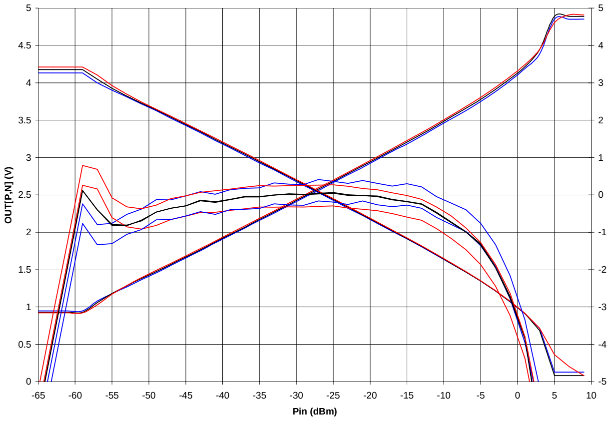


Figure 9. ***OUT[P,N]*** *V_{OUT} and Log Conformance vs. Input Amplitude at 450 MHz, With B input held at -25dBM and A input swept, Typical Device, $T_{ADJA/B}$=0V, Sine Wave, Differential Drive*

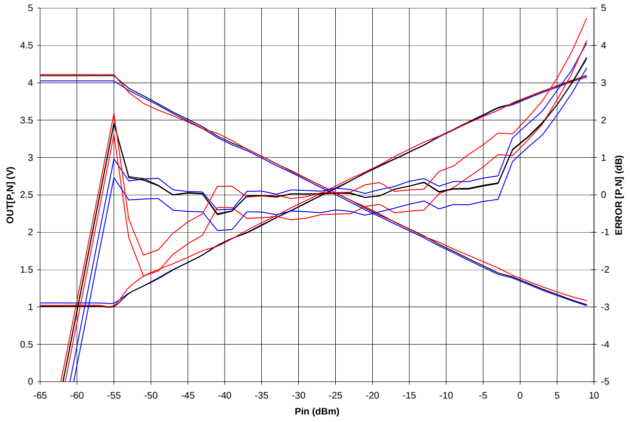


Figure 12. ***OUT[P,N]*** *V_{OUT} and Log Conformance vs. Input Amplitude at 2.14 GHz, With B input held at -25dBM and A input swept, Typical Device, $T_{ADJA/B}$=1.02V, Sine Wave, Differential Drive*

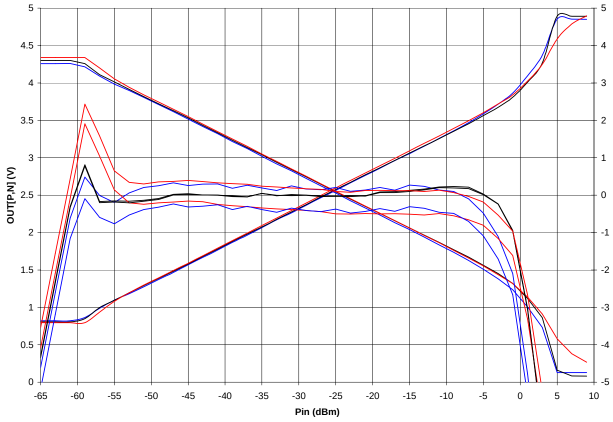


Figure 10. ***OUT[P,N]*** *V_{OUT} and Log Conformance vs. Input Amplitude at 880 MHz, With B input held at -25dBM and A input swept, Typical Device, $T_{ADJA/B}$=0V, Sine Wave, Differential Drive*

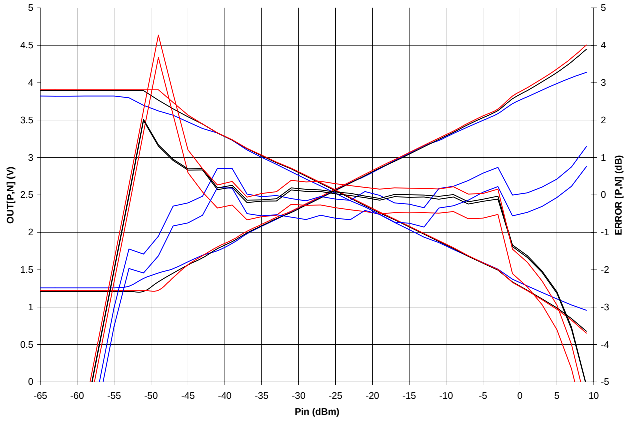


Figure 13. ***OUT[P,N]*** *V_{OUT} and Log Conformance vs. Input Amplitude at 2.5 GHz, With B input held at -25dBM and A input swept, Typical Device, $T_{ADJA/B}$=1.14V, Sine Wave, Differential Drive*

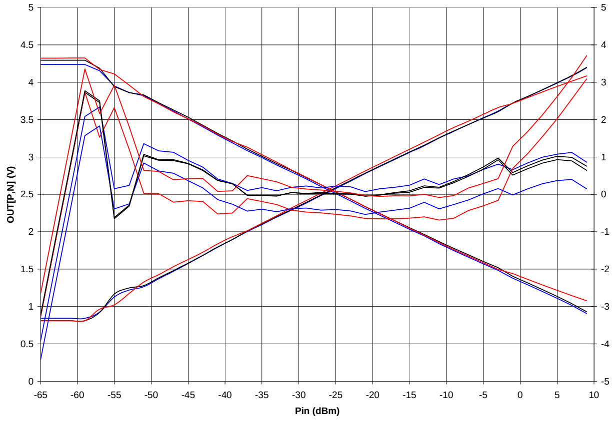


Figure 11. ***OUT[P,N]*** *V_{OUT} and Log Conformance vs. Input Amplitude at 1.88 GHz, With B input held at -25dBM and A input swept, Typical Device, $T_{ADJA/B}$=0.75V, Sine Wave, Differential Drive*

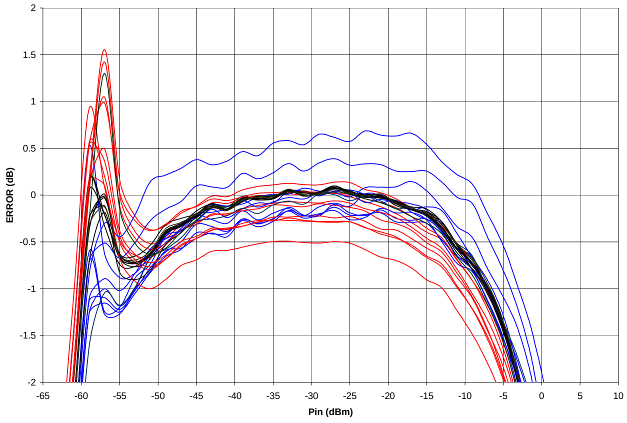


Figure 14. Distribution of ***OUT[A,B]*** *Error over Temperature after Ambient Normalization vs. Input Amplitude for 10 Devices, Frequency=450 MHz, $T_{ADJA/B}$ = 0V, Sine Wave, Differential Drive*

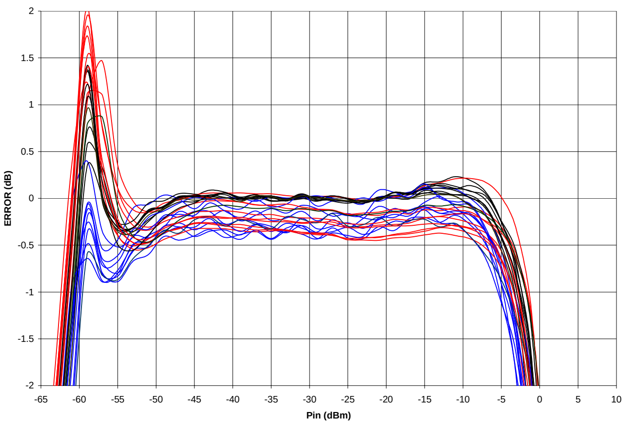


*Figure 15. Distribution of **OUT[A,B]** Error at Temperature after Ambient Normalization vs. Input Amplitude for 10 Devices, Frequency= 880 MHz, $T_{ADJA/B}$ = 0V , Sine Wave, Differential Drive*

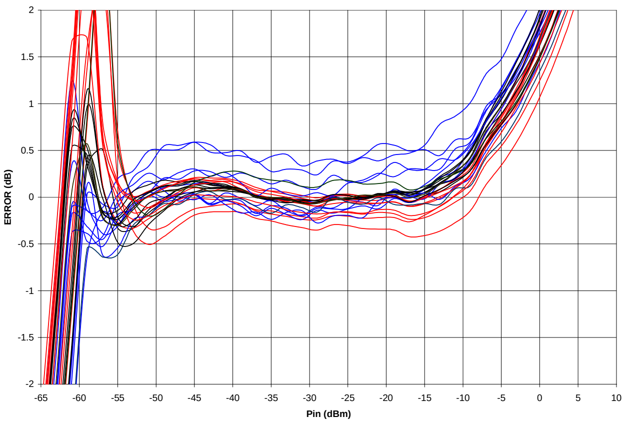


*Figure 16. Distribution of **OUT[A,B]** Error at Temperature after Ambient Normalization vs. Input Amplitude for 10 Devices, Frequency=1.88 GHz, $T_{ADJA/B}$ = 0.75V, Sine Wave, Differential Drive*

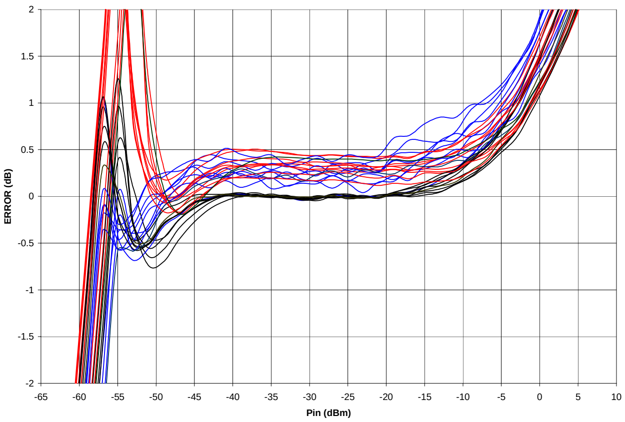


*Figure 17. Distribution of **OUT[A,B]** Error at Temperature after Ambient Normalization vs. Input Amplitude for 10 Devices, Frequency=2.14 GHz, $T_{ADJA/B}$ = 1.02V , Sine Wave, Differential Drive*

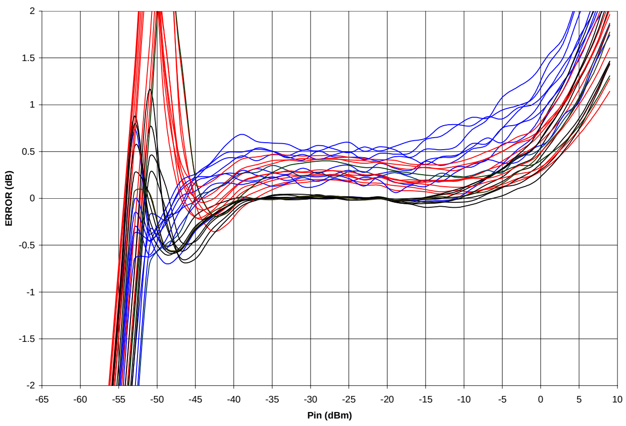


*Figure 18. Distribution of **OUT[A,B]** Error at Temperature after Ambient Normalization vs. Input Amplitude for 10 Devices, Frequency=2.5 GHz, $T_{ADJA/B}$ = 1.14V , Sine Wave, Differential Drive*

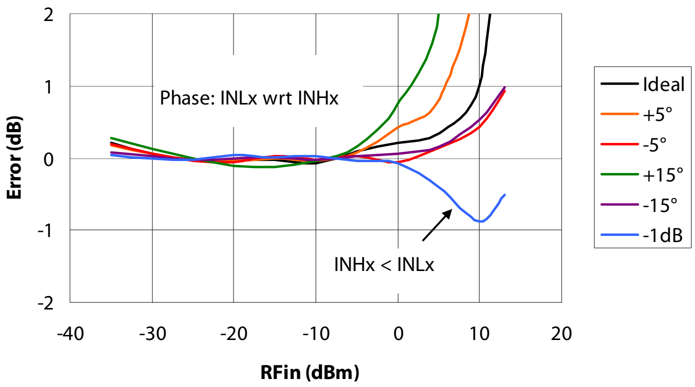


Figure 19. V_{OUT} and Log Conformance vs. Input Amplitude for magnitude balance of 0 dB, and -1 dB and phase balance of 0 deg, ±5 deg, ±15 deg at 450 MHz, Typical Device, $T_{ADJA/B}$ = 0V, Sine Wave, Differential Drive

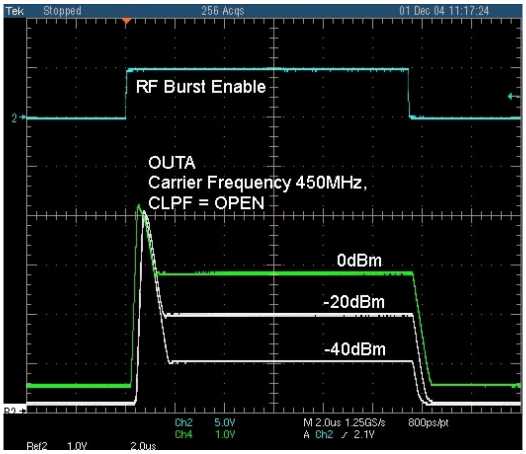


Figure 20. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA/B = 0

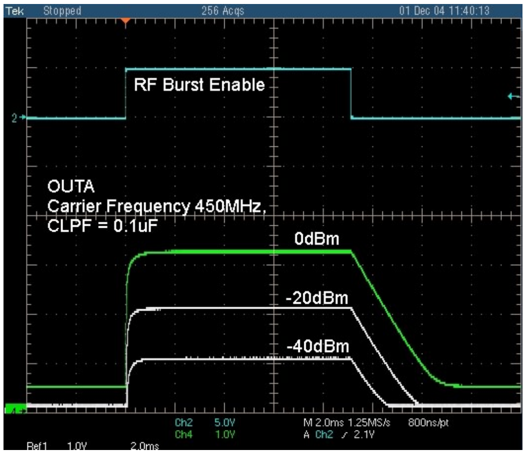


Figure 21. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA/B = 0.1 μF

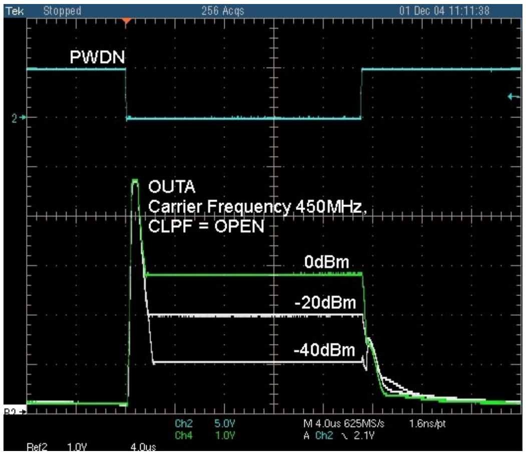


Figure 22. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = 0

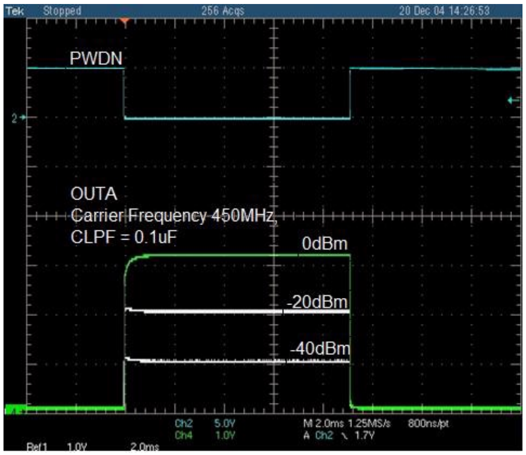


Figure 23. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = 0.1 μF, CHPA = 10nF

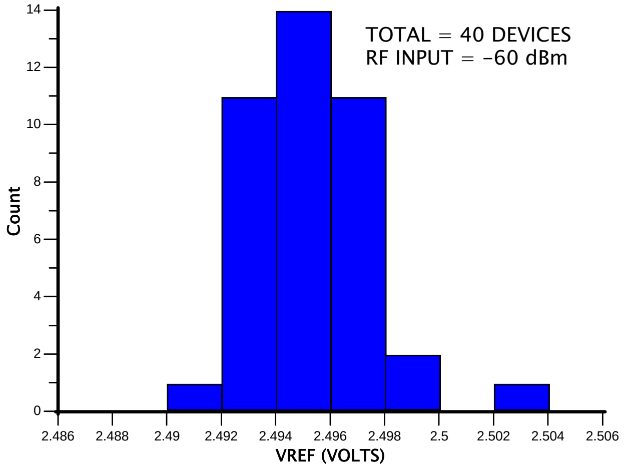


Figure 24. Distribution of VREF for 40 Devices

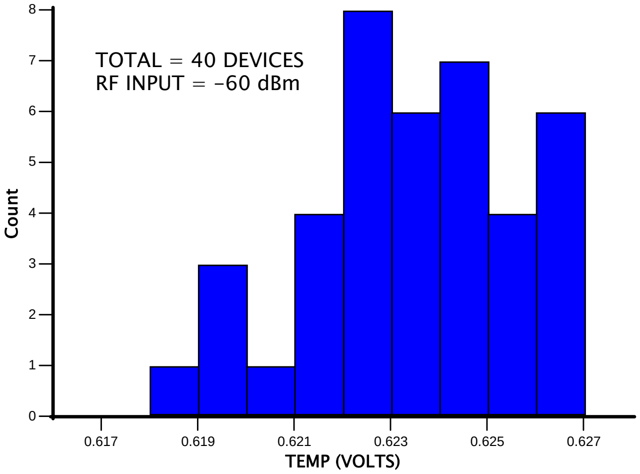


Figure 25. Distribution of TEMP voltage for 40 Devices

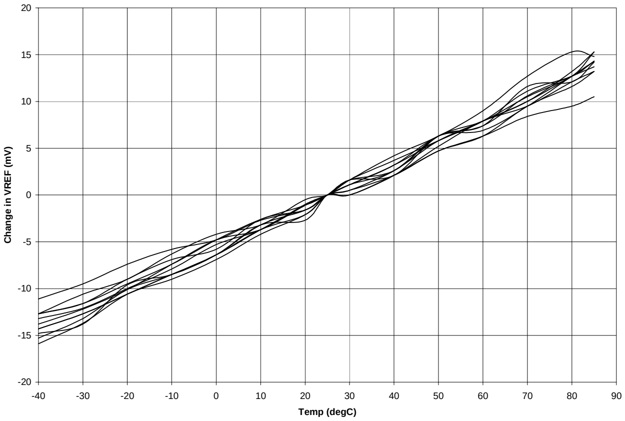


Figure 26. Change in VREF vs. Temperature, 11 parts

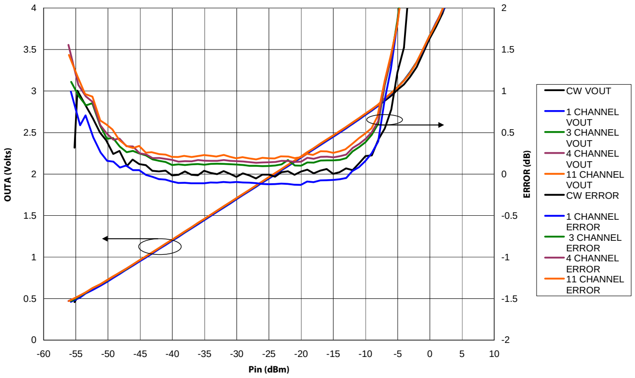


Figure 27. Output Voltage and Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, WCDMA1,3,4 and 11-Channel, Frequency 880MHz.

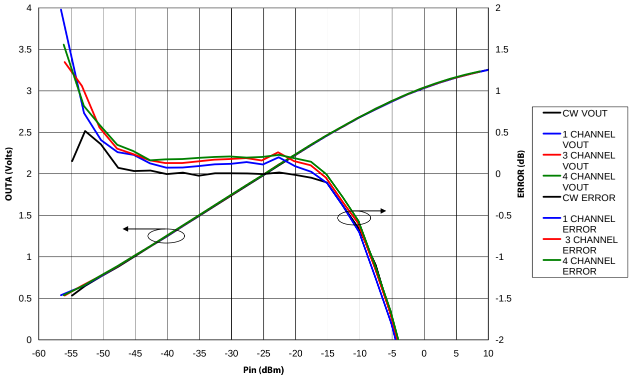


Figure 28. Output Voltage and Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, WCDMA 1,3,4-Channel, Frequency 2140 MHz

GENERAL DESCRIPTION AND THEORY

The AD8364 is a dual channel 2.7GHz true RMS responding detector with 60 dB measurement range and incorporates two AD8362 channels with shared reference circuitry (*See the AD8362 datasheet for more information*). Multiple enhancements have been made to the AD8362 cores to improve measurement accuracy. Log-conformance peak-to-peak ripple has been reduced to < ±0.2 dB, over the entire dynamic range. Temperature stability of the RMS output measurements provides < ± 0.5 dB error over the specified temperature range of -40°C to 85°C, through proprietary techniques. The use of well matched channels offers extremely temperature stable channel difference outputs at **OUTP** and **OUTN**. Given well matched channels through IC integration, the RMS measurement outputs, **OUTA** and **OUTB**, will drift in the same manner (<± 0.5 dB). With **OUTP** shorted to **FBKA**, the function at **OUTP** is:

$$OUTP = OUTA - OUTB + VLVL \qquad (1)$$

When **OUTN** is shorted to **FBKB**, the function at **OUTN** is:

$$OUTN = OUTB - OUTA + VLVL \qquad (2)$$

The difference outputs, **OUTP** and **OUTN**, are insensitive to the common drift due to the difference cancellation of ***OUTA*** and ***OUTB***.

The AD8364 is a fully calibrated RMS-to-DC converter capable of operation from signals as low as a few Hertz to at least 2.7GHz. Unlike logarithmic amplifiers, the AD8364 response is waveform independent. The device accurately measures waveforms having a high peak-to-rms ratio (crest factor). A block diagram is shown below in figure 29.

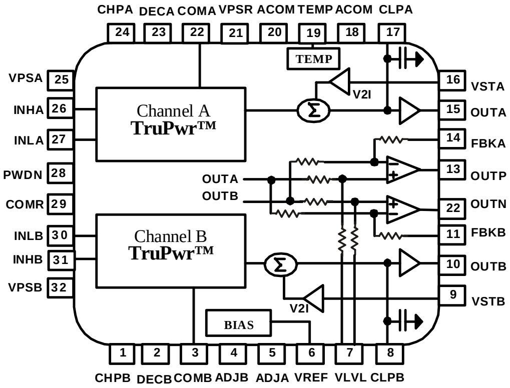


Figure 29. Block Diagram

A single channel of the AD8364 consists of a high performance AGC loop. Referring to figure 30, the AGC loop is comprised of a wide bandwidth variable gain amplifier (VGA), square law detectors, Amplitude Target circuit, and output driver. For more detailed description of the functional blocks, see AD8362 data sheet.

Square Law Detector and Amplitude Target

The output of the VGA, called V_{SIG}, is applied to a wideband square law detector. The detector provides the true RMS response of the RF input signal, independent of waveform, up to crest factors of 6. The detector output, called I_{SQU}, is a fluctuating current with positive mean value. The difference between I_{SQU} and an internally generated current, $I_{TGT[A,B]}$,is integrated by C_F and a capacitor attached to **CLP[A,B]**. C_F is the on chip 25pF filter capacitor. **CLP[A,B]** can be used to arbitrarily increase the averaging time while trading off response time. When the AGC loop is at equilibrium:

$$\mathrm{MEAN}(I_{SQU}) = I_{TGT[A,B]} \qquad (3)$$

This equilibrium occurs only when:

$$\mathrm{MEAN}(V_{SIG}^2) = V_{TGT[A,B]}^2 \qquad (4)$$

Where V_{TGT} is an attenuated version of the V_{REF} voltage.

Since the square law detectors are electrically identical and well matched, process and temperature-dependant variations are effectively cancelled.

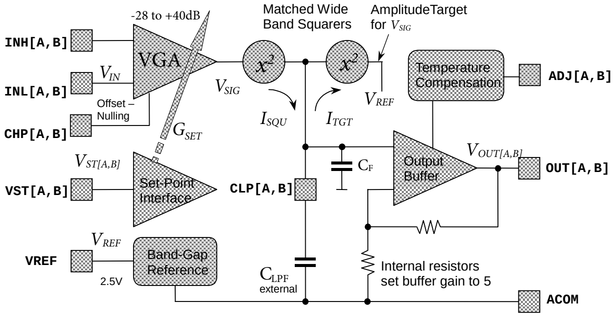


Figure 30. Single Channel Details

By forcing the above identity through varying the VGA set-point, it is apparent that:

$$\mathrm{RMS}(V_{SIG}) = \sqrt{(\mathrm{MEAN}(V_{SIG}^2))} = \sqrt{(V_{TGT}^2)} = V_{TGT} \qquad (5)$$

Substituting the value of V_{SIG}, we have:

$$\mathrm{RMS}(G_0{*}RF_{IN}\exp(-V_{ST[A,B]}/V_{GNS})) = V_{TGT} \qquad (6)$$

When connected as a measurement device $VST[A,B] = OUT[A,B]$. Solving for $OUT[A,B]$ as a function of RF_{IN}:

$$OUT[A,B] = V_{SLOPE}{*}\mathrm{Log10}(\mathrm{RMS}(RF_{IN})/V_Z) \qquad (7)$$

Where V_{SLOPE} is approximately1V/decade or 50mV/dB. V_Z is the intercept voltage, since Log10(1) = 0 when $\mathrm{RMS}(RF_{IN}) = V_Z$. If desired, the effective value of V_{SLOPE} may be altered by using a resistor divider from **OUT[A,B]** to drive **VST[A,B]**. The intercept, V_Z, is approximately 316μV (-70 dBV) with a CW signal. This is the extrapolated intercept since **OUT[A,B]** does not measure down to 0V.

In most applications, the AGC loop is closed through the set point interface, **VST[A,B]**. In measurement mode, **OUT[A,B]** is tied to **VST[A,B]**, respectively. In controller mode, a control voltage is applied to **VST[A,B]**. Pins **OUT[A,B]** drive the control input of a system. The RF feedback signal to the input pins is forced to have an RMS value determined by **VSTA** or **VSTB**.

RF Input interface

The AD8364's RF inputs are connected as shown in figure 31. There are 100Ω resistors connected between DEC[A,B] and INH[A,B] and INL[A,B]. The mid-point is wired to a pin called DEC[A,B]. Internally to the IC, the DC level on DEC[A,B] is established as (7*VPS[A,B] + 55*Vbe)/30. With a 5V supply, DEC[A,B] is at about 2.6V.

Signal coupling capacitors must be connected from the input signal to the INH[A,B] and INL[A,B] pins. The high-pass corner is found as:

$$f_{high\text{-}pass} = 1/(2*\pi*100*C) \qquad (8)$$

A decoupling capacitor should be connected from DEC[A,B] to ground to attenuate any signal at the mid-point. A 100pF and 0.1 F cap from DEC[A,B] to ground are recommended with a 1nF coupling capacitor such that signals above 1.6MHz can be measured. For coupling of signals below 1.6MHz, a good rule of thumb would be to use 100*$C_{coupling}$ for the DEC[A,B] capacitor.

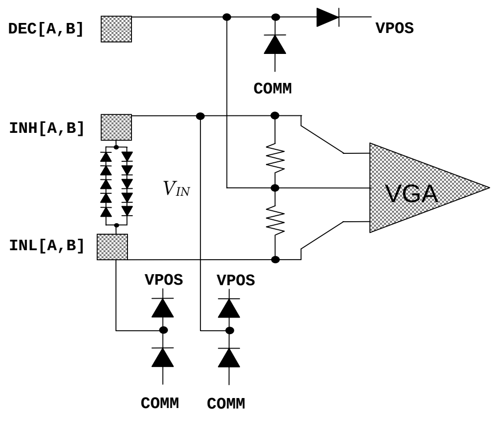


Figure 31. AD8364 RF Inputs

Offset Compensation

An offset-nulling loop is used to address small DC offsets in the VGA. The high-pass corner frequency of this loop is internally preset to about 1 MHz using an on chip capacitor of 25pF (1/(2*π*5KΩ*25pF)), sufficiently low for most HF applications. The high pass corner can be reduced by a capacitor from CHP[A,B] to ground. The input offset voltage varies depending on the actual gain at which the VGA is operating, and thus, on the input signal amplitude. When an excessively large value of $C_{HP[A,B]}$ is used, the offset correction process may lag the more rapid changes in the VGA's gain, which may increase the time required for the loop to fully settle for a given steady input amplitude.

Temperature Sensor Interface

The AD8364 provides a temperature sensor output capable of driving about 1.6 mA. A 330Ω internal resistor is connected from **TEMP** to **COMR** to provide current sink capability. The temperature scaling factor of the output voltage is approximately 2mV/°C. The typical absolute voltage at 27°C is about 630 mV.

VREF Interface

An internal voltage reference is provided to the user at pin **VREF**. The **VREF** voltage is a temperature stable 2.5V reference that can drive about 18mA. An 830Ω internal resistor is connected from **VREF** to **ACOM** for 6mA sink capability.

Power Down Interface

The operating and stand-by currents for the AD8364 at 27°C are approximately 72 mA and 500 μA respectively; The **PWDN** pin is connected to an internal resistor divider made with two 42KΩ resistors. The divider voltage is applied to the base of an npn transistor to force a power down condition when the device is active. Typically when **PWDN** is pulled greater than 1.6V the device is powered down. Figure 22 shows typical response times for various RF input levels. The output reaches to within 0.1 dB of its steady-state value in about 1.6 μs; the reference voltage is available to full accuracy in a much shorter time. This "wake-up" response will vary in detail depending on the input coupling means and the capacitances $C_{DEC[A,B]}$, $C_{HP[A,B]}$ and $C_{LP[A,B]}$; these result are for a measurement system operating in the 0.8 to 2 GHz range, balun-coupled at the input port, with $C_{DEC[A,B]}$ = 100 nF, $C_{HP[A,B]}$ = Open and $C_{LP[A,B]}$ = Open.

VST[A,B] Interface

The **VST[A,B]** interface has a high input impedance of 72KΩ. The voltage at **VST[A,B]** is converted to an internal current used to steer the VGA gain. The VGA attenuation control is set to 20 dB/V.

OUT[A,B,P,N] Outputs

The output drivers used in the AD8364 are different than the output stage on the AD8362. The AD8364 incorporates rail-to-rail output drivers with pull-up and pull-down capability. OUT[A,B,P,N] can source and sink up 70mA. There is also an internal load from both OUTA and OUTB to ACOM of 2.5KΩ.

Measurement Difference Output using OUT[P,N]

The AD8364 incorporates two operational amplifiers with rail-to-rail output capability to provide a difference output. As in the case of the output drivers for OUT[A,B], the output stages have the capability of driving 160mA. **OUTA** and **OUTB** are internally connected through 1KΩ resistors to the inputs of each op-amp. The pin **VLVL** is connected to the positive terminal of both op-amps through 1KΩ resistors to provide level shifting. The negative feedback terminal is also made available through a 1KΩ resistor. The input impedance of **VLVL** is 1KΩ and **FBK[A,B]** is 2KΩ.. See figure 32 below for the connections of these pins.

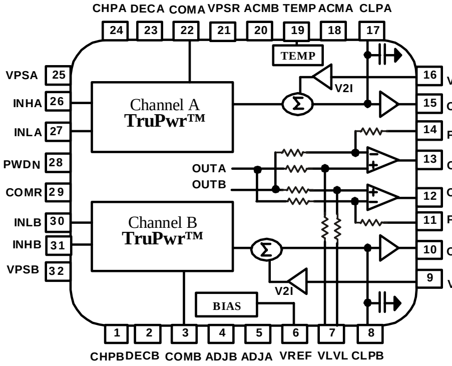


Figure 32. Op-Amp Connections (All resistors are 1KΩ±12%)

If **OUTP** is connected to **FBKA**, then **OUTP** will be given as:

$$OUTP = OUTA - OUTB + VLVL \quad (9)$$

If **OUTN** is connected to **FBKB**, then **OUTN** will be given as:

$$OUTN = OUTB - OUTA + VLVL \quad (10)$$

In this configuration, all four measurements are made available simultaneously **OUT[A,B,P,N]**. A differential output can be taken from ***OUTP*** – ***OUTN*** and **VLVL** can be used to adjust the common mode level for an ADC connection.

Controller mode

The difference outputs can be used for controlling a feedback loop to the AD8364's RF inputs. A capacitor connected between **FBKA** and **OUTP** will form an integrator, keeping in mind that the 1KΩ feedback resistor forms a zero. The sheet resistance of the on chip resistors is ±12%. If Channel A is driven and Channel B has a feedback loop from **OUTP** through a PA, then **OUTP** will integrate to a voltage value such that:

$$OUTB = (OUTA + VLVL)/2 \quad (11)$$

The output value from **OUTN** may or may not be useful. It is given by:

$$OUTN = 0\text{V} \quad (12)$$

For $VLVL < OUTA/3$,

Else,

$$OUTN = (3 * VLVL - OUTA)/2 \quad (13)$$

If **VLVL** is connected to **OUTA**, then **OUTB** will be forced to equal ***OUTA*** through the feedback loop. This flexibility provides the user with the capability to measure one channel operating at given power level and frequency while forcing the other channel to the same power level, or another desired power level, at another frequency. If both channels are operating at the same frequency and ***ADJA*** = ***ADJB***, then there will be little to no temperature drift. When different frequencies are driven into each channel, **ADJA** and **ADJB** must be set accordingly to reduce the temperature drift of the output measurement. The temperature drift will be a statistical sum of the drift from Channel A and Channel B. As stated before, **VLVL** can be used to force the slaved channel to operate at a different power than the other channel. If the two channels are forced to operate at different power level, then some static offset will occur due to voltage drops across metal wiring internal to the IC.

If an inversion is necessary in the feedback loop, **OUTN** can be used as the integrator by placing a capacitor between **OUTN** and **OUTP**. This changes the output equation for **OUTB** and **OUTP** to:

$$OUTB = 2 * OUTA - VLVL \quad (14)$$

For $VLVL < OUTA/2$,

$$OUTN = 0\text{V} \quad (15)$$

Else,

$$OUTN = 2 * VLVL - OUTA \quad (16)$$

The above equations are valid when Channel A is driven and Channel B is slaved through a feedback loop. When Channel B is driven and Channel B is slaved, the above equations can be altered by changing ***OUTB*** to ***OUTA*** and ***OUTN*** to ***OUTP***.

Temperature Compensation Adjustment

The AD8364 has a highly stable measurement output with respect to temperature. However, when the RF inputs exceed a frequency of 1.7GHz, the output temperature drift must be compensated using **ADJ[A/B]**. Proprietary techniques are used to compensate for the temperature drift. However, the absolute value of compensation is different for various frequencies. The following chart can be used to apply the appropriate **ADJ[A/B]** voltage to maintain a temperature drift error less than +/- 0.5dB over the entire temperature range.

F (MHz)	450	900	1700	1900	2200	2500	2700
ADJ[A/B] (V)	0	0	0	0.75	1.02	1.14	1.18

Table 4

Compensating the device for temperature drift using **ADJ[A/B]** allows for great flexibility. If the user requires minimum temperature drift at a given input power or subset of the dynamic range, the **ADJ[A,B]** voltage can be swept while monitoring **OUT[A,B]** over temperature. Figure 33 shows an example of this. The **ADJ[A,B]** value where the output does not change is the voltage that must be applied to have minimum temperature drift at the given power and frequency.

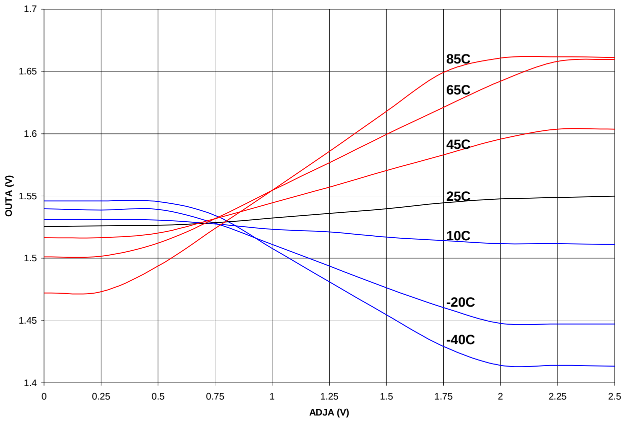


Figure 33. OUTA vs. ADJA over Temp. Pin=-30dBm, 1.9GHz

The **ADJ[A,B]** input has a high input impedance. The input can be conveniently driven from an attenuated value of **VREF**, using a resistor divider.

ALTERING THE SLOPE

None of the changes in operating conditions discussed so far affect the logarithmic slope, V_{SLP}, in Equation 9. However, this can readily be altered by controlling the fraction of VOUT that is fed back to the setpoint interface at the VSET pin. When the full signal from VOUT is applied to VSET, the slope assumes its nominal value of 50 mV/dB. It can be increased by including an attenuator between these pins, as shown in Figure 34. Moderately low resistance values should be used to minimize scaling errors due to the 70 kΩ input resistance at the VSET pin. Keep in mind that this resistor string also loads the output, and it eventually reduces the load-driving capabilities if very low values are used. To calculate the resistor values, use

$$R1 = R2'\left(S_D/50 - 1\right) \qquad (17)$$

where S_D is the desired slope, expressed in mV/dB, and *R2'* is the value of R2 in parallel with 70 kΩ. For example, using R1 = 1.65 kΩ and R2 = 1.69 kΩ (R2' = 1.649 kΩ), the nominal slope is increased to 100 mV/dB. This choice of scaling is useful when the output is applied to a digital voltmeter because the displayed number reads as a decibel quantity directly, with only a decimal point shift.

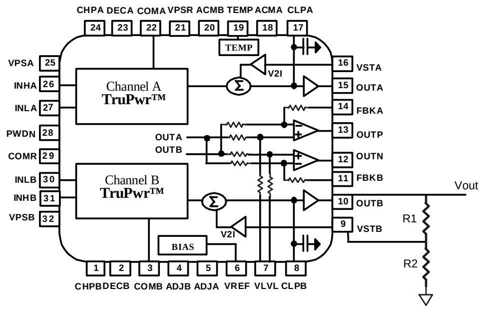
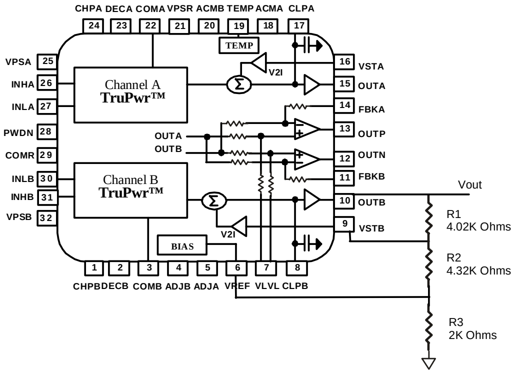


Figure 34. External Network to Raise Slope

Operation at high slopes is useful when a particular sub-range of the input is measured in greater detail. However, a measurement range of 60 dB would correspond to a 6 V change in VOUT at this slope, exceeding the capacity of the AD8364's output stage when operating on a 5 V supply. This requires that the intercept is repositioned to place the desired sub-range within a window corresponding to an output range of 0.2 V ≤ VOUT ≤ 4.8 V,
a 46 dB range.



Using the arrangement shown in Figure 35, an output of 0.5 V corresponds to the lower end of the desired sub-range, and 4.5 V corresponds to the upper limit with 3 dB of margin at each end of the range, which is nominally 3 mV rms to 300 mV rms, with the intercept at 1.9 mV rms. Note that R2 is connected to VREF rather than ground. R3 is needed to ensure that the AD8364's reference buffer, which can sink only a small current, is correctly loaded.

It is apparent that a variable attenuation factor based on this scheme could provide a manual adjustment of the slope, but there are few situations in which this is of value. When the slope is raised by some factor, the loop capacitor, CLPF, should be raised by the same factor to ensure stability and to preserve a chosen averaging time. The slope can be lowered by placing a two-resistor attenuator after the output pin, following standard practice.

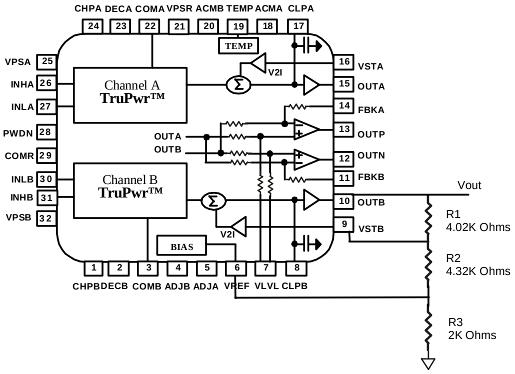


Figure 35. Scheme Providing 100 mV/dB Slope for Operation over a 3 mV to 300 mV Input Range

CHOOSING THE RIGHT VALUE FOR CHPF AND CLPF

The AD8364's variable gain amplifier includes an offset cancellation loop, which introduces a high-pass filter effect in its transfer function. The corner frequency, f_{HP}, of this filter must be below that of the lowest input signal in the desired measurement bandwidth frequency to properly measure the amplitude of the input signal. The required value of the external capacitor is given by

$$CHP[A,B] = 200\mu\text{F}/2\times\pi\times f_{HP}\left(f_{HP}\ in\ Hz\right) \quad (18)$$

Thus, for operation at frequencies down to 100 kHz, **CHP[A,B]** should be 318 pF.

In the standard connections for the measurement mode, the **VST[A,B]** pin is tied to **OUT[A,B]**. For small changes in input amplitude (a few decibels), the time-domain response of this loop is essentially linear with a 3 dB low-pass corner frequency of nominally $f_{LP} = 1/(2\times\pi\times$***CLP[A,B]***$\times 1.1\ \text{k}\Omega)$. Internal time delays around this local loop set the minimum recommended value of this capacitor to about 300 pF, making f_{LP} = 482 KHz.

For operation at lower signal frequencies, or whenever the averaging time needs to be longer, use

$$CLP[A,B]\ = 900\mu\text{F}/2\times\pi\times f_{LP}\left(f_{LP}\ in\ Hz\right) \quad (19)$$

When the input signal exhibits large crest factors, such as a WCDMA signal, ***CLP[A,B]*** must be much larger than might at first seem necessary. This is due to the presence of significant low frequency components in the complex, pseudo-random modulation, which generates fluctuations in the output of the AD8364.

Table 5 Evaluation Board Configuration Options

Component	Function/Notes	Part Number	Default Value
T1, T2	The dynamic range of the AD8364 is directly related to the magnitude and phase balance of the Balun feeding the RF signal to the part. The evaluation board includes M/A-COM MABAES0031 solderd to the board and two unsoldered M/A-COM ETC1.6-4-2-3. The MABAES0031 has good magnitude and phase balance between 10MHz and 500MHz, then slowly degrades above 500MHz. The performance of the evaluation board will be degraded above 500 MHz due to the balun. The M/A-COM ETC1.6-4-2-3 broadband baluns allows limited dynamic range performance between 500 – 2500 MHz. Better dynamic range can be achieved by using narrow band baluns with better magnitude and phase performance.	M/A-COM MABAES0031	
C11, C13, C21	Supply filtering/decoupling capacitors		0.1 µF
C10, C12,C20	Supply filtering/decoupling capacitors		100 pF
C19	VREF filtering/decoupling capacitors		0.1 µF
C18	VLVL filtering/decoupling capacitors		tbd
C15, C17	Output low-pass filter capacitors		0.1 µF
C14, C16	Output low-pass filter capacitors, can be activated by removing jumpers R15 and R6		0.1 µF
C23, C24	Input bias-point decoupling capacitors		100 pF
C1, C8	Input bias-point decoupling capacitors		0.1 µF
C2, C3, C4, C5, C6, C7	Input signal coupling capacitors		0.1 µF
C9, C22	Input high-pass filter capacitor		0.1 µF
DUT	AD8364	AD8364XCP	
R4, R5, R6, R9, R12, R15, R17, R19, R21, R24, R23,	Jumpers		0 Ω
R10, R11	Capacitors can be installed for controller mode		
R2, R13, R16, R18, R20	Optional pull-down resistors		10 kΩ/OPEN
R1, R3	100 Ω Resistor to be added when input coupling from a single-ended source (not installed)		100 Ω
R14	To be added for use in slope adjustment (not installed)		
SW1	Power-down/enable or external power-down selector		
SW2, SW3	Measurement mode/controller mode selector		
SW4	VLVL VREF/External controll selector		
SW5	ADJA VREF/External controll selector		
SW6	ADJB VREF/External controll selector		

Evaluation Board (10MHz – 500MHz)

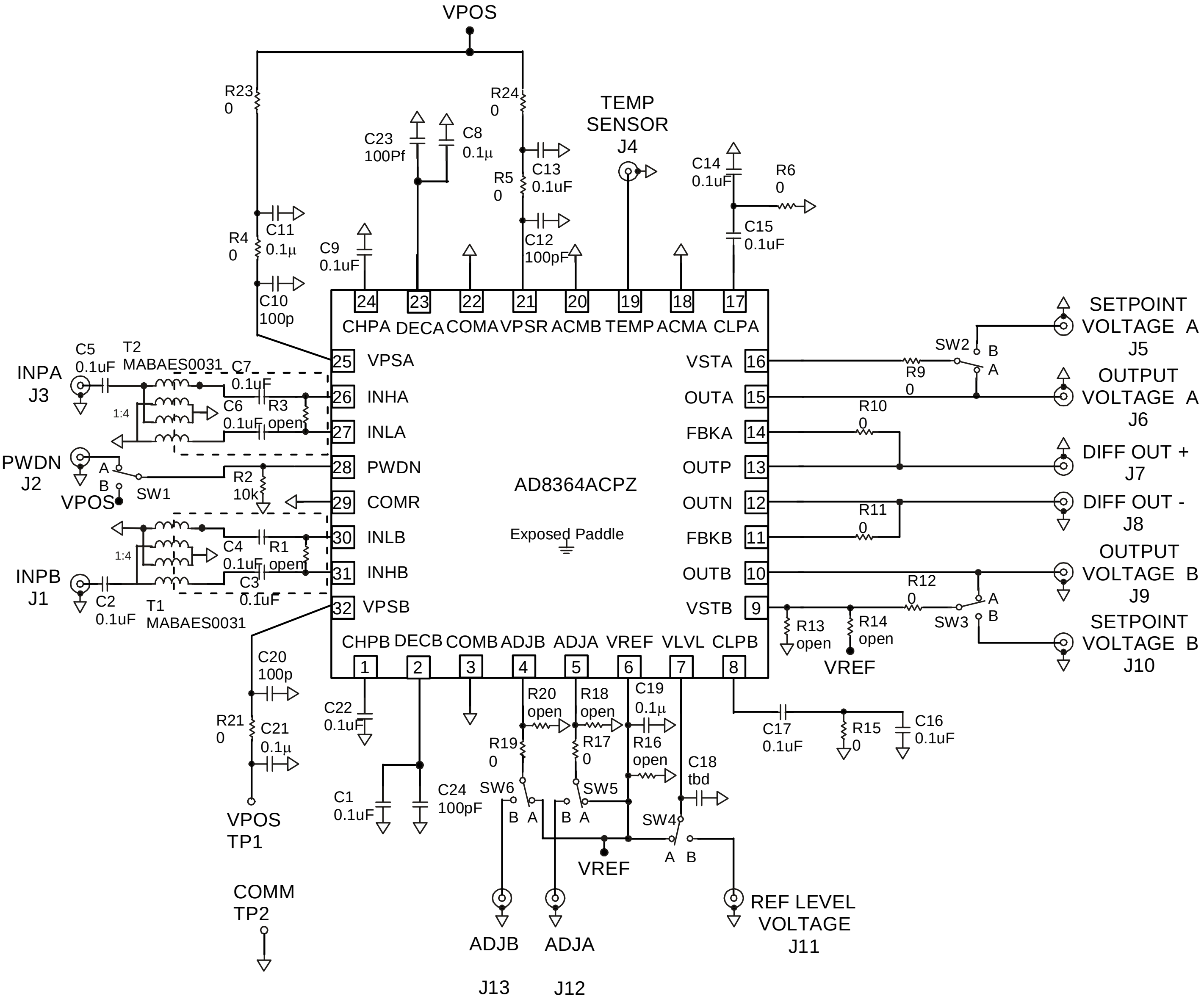


Figure 36. Evaluation Board

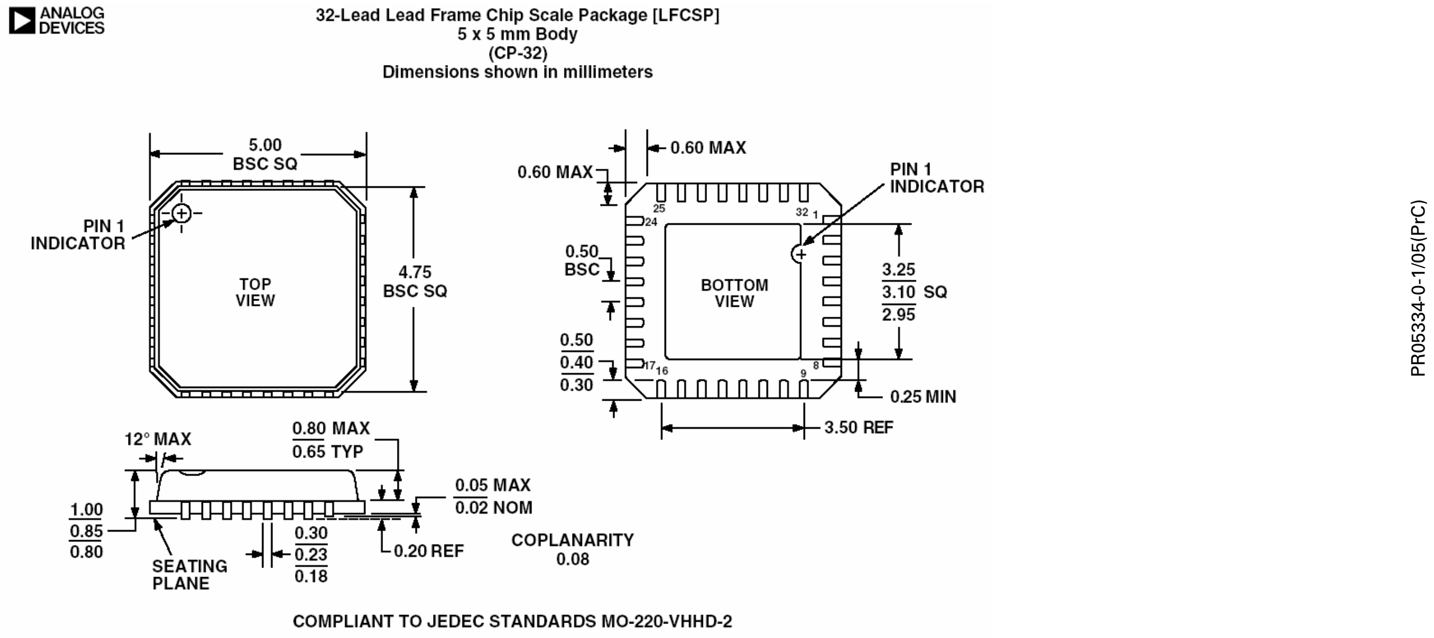


Figure 37. Package

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8364XCP	−40°C to +85°C	32-Lead LFCSP	
AD8364-EVAL		Evaluation Board	