DDR SDRAM DIMM

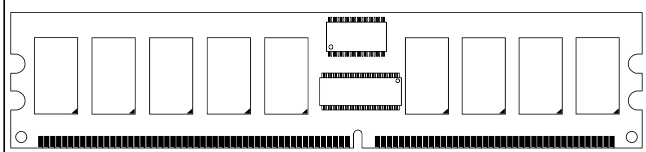
MT18VDDF6472

For the latest data sheet, please refer to the Micron Web site: www.micron.com/moduleds

FEATURES

- 184-pin, dual in-line memory modules (DIMM)
- ECC, 1-bit error detection and correction
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 333MT/s, 266MT/s, and 200MT/s DDR FBGA SDRAM components
- Fast data transfer rates; PC2700, PC2100, or PC1600
- 512MB (64 Meg x 72)
- V_{DD} = $V_{DD}Q$ = +2.5V ±0.2V
- V_{DDSPD} = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto Refresh and Self Refresh Modes
- 7.8125µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Selectable READ CAS latency
- Gold-plated edge contacts

184-Pin DIMM
MO-206



ADDRESS TABLE

	512MB
Refresh Count	8K
Base Device Configuration	64 Meg x 4
Device Bank Addressing	4 (BA0, BA1)
Device Row Addressing	8K (A0–A12)
Device Column Addressing	2K (A0–A9, A11)
Module Bank Addressing	1 (S0#)

OPTIONS — MARKING

- Package
  - 184-pin DIMM (gold) — G
- Memory Clock/Speed, CAS Latency*
  - 6ns (166 MHz), 333MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2 — -26A
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5 — -265
  - 10ns (133 MHz), 200 MT/s, CL = 2 — -202

*An additional clock cycle will be incurred when module is in registered mode

PART NUMBERS AND TIMING PARAMETERS

PART NUMBER	PART MARKING	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA BIT RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)*
MT18VDDF6472G-335__	-335	512MB	64 Meg x 72	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT18VDDF6472G-26A__	-26A	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT18VDDF6472G-265__	-265	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT18VDDF6472G-202__	-202	512MB	64 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18VDDF6472G-265A1

PIN ASSIGNMENT (184-PIN DIMM FRONT)

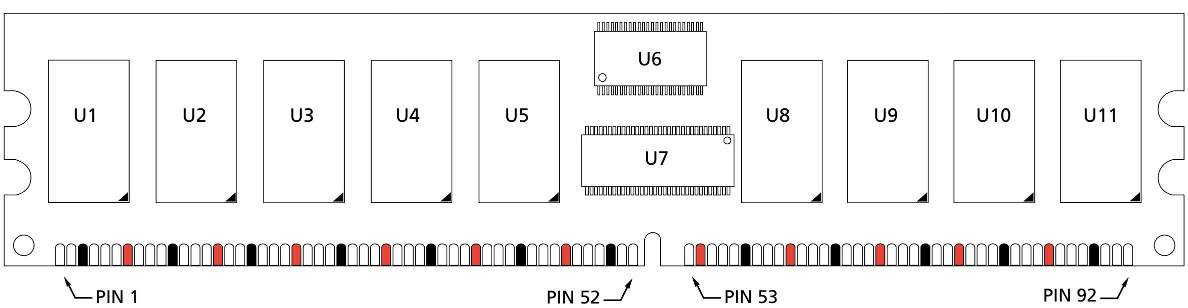
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DQS8	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	CB2	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	CB3	74	VSS
6	DQ2	29	A7	52	BA1	75	NC
7	VDD	30	VDD	53	DQ32	76	NC
8	DQ3	31	DQ19	54	VDD	77	VDD
9	NC	32	A5	55	DQ33	78	DQS6
10	RESET#	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	NC	39	DQ26	62	VDD	85	VDD
17	NC	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	CB0	67	DQS5	90	NC
22	VDD	45	CB1	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

PIN ASSIGNMENT (184-PIN DIMM BACK)

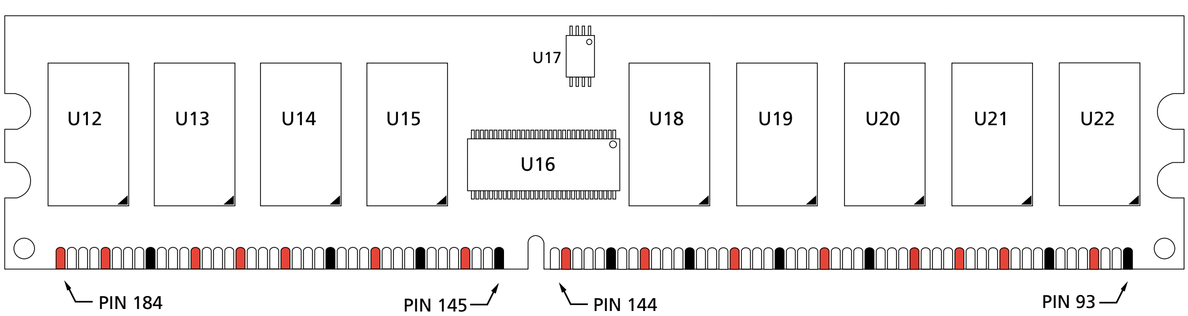
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DQS17	163	NC
95	DQ5	118	A11	141	A10	164	VDD
96	VDD	119	DQS11	142	CB6	165	DQ52
97	DQS9	120	VDD	143	VDD	166	DQ53
98	DQ6	121	DQ22	144	CB7	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13	172	VDD
104	VDD	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDD	151	DQ39	174	DQ60
106	DQ13	129	DQS12	152	VSS	175	DQ61
107	DQS10	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DQS16
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDD	179	DQ63
111	DNU	134	CB4	157	S0#	180	VDD
112	VDD	135	CB5	158	DNU	181	SA0
113	NC	136	VDD	159	DQS14	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	A12	138	CK0#	161	DQ46	184	VDDSPD

PIN ASSIGNMENT (184-Pin DIMM)

Front View



Back View



Indicates a VDD or VDDQ pin   Indicates a VSS pin

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
137, 138	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS pins) is referenced to the crossings of CK0 and CK0#.
21	CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
157	S0#	Input	Chip Select: S# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S0# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115, 118, 122, 125, 130, 141	A0-A12	Input	Address Inputs: A0-A12 provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
1	V_{REF}	Input	SSTL_2 reference voltage.

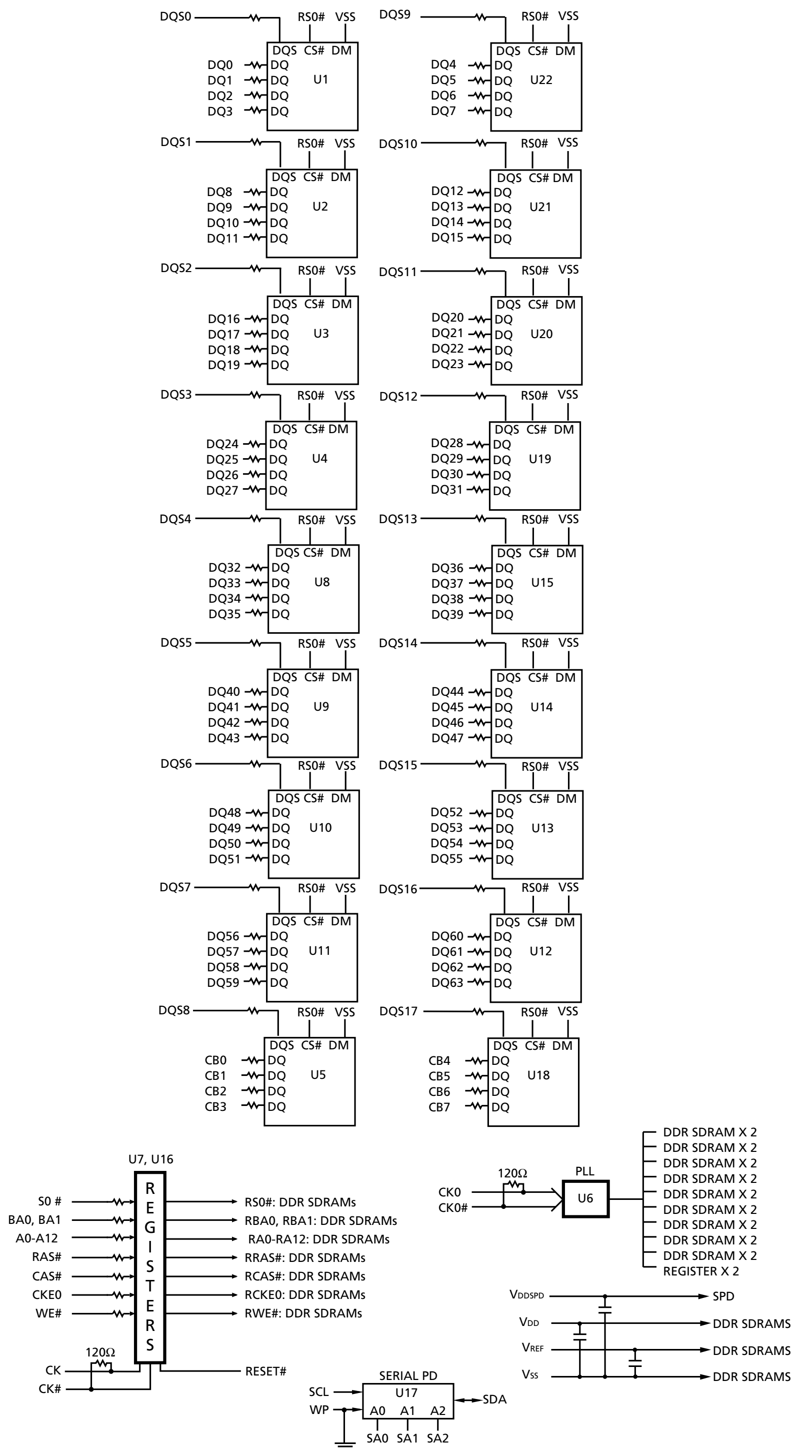
NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number/symbol information.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
91	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
10	RESET#	Input	Asynchronously forces all register outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure CKE are LOW and DDR SDRAM DQs are High-Z.
44, 45, 49, 51, 134, 135, 142, 144	CB0-CB7	Input/ Output	Data I/Os: Check bits. ECC, 1-bit error detection and correction.
5, 14, 25, 36, 47, 56, 67, 78, 86, 97, 107, 119, 129, 140, 149, 159, 169, 177	DQS0-DQS17	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
2, 4, 6, 8, 12,13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162 165, 166, 170, 171, 174 175, 178, 179	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
7, 15, 22, 30, 38, 46, 54, 62, 70, 77, 85, 96,104, 108, 112, 120, 128, 136, 143, 148, 156, 164, 168, 172, 180	V_{DD}	Supply	DQ Power Supply: +2.5V $\pm$0.2V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply–2.3V to 3.6V.
9, 16, 17, 71, 75, 76, 82, 90, 101 - 103,113, 163, 167, 173	NC	—	No Connect: These pins should be left unconnected.
111, 158	DNU	—	Do Not Use: These pins are not connected on this module but are assigned pins on other modules in this product family.

NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number/symbol information.

FUNCTIONAL BLOCK DIAGRAM



U1-U5, U8-U15, U18-U22 = MT46V46MFJ DDR SDRAMs

NOTE: 1. All resistor values are 22 ohms unless otherwise specified.

2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.
3. To optimize system and loading and signal integrity for -335 speed grade modules, 3Ω (single bank modules) or 5Ω (dual bank modules) stub resistors may be placed on command/address and control lines. Contact Micron CCG Applications for additional information.

GENERAL DESCRIPTION

The MT18VDDF6472 is a high-speed CMOS, dynamic random-access, 512MB registered memory module organized in a x72 (ECC) configuration. This module uses internally configured quad-bank DDR SDRAMs.

The DDR SDRAM module uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single $2n$-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The DDR SDRAM module operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting column location for the burst access.

The DDR SDRAM module provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of the DDR SDRAM module allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the Micron 256Mb DDR SDRAM data sheet.

PLL AND REGISTER OPERATION

The DDR SDRAM module is operated in registered mode where the control/address input signals are latched in the register on one rising clock edge and sent to the DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock). A phase-lock loop (PLL) on the module is used to redrive the differential clock signals CK and CK# to the DDR SDRAM devices to minimize system clock loading.

SERIAL PRESENCE-DETECT OPERATION

The DDR SDRAM module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

REGISTER DEFINITION

MODE REGISTER

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in the Mode Register Diagram. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

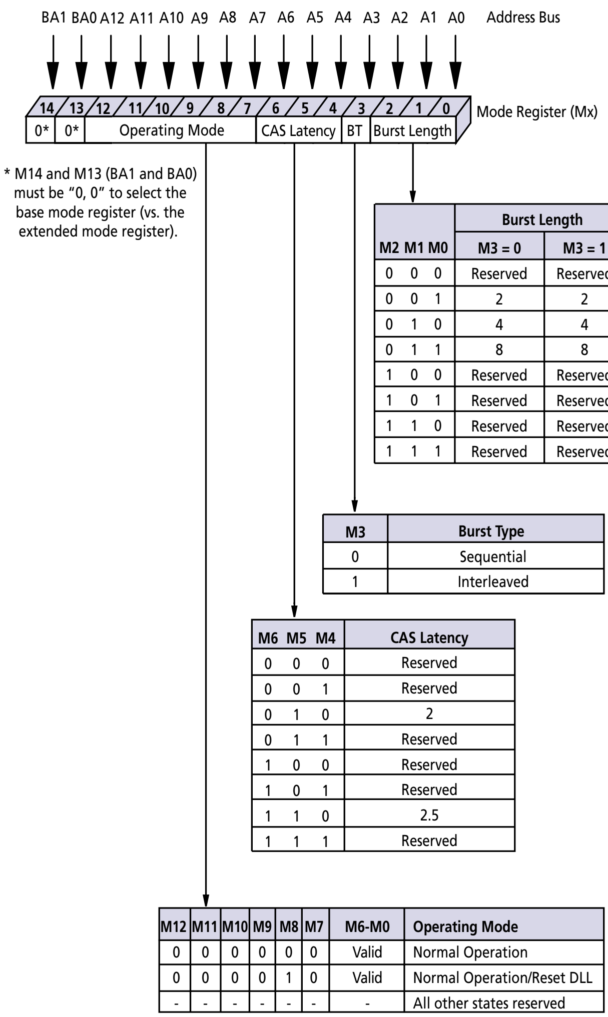
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A12 when the burst length is set to two, by A2-A12 when the burst length is set to four and by A3-A12 when the burst length is set to eight. The remaining address bits are used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table.



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Mode Register Definition Diagram

Burst Definition Table

Burst Length	Starting Column Address	Order of Accesses Within a Burst: Type = Sequential	Type = Interleaved
2	**A0**		
	0	0-1	0-1
	1	1-0	1-0
4	**A1 A0**		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	**A2 A1 A0**		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

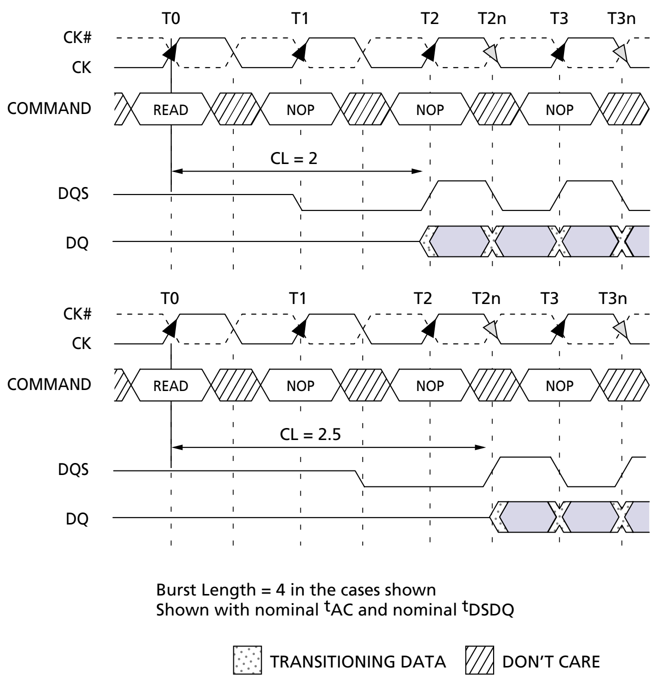
NOTE:
1. For a burst length of two, A1-A12 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A12 select the four-data-element block; A0-A1 select the first access within the block.
3. For a burst length of eight, A3-A12 select the eight-data-element block; A0-A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in CAS Latency Diagram.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.



CAS Latency Diagram

CAS LATENCY (CL) TABLE

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CL = 2*	CL = 2.5*
-335	75 ≤ f ≤ 133	75 ≤ f ≤ 167
-26A	75 ≤ f ≤ 133	75 ≤ f ≤133
-265	75 ≤ f ≤ 100	75 ≤ f ≤133
-202	75 ≤ f ≤ 100	75 ≤ f ≤125

* An additional clock cycle will be incurred when module is in register mode.

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A12 each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

EXTENDED MODE REGISTER

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in the Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

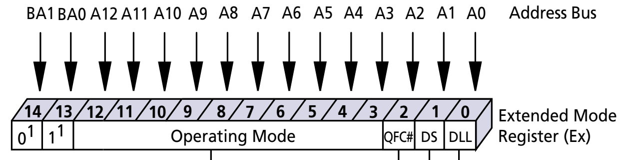
The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Output Drive Strength

The normal full drive strength for all outputs are specified to be SSTL2, Class II. For detailed information on output drive strength option, refer to the 256Mb DDR SDRAM data sheet.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.



E0	DLL
0	Enable
1	Disable

E1[1]	Drive Strength
0	Normal

E2[2]	QFC# Function
0	Disabled
–	Reserved

E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2, E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	Reserved

NOTE: 1. E14 and E13 (BA1 and BA0) must be “0, 1” to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

Extended Mode Register Definition Diagram

COMMANDS

Truth Tables 1 and 2 provide a general reference of available commands. For a more detailed description of commands and operations, refer to Micron's 256Mb DDR SDRAM data sheet.

TRUTH TABLE 1 – COMMANDS

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select device bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select device bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select device bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in device bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

TRUTH TABLE 2 – DM OPERATION

(Note: 10)

NAME (FUNCTION)	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A12 provide the op-code to be written to the selected mode register.
3. BA0-BA1 provide device bank address and A0-A12 provide row address.
4. BA0-BA1 provide device bank address; A0-A9, 11 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which device bank is precharged.
   A10 HIGH: all device banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data; provided coincident with the corresponding data.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} Supply Voltage Relative to V_{SS} .... -1V to +3.6V
$V_{DD}Q$ Supply Voltage Relative to V_{SS} .... -1V to +3.6V
V_{REF} and Inputs Voltage
Relative to V_{SS} .... -1V to +3.6V
I/O Pins Voltage
Relative to V_{SS} .... -0.5V to $V_{DD}Q$ +0.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1–5, 14; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{DD}	2.3	2.7	V	32, 36
I/O Supply Voltage		$V_{DD}Q$	2.3	2.7	V	32, 36, 39
I/O Reference Voltage		V_{REF}	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	6, 39
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 39
Input High (Logic 1) Voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	25
Input Low (Logic 0) Voltage		$V_{IL(DC)}$	-0.3	V_{REF} - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Registered Inputs	I_I	-5	5	µA	48
	DQ, DQS	I_I	-2	2	µA	
	CK0/CK0#	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)		I_{OZ}	-5	5	µA	48
OUTPUT LEVELS: High Current (V_{OUT} = $V_{DD}Q$-0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	-16.8	–	mA	33, 32
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA	

AC INPUT OPERATING CONDITIONS

(Notes: 1–5, 14; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	$V_{IH(AC)}$	V_{REF} + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	–	V_{REF} - 0.310	V	12, 25, 35
I/O Reference Voltage	$V_{REF(AC)}$	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	6

I_{DD} SPECIFICATIONS AND CONDITIONS*

(Notes: 1–5, 8, 10, 12; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER/CONDITION		SYM	MAX -335	MAX -26A/-265	MAX -202	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.		I_{DD0}	TBD	TBD	TBD	mA	20, 43
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle.		I_{DD1}	TBD	TBD	TBD	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW.		I_{DD2P}	TBD	TBD	TBD	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^tCK = ^tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM.		I_{DD2F}	TBD	TBD	TBD	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW.		I_{DD3P}	TBD	TBD	TBD	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.		I_{DD3N}	TBD	TBD	TBD	mA	42
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA.		I_{DD4R}	TBD	TBD	TBD	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle.		I_{DD4W}	TBD	TBD	TBD	mA	20
AUTO REFRESH CURRENT	^tRC = ^tRFC (MIN)	I_{DD5}	TBD	TBD	TBD	mA	20, 45
	^tRC = 7.8125µs	I_{DD5}[a]	TBD	TBD	TBD	mA	24, 44
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD6}	TBD	TBD	TBD	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL=4) with auto precharge with, ^tRC = minimum ^tRC allowed; ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands.		I_{DD7}	TBD	TBD	TBD	mA	20, 44

*DDR SDRAM components only

CAPACITANCE

(Note: 11; notes appear following parameter tables)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C_{IO}	4.0	5.0	pF
Input Capacitance: Command and Address; S0#; CKE0	C_{I1}	2.5	3.5	pF
Input Capacitance: CK0, CK0#	C_{I2}	-	4.0	pF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

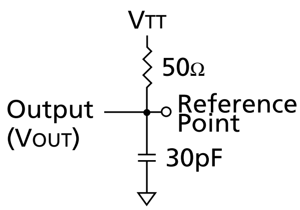
(Notes: 1–5, 12–15, 29; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

AC CHARACTERISTICS		-335		-26A/-265		-202			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#	^{t}AC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width	^{t}CH	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	26
CK low-level width	^{t}CL	0.45	0.55	0.45	0.55	0.45	0.55	^{t}CK	26
Clock cycle time CL = 2.5	^{t}CK (2.5)	6	13	7.5	13	8	13	ns	40, 47
Clock cycle time CL = 2	^{t}CK (2)	7.5	13	7.5/10	13	10	13	ns	40, 47
DQ and DM input hold time relative to DQS	^{t}DH	0.45		0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS	^{t}DS	0.45		0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)	^{t}DIPW	1.75		1.75		2		ns	27
Access window of DQS from CK/CK#	^{t}DQSCK	-0.60	+0.60	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width	^{t}DQSH	0.35		0.35		0.35		^{t}CK	
DQS input low pulse width	^{t}DQSL	0.35		0.35		0.35		^{t}CK	
DQS-DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ		.35*		0.5		0.6	ns	22, 23
Write command to first DQS latching transition	^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	^{t}CK	
DQS falling edge to CK rising - setup time	^{t}DSS	0.2		0.2		0.2		^{t}CK	
DQS falling edge from CK rising - hold time	^{t}DSH	0.2		0.2		0.2		^{t}CK	
Half clock period	^{t}HP	^{t}CH,^{t}CL		^{t}CH,^{t}CL		^{t}CH,^{t}CL		ns	30
Data-out high-impedance window from CK/CK#	^{t}HZ		+0.75		+0.75		+0.8	ns	16, 37
Data-out low-impedance window from CK/CK#	^{t}LZ	-0.70		-0.75		-0.8		ns	16,38
Address and control input hold time (fast slew rate)	$^{t}IH_F$	.75		.90		1.1		ns	12
Address and control input setup time (fast slew rate)	$^{t}IS_F$	.75		.90		1.1		ns	12
Address and control input hold time (slow slew rate)	$^{t}IH_S$	.80		1		1.1		ns	12
Address and control input setup time (slow slew rate)	$^{t}IH_S$	.80		1		1.1		ns	12
LOAD MODE REGISTER command cycle time	^{t}MRD	12		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	^{t}QH	^{t}HP -^{t}QHS		^{t}HP -^{t}QHS		^{t}HP -^{t}QHS		ns	22, 23
Data Hold Skew Factor	^{t}QHS		0.50*		0.75		1	ns	
ACTIVE to PRECHARGE command	^{t}RAS	42	70,000	40	120,000	40	120,000	ns	31
ACTIVE to READ with Auto precharge command	^{t}RAP	18		20		20		ns	41
ACTIVE to ACTIVE/AUTO REFRESH command period	^{t}RC	60		65		70		ns	
AUTO REFRESH command period	^{t}RFC	72		75		80		ns	45
ACTIVE to READ or WRITE delay	^{t}RCD	18		20		20		ns	
PRECHARGE command period	^{t}RP	18		20		20		ns	
DQS read preamble	^{t}RPRE	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CK	37
DQS read postamble	^{t}RPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
ACTIVE bank *a* to ACTIVE bank *b* command	^{t}RRD	12		15		15		ns	
DQS write preamble	^{t}WPRE	0.25		0.25		0.25		^{t}CK	
DQS write preamble setup time	^{t}WPRES	0		0		0		ns	18, 19
DQS write postamble	^{t}WPST	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	17
Write recovery time	^{t}WR	15		15		15		ns	
Internal WRITE to READ command delay	^{t}WTR	1		1		1		^{t}CK	
Data valid output window (DVW)	na	^{t}QH - ^{t}DQSQ		^{t}QH - ^{t}DQSQ		^{t}QH - ^{t}DQSQ		ns	22
REFRESH to REFRESH command interval	^{t}REFC		70.3		70.3		70.3	µs	21
Average periodic refresh interval	^{t}REFI		7.8		7.8		7.8	µs	21
Terminating voltage delay to V_{DD}	^{t}VTD	0		0		0		ns	
Exit SELF REFRESH to non-READ command	^{t}XSNR	75		75		80		ns	
Exit SELF REFRESH to READ command	^{t}XSRD	200		200		200		^{t}CK	

*AC timing values for -335 FBGA DDR SDRAM device.

NOTES

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:

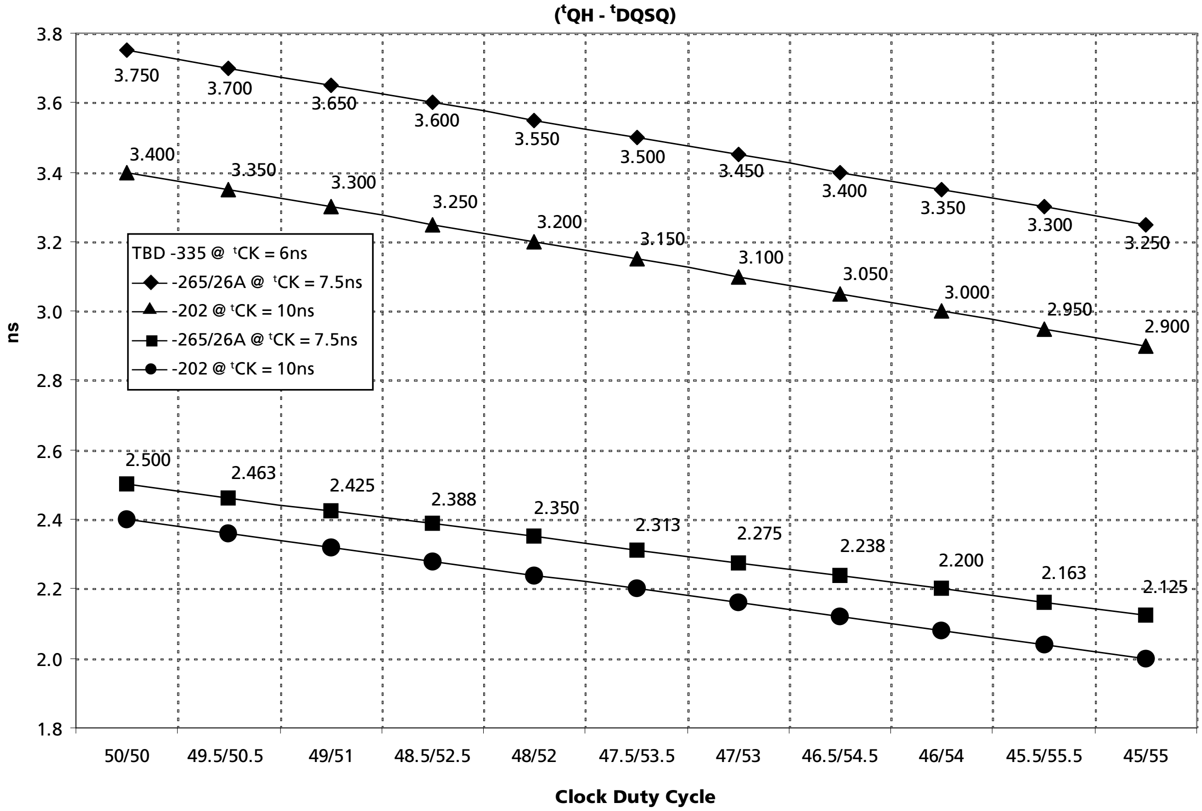


4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from $V_{DD}Q/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -26A and -202, CL = 2.5 for -335 and -265 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, $V_{OUT(DC)}$ = $V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -265 with slew rates 1V/ns and faster, ^{t}IS and ^{t}IH are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. ^{t}IH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x $V_{DD}Q$ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
20. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

NOTES (continued)

21. The refresh period 64ms. This equates to an average refresh rate of 7.821µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications - ^tHP ($^tCK/2$), ^tDQSQ, and ^tQH ($^tQH = {}^tHP - {}^tQHS$). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
23. Referenced to each output group: x4 = DQS with DQ0-DQ3.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^tRFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^tDS and ^tDH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.

DERATING DATA VALID WINDOW (^tQH - ^tDQSQ)



NOTES (continued)

28. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. ^tHP min is the lesser of ^tCL minimum and ^tCH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until $^tRAS_{(MIN)}$ can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch must be less than 1/3 of the clock and not more than +400mV or 2.9 volts, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2 volts, whichever is more positive.
33. Normal Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure A.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure A.
    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure B.
    d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure B.
    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 Volt, and at the same voltage and temperature.
    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0 Volt.
34. The voltage levels used are derived from a minimum V_{DD} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VIH overshoot: VIH(MAX) = $V_{DD}Q$+1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL(MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. V_{DD} and V_{DDQ} must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for ^tHZ(MAX) and the last DVW. ^tHZ(MAX) will prevail over ^tDQSCK(MAX) + ^tRPST(MAX) condition. ^tLZ(MIN) will prevail over ^tDQSCK(MIN) + ^tRPRE(MAX) condition.

Figure A
Pull-Down Characteristics

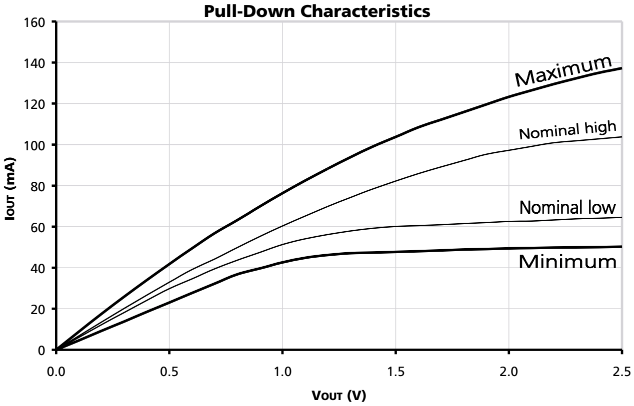
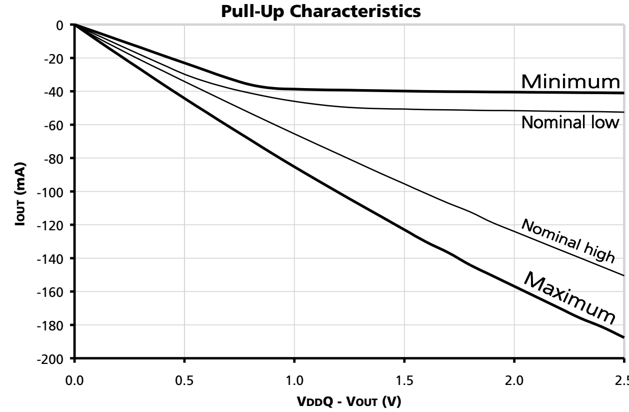


Figure B
Pull-Up Characteristics



NOTES (continued)

38. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, V_{DDQ}, V_{TT}, and V_{REF} must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{DD}/V_{DDQ} are 0 volts, provided a minimum of 42 ohms of series resistance is used between the V_{TT} supply and the input pin.
40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. $^{t}RAP \geq {}^{t}RCD$.
42. For the -335, -26A, and -265 modules, $I_{DD}3N$ is specified to be 35mA.
43. Random addressing changing 50% of data changing at every transfer.
44. Random addressing changing 100% of data changing at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
46. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
48. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

REGISTER TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

(Note: 1)

REGISTER	SYMBOL	PARAMETER	CONDITIONS	T_A = 0-70° C V_{DD} = 2.5V ± 0.2V MIN	MAX	UNITS	NOTES
1:2 13-26 bit SSTL	^tCK	Clock Frequency		–	200	MHz	
	^tPD	Clock to Output Time	30pF to GND and 50 ohms to V_{TT}	1.1	2.8	ns	
	^tsu	Setup time, fast slew rate (see Notes 1 and 3)		0.75	–	ns	2, 4
		Setup time, slow slew rate (see Notes 2 and 3)		0.9	–	ns	3, 4
	th	Hold time, fast slew rate (see Notes 1 and 3)		0.75	–	ns	2, 4
		Hold time, slow slew rate (see Notes 2 and 3)		0.9	–	ns	3, 4
	$C_{IN}(CK)$	Clock Input Capacitance		2.5	3.5	pF	
	$C_{IN}(data)$	Data Input Capacitance		2.5	3.5	pF	

NOTE:
1. The timing specifications for the register listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information on this part has been shown at the JEDEC JC-40 Committee. Please contact Micron Technology's Module Applications Team if further information on the specific register model is required.
2. For data signal, input slew rate ≥ 1 V/ns.
3. For data signal, input slew rate ≥ 0.5 V/ns and < 1 V/ns.
4. For CK and CK# signals, input slew rates are ≥ 1 V/ns.

PLL CLOCK DRIVER TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

(Note: 1) (Specifications for the PLL component used on the module.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Clock frequency	^{f}C		66		167	MHz
Input clock duty cycle			40%		60%	
Stabilization time[1]					0.1	ms
Low-to high level propagation delay time	^{t}PLH	CK mode/CK to any output	1.5	3.5	6	ns
High-to low level propagation delay time	^{t}PHL	CK mode/CK to any output	1.5	3.5	6	ns
Output enable time	^{t}en	CK mode/G to any Y output		3		ns
Output disable time	^{t}dis	CK mode/G to any Y output		3		ns
Jitter (peak-to-peak)	^{t}(jitter)	66 MHz			120	ps
		100/125/133/167 MHz			75	
Jitter (cycle-to-cycle)	^{t}(jitter)	66 MHz			110	ps
		100/125/133/167 MHz			65	
Phase error	^{t}(phase error)	Terminated with 120 ohm/16pF	-150		150	ns
Output skew	^{t}skew(o)	Terminated with 120 ohm/16pF			100	ns
Pulse skew	^{t}dis	Terminated with 120 ohm/16pF			100	ns
Duty cycle		66 MHz to 100 MHz	49.5%		50.5%	
		101 MHz to 167 MHz	49%		51%	
Output rise and fall times (20% - 80%)	^{t}r, ^{t}f	Load = 120 ohm/16pF	650	800	950	ps

NOTE:
1. The timing specifications for the register listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information on this part has been shown at the JEDEC JC-40 Committee. Please contact Micron Technology's Module Applications Team if further information on the specific register model is required.
2. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions as indicated in Figures 1 and 2.

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data as indicated in Figure 3.

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 1
Data Validity

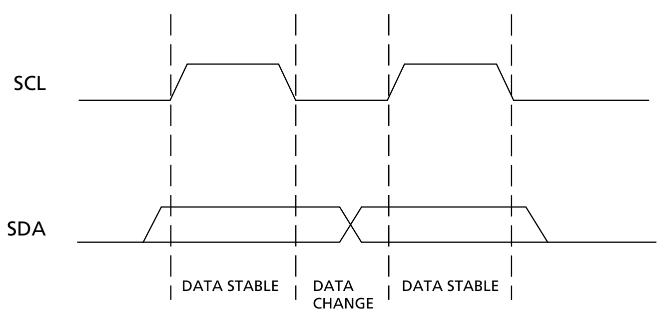


Figure 2
Definition of Start and Stop

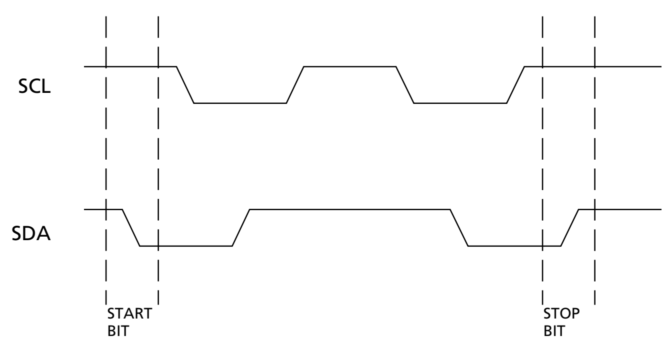
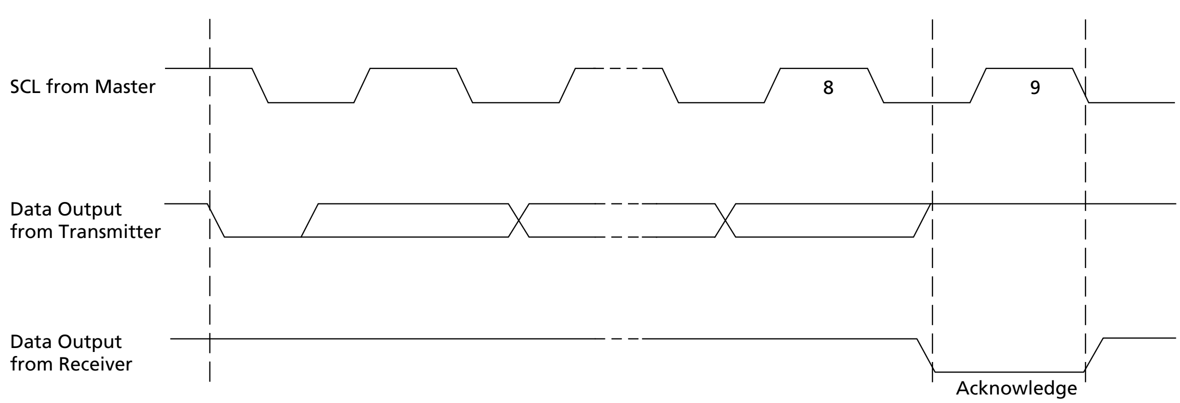


Figure 3
Acknowledge Response From Receiver



EEPROM DEVICE SELECT CODE

The most significant bit (b7) is sent first

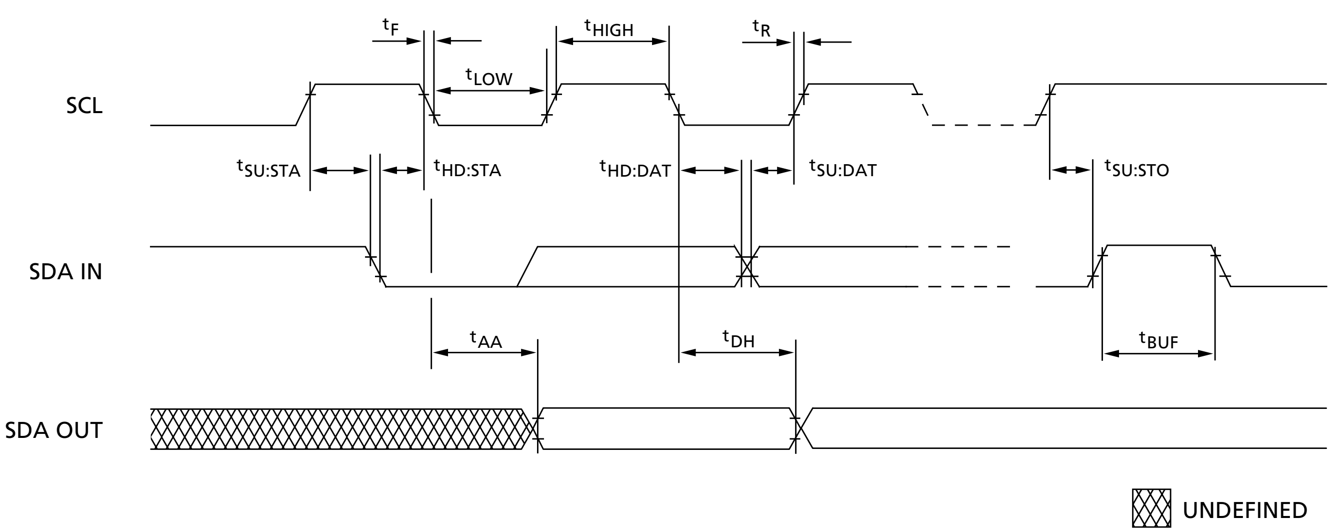
	DEVICE TYPE IDENTIFIER				CHIP ENABLE			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	$R\overline{W}$
Protection Register Select Code	0	1	1	0	E2	E1	E0	$R\overline{W}$

EEPROM OPERATING MODES

MODE	$R\overline{W}$ BIT	WC[1]	BYTES	INITIAL SEQUENCE
Current Address Read	1	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	0	X	1	START, Device Select, $R\overline{W}$ = '0', Address
	1	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Page Write	0	V_{IL}	≤ 16	START, Device Select, $R\overline{W}$ = '0'

NOTE: 1. X = V_{IH} or V_{IL}.

SPD EEPROM TIMING DIAGRAM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
^tAA	0.3	3.5	µs
^tBUF	4.7		µs
^tDH	300		ns
^tF		300	ns
$^tHD:DAT$	0		µs
$^tHD:STA$	4		µs

SYMBOL	MIN	MAX	UNITS
^tHIGH	4		µs
^tLOW	4.7		µs
^tR		1	µs
$^tSU:DAT$	250		ns
$^tSU:STA$	4.7		µs
$^tSU:STO$	4.7		µs

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DDSPD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DDSPD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

NOTE: 1. The timing specifications for the register listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information on this part has been shown at the JEDEC JC-40 Committee. Please contact Micron Technology's Module Applications Team if further information on the specific register model is required.

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 2) (V_{DDSPD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	3

NOTE:
1. All voltages referenced to V_{SS}.
2. All voltages referenced to V_{SS}.
3. Timing actually specified by ^{t}WR.

SERIAL PRESENCE-DETECT MATRIX

(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18VDDF6472G (Hex)
0	NUMBER OF SPD BYTES USED BY MICRON	128	80
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	256	08
2	FUNDAMENTAL MEMORY TYPE	SDRAM DDR	07
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	13	0D
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	11	0B
5	NUMBER OF PHYSICAL BANKS ON DIMM	1	01
6	MODULE DATA WIDTH	72	48
7	MODULE DATA WIDTH (continued)	0	00
8	MODULE VOLTAGE INTERFACE LEVELS ($V_{DD}Q$)	SSTL 2.5V	04
9	SDRAM CYCLE TIME, (^{t}CK) (CAS LATENCY = 2.5) (Note 2)	6ns (-335) 7ns (-26A) 7.5ns (-265) 8ns (-202)	60 70 75 80
10	SDRAM ACCESS FROM CLOCK,(^{t}AC) (CAS LATENCY = 2.5)	0.7ns (-335) 0.75ns (-26A/-265) 0.8ns (-202)	70 75 80
11	MODULE CONFIGURATION TYPE	ECC	02
12	REFRESH RATE/TYPE	7.81µs /SELF	82
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	x4	04
14	ERROR-CHECKING SDRAM DATA WIDTH	x4	04
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	1 clock	01
16	BURST LENGTHS SUPPORTED	2, 4, 8	0E
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04
18	CAS LATENCIES SUPPORTED	2, 2.5	0C
19	CS LATENCY	0	01
20	WE LATENCY	1	02
21	SDRAM MODULE ATTRIBUTES	REGISTERED, PLL	26
22	SDRAM DEVICE ATTRIBUTES: GENERAL	Fast / Conconcurrent A/P	C0
23	SDRAM CYCLE TIME, (^{t}CK) (CAS LATENCY = 2)	7.5ns (-335/-26A) 10ns (-265/-202)	75 A0
24	SDRAM ACCESS FROM CK , (^{t}AC) (CAS LATENCY = 2)	0.7ns (-335) 0.75ns (-26A/-265) 0.8ns (-202)	70 75 80
25	SDRAM CYCLE TIME, (^{t}CK) (CAS LATENCY = 1.5)	N/A	00
26	SDRAM ACCESS FROM CK , (^{t}AC) (CAS LATENCY = 1.5)	N/A	00
27	MINIMUM ROW PRECHARGE TIME, (^{t}RP)	18ns (-335) 20ns (-26A/-265/-202)	48 50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (^{t}RRD)	12ns (-335) 15ns (-26A/-265/-202)	30 3C
29	MINIMUM RAS# TO CAS# DELAY, (^{t}RCD)	18ns (-335) 20ns (-26A/-265/-202)	48 50
30	MINIMUM ACTIVE TO PRECHARGE TIME, (^{t}RAS) (Note 3)	42ns (-335) 45ns (-26A/-265) 40ns (-202)	2A 2D 28

NOTE:
1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. Value for -26A ^{t}CK set to 7ns (0x70) for optimum BIOS compatibility. Actual device spec. value is 7.5ns.
3. The value of ^{t}RAS used for the -26A/-265 module is calculated from ^{t}RC- ^{t}RP. Actual device spec. value is 40ns.

SERIAL PRESENCE-DETECT MATRIX (continued)

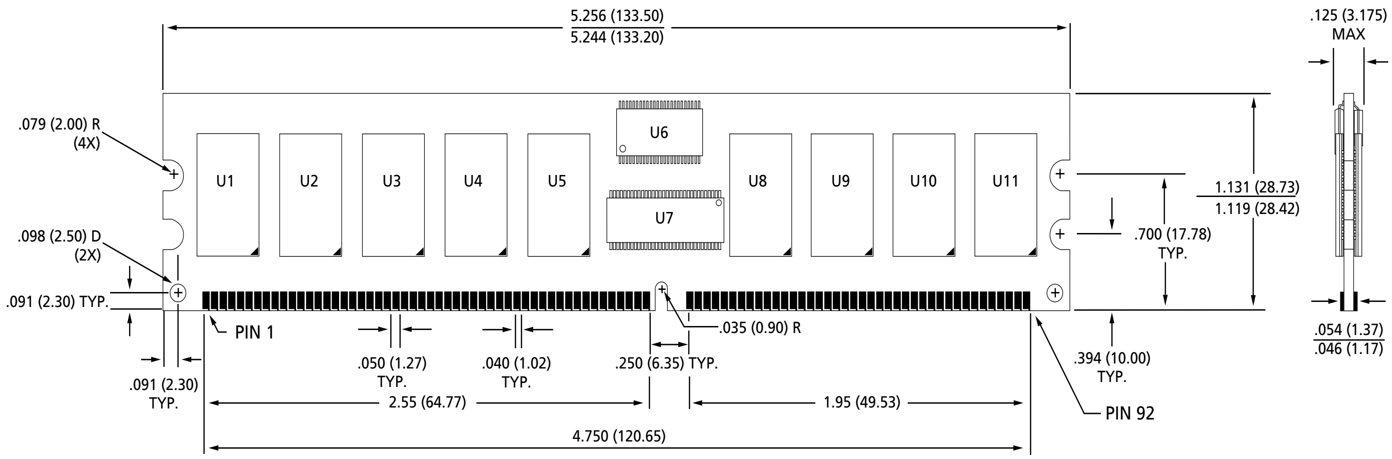
(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18VDDF6472G (Hex)
31	MODULE BANK DENSITY	512MB	80
32	ADDRESS AND COMMAND SETUP TIME, (^{t}IS) [Value set to slow slew rate (^{t}IS$_S$)] (Note: 2)	.80ns (-335) 1.0ns (-26A/-265) 1.1ns (-202)	80 A0 B0
33	ADDRESS AND COMMAND HOLD TIME, (^{t}IH) [Value set to slow slew rate (^{t}IH$_S$)] (Note: 2)	.80ns (-335) 1.0ns (-26A/-265) 1.1ns (-202)	80 A0 B0
34	DATA/DATA MASK INPUT SETUP TIME, (^{t}DS)	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	45 50 60
35	DATA/DATA MASK INPUT HOLD TIME, (^{t}DH)	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	45 50 60
36-40	RESERVED		00
41	MINIMUM ACTIVE/AUTO REFRESH TIME, (^{t}RC)	60ns (-335) 65ns (-26A/-265) 70ns (-202)	3C 41 46
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (^{t}RFC)	72ns (-335) 75ns (-26A/-265) 80ns (-202)	48 4B 50
43	MAXIMUM CYCLE TIME, (^{t}CK (MAX))	12ns (-335) 13ns (-26A/-265/-202)	30 34
44	MAXIMUM DQS-DQ SKEW TIME, (^{t}DQSQ)	0.35ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	23 32 3C
45	MAXIMUM READ DATA HOLD SKEW FACTOR, (^{t}QHS)	0.50ns (-335) 0.75ns (-26A/-265) 1.0ns (-202)	50 75 A0
46-61	RESERVED		00
62	SPD REVISION	Release 0.0	00
63	CHECKSUM FOR BYTES 0-62	-335 -26A -265 -202	58 27 57 F2
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C
65-71	MANUFACTURER'S JEDEC ID CODE (continued)		FF
72	MANUFACTURING LOCATION	1 - 11	01 - B0
73-90	MODULE PART NUMBER (ASCII)		x
91	PCB IDENTIFICATION CODE	1 - 9	01 -09
92	IDENTIFICATION CODE (continued)	0	00
93	YEAR OF MANUFACTURE IN BCD		x
94	WEEK OF MANUFACTURE IN BCD		x
95-98	MODULE SERIAL NUMBER		x
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		–

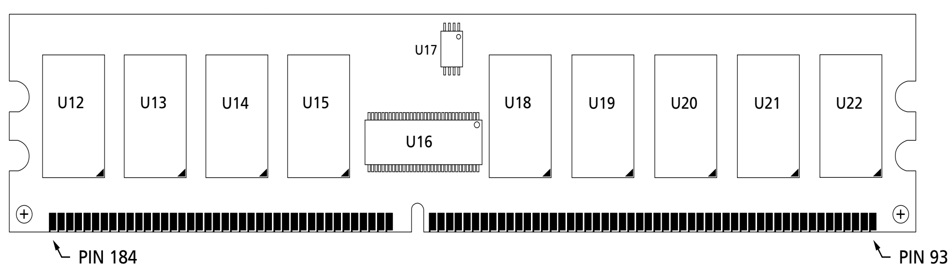
NOTE:
1. x = Variable Data.
2. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

184-PIN DIMM

FRONT VIEW



BACK VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATION

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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