

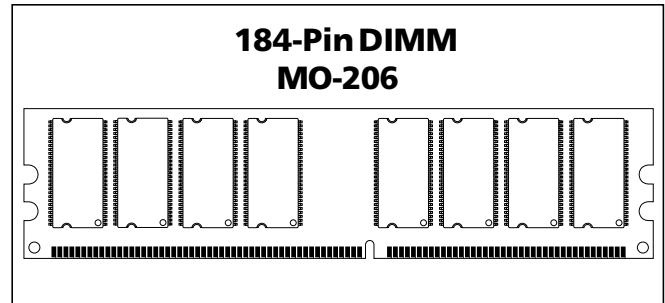
DDR SDRAM DIMM MODULE

MT16VDDT3264A - 256MB
MT16VDDT6464A - 512MB

For the latest data sheet, please refer to the Micron Web site: www.micron.com/modules

FEATURES

- 184-pin dual in-line memory module (DIMM)
- Fast data transfer rates PC1600, PC2100, or PC2700
- Utilizes 200 MT/s, 266 MT/s, and 333 MT/s DDR SDRAM components
- 256MB (32 Meg x 64) and 512MB (64 Meg x 64)
- $V_{DD} = V_{DDQ} = +2.5V \pm 0.2V$
- $V_{DDSPD} = +2.3V$ to $+3.6V$
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6 μ s (256MB), 7.8125 μ s (512MB) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold-plated edge contacts



OPTIONS

- Packages
184-pin DIMM (gold)
- Memory Clock/Speed, CAS Latency
6ns (167 MHz), 333 MT/s, CL = 2.5 -335
7.5ns (133 MHz), 266 MT/s, CL = 2 -26A
7.5ns (133 MHz), 266 MT/s, CL = 2.5 -265
10ns (100 MHz), 200 MT/s, CL = 2 -202

MARKING

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ADDRESS TABLE

	256MB	512MB
Refresh Count	4K	8K
Row Addressing	4K (A0–A11)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	16 Meg x 8	32 Meg x 8
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Bank Addressing	2 (S0#, S1#)	2 (S0#, S1#)

PART NUMBERS AND TIMING PARAMETERS

PART NUMBER	PART MARKING	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA RATE	LATENCY (CL - ^t RCD - ^t RP)
MT16VDDT3264AG-335__	-335	256MB	32 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT16VDDT3264AG-26A__	-26A	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT16VDDT3264AG-265__	-265	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT16VDDT3264AG-202__	-202	256MB	32 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2
MT16VDDT6464AG-335__	-335	512MB	64 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT16VDDT6464AG-26A__	-26A	512MB	64 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT16VDDT6464AG-265__	-265	512MB	64 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT16VDDT6464AG-202__	-202	512MB	64 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16VDDT6464AG-265A1

PIN ASSIGNMENT (184-Pin DIMM Front)

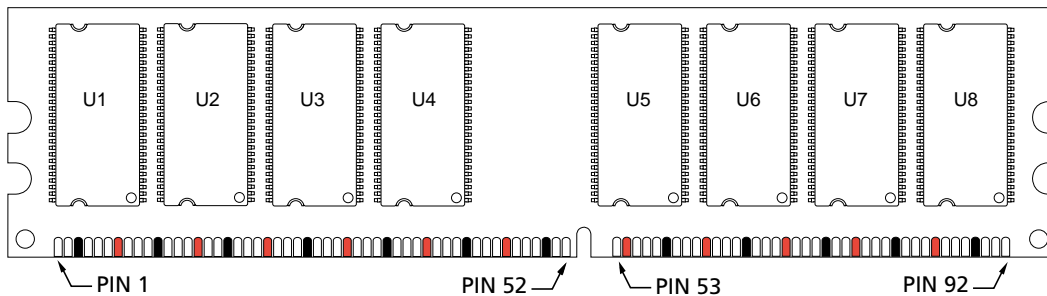
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DNU	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	DNU	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	DNU	74	VSS
6	DQ2	29	A7	52	BA1	75	CK2#
7	VDD	30	VDDQ	53	DQ32	76	CK2
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQ56
10	NC	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQ53	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	CK1	39	DQ26	62	VDDQ	85	VDD
17	CK1#	40	DQ27	63	WE#	86	DQ57
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	DNU	67	DQS5	90	NC
22	VDDQ	45	DNU	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

PIN ASSIGNMENT (184-Pin DIMM Back)

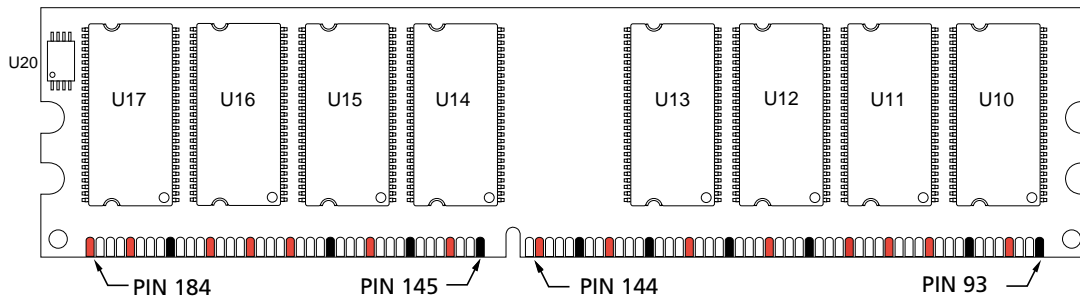
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DNU	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DQS11/DM2	142	DNU	165	DQ52
97	DQS9/DM0	120	VDD	143	VDD	166	DQ53
98	DQ6	121	DQ22	144	DNU	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15/DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13/DM4	172	VDDQ
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DQS12/DM3	152	VSS	175	DQ61
107	DQS10/DM1	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DQS16/DM7
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	CKE1	134	DNU	157	S0#	180	VDDQ
112	VDDQ	135	DNU	158	S1#	181	SA0
113	NC	136	VDDQ	159	DQS14/DM5	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	NC/A12*	138	CK0#	161	DQ46	184	VDDSPD

* Pin 115 is 'No Connect' for the 256MB module, or 'A12' for the 512MB module.

FRONT VIEW



BACK VIEW



█ Indicates a VDD and VDDQ pins █ Indicates a VSS pin

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	V _{REF}	Input	SSTL_2 reference voltage.
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
16, 17, 75, 76, 137, 138	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
21, 111	CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V _{DD} is applied.
157, 158	S0#, S1#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115 (512MB), 118, 122, 125, 130, 141	A0-A11 256MB A0-A12 512MB	Input	Address Inputs: A0-A11/A12 provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
91	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.

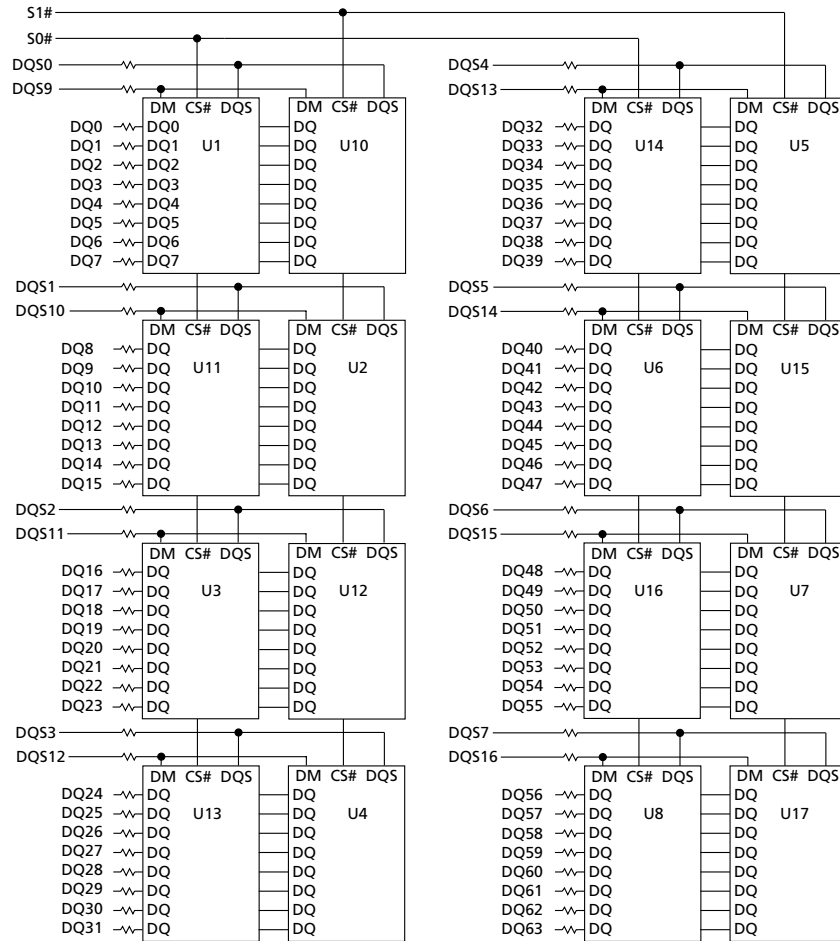
NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number and symbol information.

PIN DESCRIPTIONS (continued)

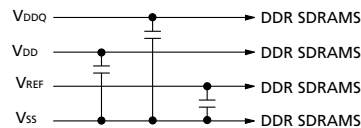
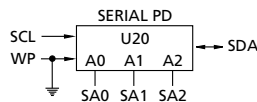
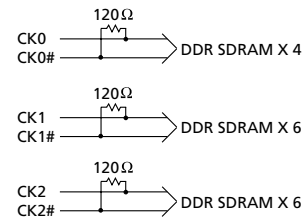
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
5, 14, 25, 36, 56, 67, 78, 86, 97, 107, 119, 129, 149, 159, 169, 177	DQS0-DQS16	Input/Output	<u>Data Strobe</u> : DQS0-DQS7, Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data. <u>Data Mask</u> : DQS9-DQS16 function as DM0-DM7 to mask WRITE data when HIGH.
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0-DQ63	Input/Output	Data I/Os: Data bus.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V _{DDQ}	Supply	DQ Power Supply: +2.5V \pm 0.2V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V _{DD}	Supply	Power Supply: +2.5V \pm 0.2V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V _{SS}	Supply	Ground.
184	V _{DDSPD}	Supply	Serial EEPROM positive power supply (+2.3V to +3.6V).
9, 10, 71, 82, 90, 101, 102, 103, 113, 115 (256MB), 163, 167, 173	NC	—	No Connect: These pins should be left unconnected.
44, 45, 47, 49, 51, 134, 135, 140, 142, 144	DNU	—	Do Not Use: These pins are not connected on this module but are assigned pins on other modules in this product family.

NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number and symbol information.

FUNCTIONAL BLOCK DIAGRAM



BA0, BA1 → BA0, BA1: DDR SDRAMS U1-U17
 A0-A11 (256MB) → A0-A11: DDR SDRAMS U1-U17
 A0-A12 (512MB) → A0-A12: DDR SDRAMS U1-U17
 RAS# → RAS#: DDR SDRAMS U1-U17
 CAS# → CAS#: DDR SDRAMS U1-U17
 CKE0 → CKE0: DDR SDRAMS BANK 0
 CKE1 → CKE1: DDR SDRAMS BANK 1
 WE# → WE#: DDR SDRAMS U1-U17



MT46V16M8TG DDR SDRAMS, 256MB Modules
 MT46V32M8TG DDR SDRAMS, 512MB Modules

- NOTE:**
- All resistor values are 22 ohms unless otherwise specified.
 - Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.
 - To optimize system and loading and signal integrity for -335 speed grade modules, 3Ω (single bank modules) or 5Ω (dual bank modules) stub resistors may be placed on command/address and control lines. Contact Micron CCG Applications for additional information.

GENERAL DESCRIPTION

The MT16VDDT3264A and MT16VDDT6464A are high-speed CMOS, dynamic random-access, 256MB and 512MB unbuffered memory modules organized in a x64 configuration. These modules use internally configured quad-bank DDR SDRAM devices.

These DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single $2n$ -bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

These DDR SDRAM modules operate from multiple differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select devices bank; A0-A11 select device row for the 256MB module, A0-A12 select device row for the 512MB module). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

These DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb and 256Mb DDR SDRAM data sheets.

SERIAL PRESENCE-DETECT OPERATION

These DDR SDRAM modules incorporate presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

REGISTER DEFINITION

MODE REGISTER

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in the Mode Register Diagram. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A11 (for the 256MB module) or A7-A12 (for the 512MB module) specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Diagram. The burst length determines the maximum number of column locations

that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A_i when the burst length is set to two, by A2-A_i when the burst length is set to four and by A3-A_i when the burst length is set to eight (where A_i is the

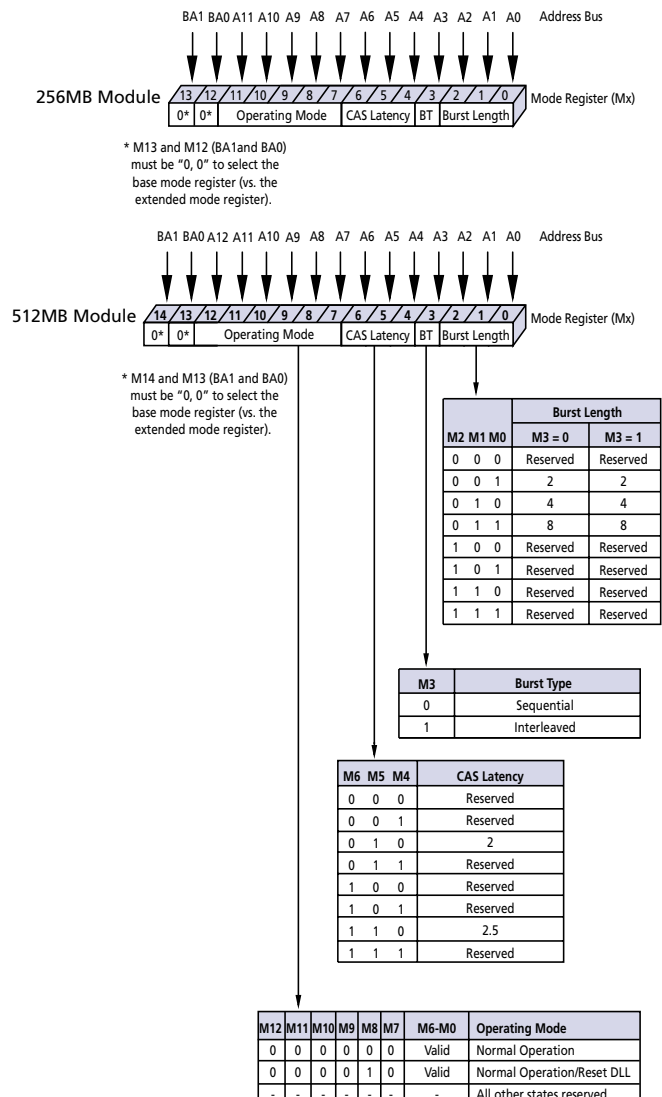
most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table.

Mode Register Definition Diagram



Burst Definition Table

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

- NOTE:**
- For a burst length of two, A1-A_i select the two-data-element block; A0 selects the first access within the block.
 - For a burst length of four, A2-A_i select the four-data-element block; A0-A1 select the first access within the block.
 - For a burst length of eight, A3-A_i select the eight-data-element block; A0-A2 select the first access within the block.
 - Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

$i = 11$ for 256MB module, or 12 for 512MB module

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in CAS Latency Diagram.

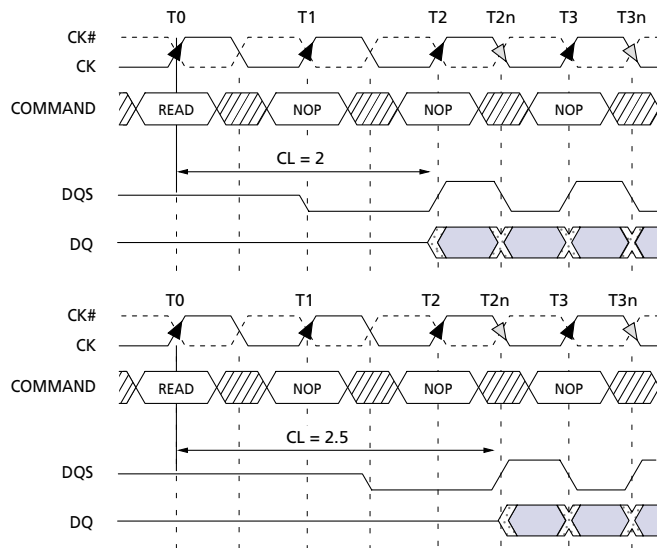
If a READ command is registered at clock edge n , and the latency is m clocks, the data will be available nominally coincident with clock edge $n + m$. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

**CAS Latency (CL)
Table**

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CL = 2	CL = 2.5
-335	NA	$83 \leq f \leq 167$
-26A	$83 \leq f \leq 133$	$83 \leq f \leq 133$
-265	$83 \leq f \leq 100$	$83 \leq f \leq 133$
-202	$83 \leq f \leq 100$	$83 \leq f \leq 125$

CAS Latency Diagram



Burst Length = 4 in the cases shown
Shown with nominal t_{AC} and nominal t_{DSDQ}

TRANSITIONING DATA DON'T CARE

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A11 (for the 256MB module), or A7-A12 (for the 512MB module) each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9-A11 (for 256MB module), or A7 and A9-A12 (for 512MB module) each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A11, or A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

EXTENDED MODE REGISTER

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in the Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

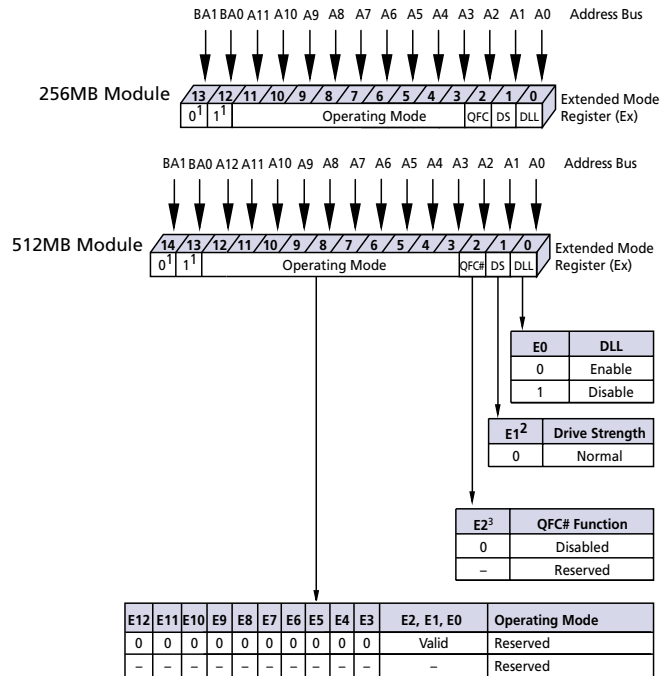
Output Drive Strength

The normal full drive strength for all outputs is specified to be SSTL2, Class II. For detailed information on output drive strength option, refer to 128Mb and 256Mb DDR SDRAM data sheets.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Extended Mode Register Definition Diagram



NOTE: 1. E13 and E12 (256MB module), or E14 and E13 (512MB Module) (BA1 and BA0) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

COMMANDS

The Truth Tables below provides a general reference of available commands. For a more detailed description

of commands and operations, refer to the 128Mb and 256Mb DDR SDRAM data sheets.

TRUTH TABLE – COMMANDS

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

TRUTH TABLE – DM OPERATION

(Note: 10)

NAME (FUNCTION)	DM	DQ
WRITE Enable	L	Valid
WRITE Inhibit	H	X

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
 2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A11 (for 256MB module) or A0-A12 (for 512MB module) provide the op-code to be written to the selected mode register.
 3. BA0-BA1 provide device bank address and A0-A11 (256MB) or A0-A12 (512MB) provide device row address.
 4. BA0-BA1 provide device bank address; A0-A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
 5. A10 LOW: BA0-BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0-BA1 are "Don't Care."
 6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
 7. Internal refresh counter controls device row addressing; all inputs and I/Os are "Don't Care" except for CKE.
 8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
 9. Deselect and NOP are functionally interchangeable.
 10. Used to mask write data; provided coincident with the corresponding data.



256MB, 512MB (x64) 184-PIN DDR SDRAM DIMMs

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{DD} Supply	
Relative to V _{SS}	-1V to +3.6V
Voltage on V _{DDQ} Supply	
Relative to V _{SS}	-1V to +3.6V
Voltage on V _{REF} and Inputs	
Relative to V _{SS}	-1V to +3.6V
Voltage on I/O Pins	
Relative to V _{SS}	-0.5V to V _{DDQ} +0.5V
Operating Temperature, T _A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	16W
Short Circuit Output Current	50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1–5, 14; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage	V _{DD}	2.3	2.7	V	32, 36	
I/O Supply Voltage	V _{DDQ}	2.3	2.7	V	32, 36 39	
I/O Reference Voltage	V _{REF}	0.49 × V _{DDQ}	0.51 × V _{DDQ}	V	6, 39	
I/O Termination Voltage (system)	V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V	7, 39	
Input High (Logic 1) Voltage	V _{IH(DC)}	V _{REF} + 0.15	V _{DD} + 0.3	V	25	
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.3	V _{REF} - 0.15	V	25	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{DD} , V _{REF} pin 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	Command/ Address	I _I	-32	32	μA	48
	CKE0/CKE1 S0#, S1#		-16	16		
	CK0/CK0#		-8	8		
	CK1/CK1#, CK2/CK2#		-12	12		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ})	I _{OZ}	-10	10	μA	48	
OUTPUT LEVELS: High Current (V _{OUT} = V _{DDQ} -0.373V, minimum V _{REF} , minimum V _{TT}) Low Current (V _{OUT} = 0.373V, maximum V _{REF} , maximum V _{TT})	I _{OH}	-16.8	–	mA	33, 34	
	I _{OL}	16.8	–	mA		

AC INPUT OPERATING CONDITIONS

(Notes: 1–5, 14; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V _{IH(AC)}	V _{REF} + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	V _{IL(AC)}	–	V _{REF} - 0.310	V	12, 25, 35
I/O Reference Voltage	V _{REF(AC)}	0.49 × V _{DDQ}	0.51 × V _{DDQ}	V	6

I_{DD} SPECIFICATIONS AND CONDITIONS* (256MB MODULE)

(Notes: 1–5, 8, 10, 12; notes appear following parameter tables)

 (0°C ≤ T_A ≤ +70°C; V_{DDQ} = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER/CONDITION	SYM	MAX			UNITS	NOTES	
		-335	-26A/-265	-202			
OPERATING CURRENT: One device bank; Active-Precharge; ^t RC = ^t RC (MIN); ^t CK = ^t CK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0} ^a	TBD	864	824	mA	20, 43	
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; ^t RC = ^t RC (MIN); ^t CK = ^t CK (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1} ^a	TBD	984	904	mA	20, 43	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^t CK = ^t CK (MIN); CKE = LOW;	I _{DD2P} ^b	TBD	48	48	mA	21, 28, 45	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^t CK = ^t CK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2F} ^b	TBD	720	560	mA	46	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^t CK = ^t CK (MIN); CKE = LOW	I _{DD3P} ^b	TBD	288	288	mA	21, 28, 45	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^t RC = ^t RAS (MAX); ^t CK = ^t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N} ^b	TBD	720	560	mA	42	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^t CK = ^t CK (MIN); I _{OUT} = 0mA	I _{DD4R} ^a	TBD	904	744	mA	20, 43	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^t CK = ^t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W} ^a	TBD	904	744	mA	20	
AUTO REFRESH CURRENT	^t RC = ^t RFC (MIN)	I _{DD5} ^b	TBD	3,520	3,280	mA	20, 45
	^t RC = 15.625μs	I _{DD5A} ^b	TBD	80	80	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V	I _{DD6} ^b	TBD	32	48	mA	9	
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, ^t RC = minimum ^t RC allowed; ^t CK = ^t CK (MIN); Address and control inputs change only during Active, READ, or WRITE commands.	I _{DD7} ^a	TBD	2,624	2,104	mA	20, 44	

*DRAM components only

 a - Value calculated as one module bank in this operating condition, and all other banks in I_{DD2P}, power-down mode.

b - Value calculated reflects all module banks in this operating condition.

I_{DD} SPECIFICATIONS AND CONDITIONS* (512MB MODULE)

(Notes: 1-5, 8, 10, 12; notes appear following parameter tables)
(0°C ≤ T_A ≤ +70°C; V_{DDQ} = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER/CONDITION	SYM	MAX			UNITS	NOTES	
		-335	-26A/-265	-202			
OPERATING CURRENT: One device bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0} ^a	TBD	TBD	TBD	mA	20, 43	
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1} ^a	TBD	TBD	TBD	mA	20, 43	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = (LOW)	I _{DD2P} ^b	TBD	TBD	TBD	mA	21, 28, 45	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2P} ^b	TBD	TBD	TBD	mA	46	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW	I _{DD3P} ^b	TBD	TBD	TBD	mA	21, 28, 45	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N} ^b	TBD	TBD	TBD	mA	42	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; I _{OUT} = 0mA	I _{DD4R} ^a	TBD	TBD	TBD	mA	20, 43	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W} ^a	TBD	TBD	TBD	mA	20	
AUTO REFRESH CURRENT	$t_{RFC} = t_{RFC}(\text{MIN})$	I _{DD5} ^b	TBD	TBD	TBD	mA	20, 45
	$t_{RC} = 7.8125\mu\text{s}$	I _{DD5A} ^b	TBD	TBD	TBD	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V	I _{DD8} ^b	TBD	TBD	TBD	mA	9	
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, $t_{RC} = \text{minimum } t_{RC}$ allowed; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during Active READ, or WRITE commands.	I _{DD7} ^a	TBD	TBD	TBD	mA	20, 44	

*DRAM components only

a - Value calculated as one module bank in this operating condition, and all other banks in I_{DD2P}, power-down mode.

b - Value calculated reflects all module banks in this operating condition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS*

(Notes: 1–5, 12–15, 29; notes appear following parameter tables)

 (0°C ≤ T_A ≤ +70°C; V_{DDQ} = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

AC CHARACTERISTICS		-335		-26A/-265		-202		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Access window of DQs from CK/CK#	t ^{AC}	-0.70	+0.70	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width	t ^{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t ^{CK}	26
CK low-level width	t ^{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t ^{CK}	26
Clock cycle time	CL = 2.5 t ^{CK} (2.5)	6	12	7.5	13	8	13	ns	40, 47
	CL = 2 t ^{CK} (2)	7.5	12	7.5/10	13	10	13	ns	40, 47
DQ and DM input hold time relative to DQS	t ^{DH}	0.45		0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS	t ^{DS}	0.45		0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)	t ^{DIPW}	1.75		1.75		2		ns	27
Access window of DQS from CK/CK#	t ^{DQSCK}	-0.60	+0.60	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width	t ^{DQSH}	0.35		0.35		0.35		t ^{CK}	
DQS input low pulse width	t ^{DQSL}	0.35		0.35		0.35		t ^{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access	t ^{DQSQ}		0.45		0.5		0.6	ns	22, 23
Write command to first DQS latching transition	t ^{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t ^{CK}	
DQS falling edge to CK rising - setup time	t ^{DSS}	0.2		0.2		0.2		t ^{CK}	
DQS falling edge from CK rising - hold time	t ^{DSH}	0.2		0.2		0.2		t ^{CK}	
Half clock period	t ^{HP}	t ^{CH} , t ^{CL}		t ^{CH} , t ^{CL}		t ^{CH} , t ^{CL}		ns	30
Data-out high-impedance window from CK/CK#	t ^{HZ}		+0.70		+0.75		+0.8	ns	16, 37
Data-out low-impedance window from CK/CK#	t ^{LZ}	-0.70		-0.75		-0.8		ns	16, 38
Address and control input hold time (fast slew rate)	t ^{IH_f}	0.75		0.90		1.1		ns	12
Address and control input setup time (fast slew rate)	t ^{IS_f}	0.75		0.90		1.1		ns	12
Address and control input hold time (slow slew rate)	t ^{IH_s}	0.80		1		1.1		ns	12
Address and control input setup time (slow slew rate)	t ^{IS_s}	0.80		1		1.1		ns	12
LOAD MODE REGISTER command cycle time	t ^{MRD}	12		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t ^{HP} -t ^{QHS}		t ^{HP} -t ^{QHS}		t ^{HP} -t ^{QHS}		ns	22, 23
Data hold skew factor	t ^{QHS}		0.60		0.75		1	ns	
ACTIVE to PRECHARGE command	t ^{RAS}	42	70,000	40	120,000	40	120,000	ns	31
ACTIVE to READ with auto precharge command, (256MB Modules)	t ^{RAP}	18		t ^{RAS} (MIN) - (burst length * t ^{CK} /2)				ns	41
ACTIVE to READ with auto precharge command, (512MB Modules)	t ^{RAP}	18		20		20		ns	41
ACTIVE to ACTIVE/AUTO REFRESH command period	t ^{RC}	60		65		70		ns	
AUTO REFRESH command period	t ^{RFC}	72		75		80		ns	45
ACTIVE to READ or WRITE delay	t ^{RCD}	18		20		20		ns	
PRECHARGE command period	t ^{RP}	18		20		20		ns	
DQS read preamble	t ^{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t ^{CK}	37
DQS read postamble	t ^{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t ^{CK}	
ACTIVE bank a to ACTIVE bank b command	t ^{RRD}	12		15		15		ns	
DQS write preamble	t ^{WPRE}	0.25		0.25		0.25		t ^{CK}	
DQS write preamble setup time	t ^{WPRES}	0		0		0		ns	18, 19
DQS write postamble	t ^{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t ^{CK}	17
Write recovery time	t ^{WR}	15		15		15		ns	
Internal WRITE to READ command delay	t ^{WTR}	1		1		1		t ^{CK}	

*Module AC timing parameters comply with PC1600, PC2100, and PC2700 design specifications, based on DDR SDRAM component performance parameters.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS*

(Notes: 1–5, 12–15, 29; notes appear following parameter tables)
($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{\text{DDQ}} = +2.5\text{V} \pm 0.2\text{V}$, $V_{\text{DD}} = +2.5\text{V} \pm 0.2\text{V}$)

AC CHARACTERISTICS		-335		-26A/-265		-202			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Data valid output window	na	$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		ns	22
REFRESH to REFRESH command interval (256MB)	t_{REFC}		140.6		140.6		140.6	μs	21
REFRESH to REFRESH command interval (512MB)	t_{REFC}		70.3		70.3		70.3	μs	21
Average periodic refresh interval (256MB)	t_{REFI}		15.6		15.6		15.6	μs	21
Average periodic refresh interval (512MB)	t_{REFI}		7.8		7.8		7.8	μs	21
Terminating voltage delay to V_{DD}	t_{VTD}	0		0		0		ns	
Exit SELF REFRESH to non-READ command	t_{XSNR}	75		75		80		ns	
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		t_{CK}	

* - Module AC timing parameters comply with PC 2700, PC2100, and PC1600 design specifications, based on DDR SDRAM component performance parameters.

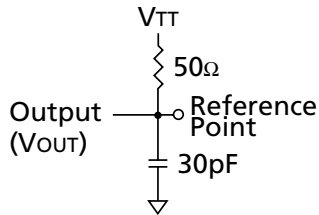
CAPACITANCE (All Modules)

(Note: 11; notes appear following parameter tables)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C_{IO}	8.0	10.0	pF
Input Capacitance: Command and Address	C_{I1}	32.0	48.0	pF
Input Capacitance: S0#, S1#	C_{I2}	16.0	24.0	pF
Input Capacitance: CK0, CK0#	C_{I3a}	8.0	12.0	pF
Input Capacitance: CK1, CK1#, CK2, CK2#	C_{I3b}	12.0	18.0	pF
Input Capacitance: CKE0, CKE1	C_{I4}	16.0	24.0	pF

NOTES

1. All voltages referenced to V_{SS} .
2. Tests for AC timing, I_{DD} , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:

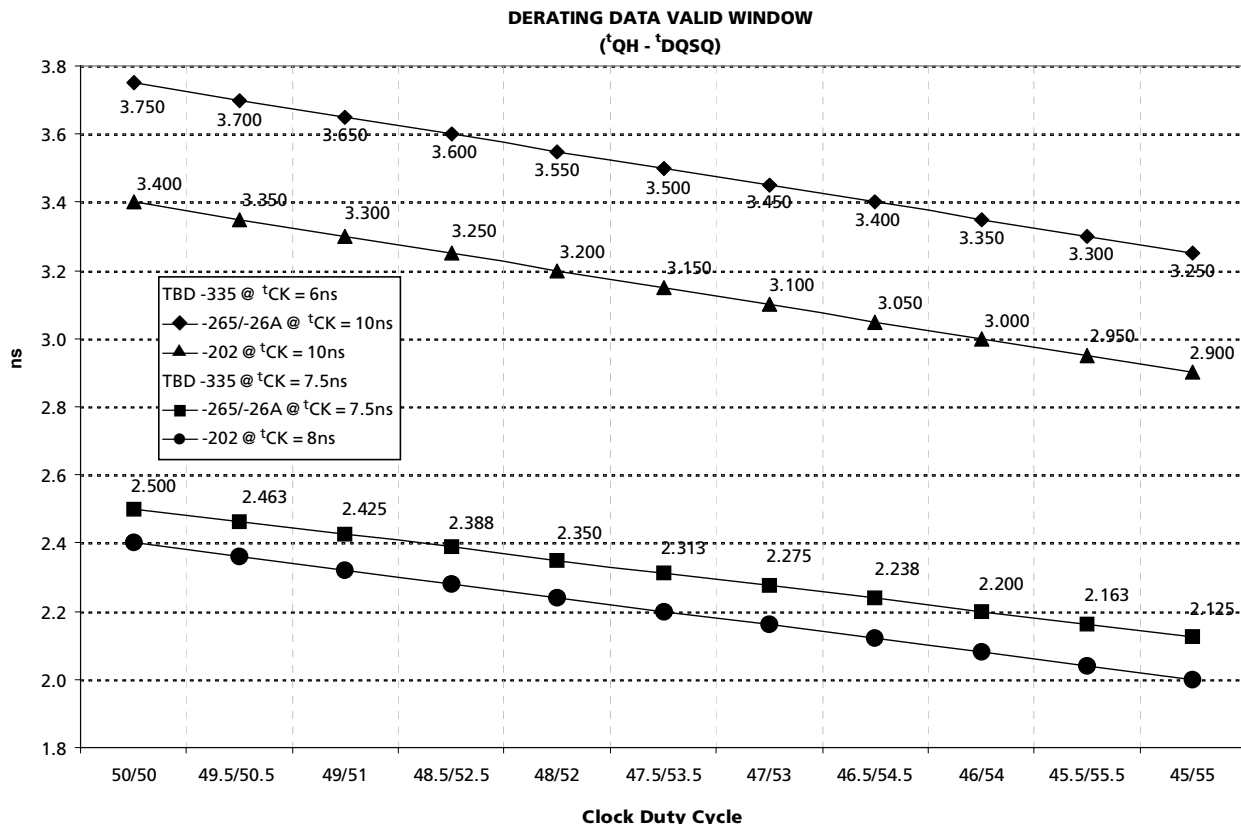


4. AC timing and I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ± 2 percent of the DC value. Thus, from $V_{DDQ}/2$, V_{REF} is allowed ± 25 mV for DC error and an additional ± 25 mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF} .
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at $CL = 2$ for -26A and -202, $CL = 2.5$ for -335 and -265 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.

11. This parameter is sampled. $V_{DD} = +2.5V \pm 0.2V$, $V_{DDQ} = +2.5V \pm 0.2V$, $V_{REF} = V_{SS}$, $f = 100$ MHz, $T_A = 25^\circ C$, $V_{OUT(DC)} = V_{DDQ}/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -265 with slew rates 1V/ns and faster, t_{IS} and t_{IH} are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. t_{IH} has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF} .
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, $CKE \leq 0.3 \times V_{DDQ}$ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT} .
16. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DQSS} .
20. MIN (t_{RC} or t_{RFC}) for I_{DD} measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for I_{DD} measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS} .

NOTES (continued)

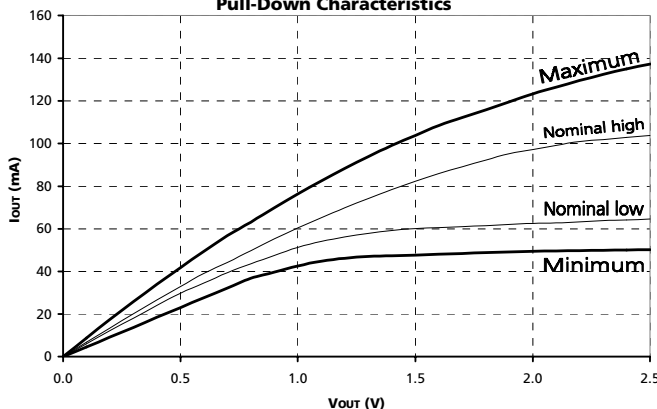
21. The refresh period 64ms. This equates to an average refresh rate of 15.625 μ s (256MB modules), or 7.821 μ s (512MB modules). However, an AUTO REFRESH command must be asserted at least once every 140.6 μ s (256MB modules) or 70.3 μ s (512MB modules); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications - t_{HP} ($t_{CK}/2$), t_{DQSQ} , and t_{QH} ($t_{QH} = t_{HP} - t_{QHS}$). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
23. Referenced to each output group: x8 = DQS with DQ0-DQ7.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (t_{RFC} [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
 - a) Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
 - b) Reach at least the target AC level.
 - c) After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
26. JEDEC specifies CK and CK# input slew rate must be $\geq 1V/ns$ (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.



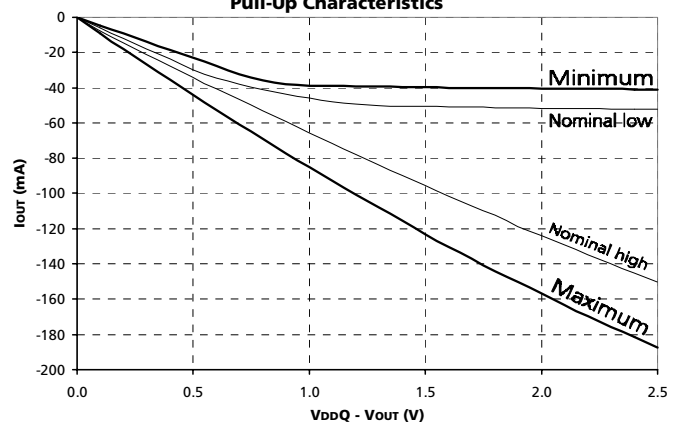
NOTES (continued)

28. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
29. The clock is allowed up to ± 150 ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. t_{HP} min is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until $t_{RAS(MIN)}$ can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch must be less than $1/3$ of the clock and not more than +400mV or 2.9 volts, whichever is less. Any negative glitch must be less than $1/3$ of the clock cycle and not exceed either -300mV or 2.2 volts, whichever is more positive.
33. Normal Output Drive Curves:
 - a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure A.
 - b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure A.
 - c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure B.
 - d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure B.
 - e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 Volt, and at the same voltage and temperature.
 - f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity $\pm 10\%$, for device drain-to-source voltages from 0.1V to 1.0 Volt.
34. The voltage levels used are derived from a minimum V_{DD} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. V_{IH} overshoot: $V_{IH(MAX)} = V_{DDQ} + 1.5V$ for a pulse width ≤ 3 ns and the pulse width can not be greater than $1/3$ of the cycle rate. V_{IL} undershoot: $V_{IL(MIN)} = -1.5V$ for a pulse width ≤ 3 ns and the pulse width can not be greater than $1/3$ of the cycle rate.
36. V_{DD} and V_{DDQ} must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for $t_{HZ(MAX)}$ and the last DVW. $t_{HZ(MAX)}$ will prevail over $t_{DQCK(MAX)} + t_{RPST(MAX)}$ condition. $t_{LZ(MIN)}$ will prevail over $t_{DQCK(MIN)} + t_{RPRE(MAX)}$ condition.
38. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, V_{DDQ} , V_{TT} , and V_{REF} must be equal to or less than $V_{DD} + 0.3V$. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{DD}/V_{DDQ} are 0 volts, provided a minimum of 42 ohms of series resistance is used between the V_{TT} supply and the input pin.

**Figure A
Pull-Down Characteristics**



**Figure B
Pull-Up Characteristics**



NOTES (continued)

40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. $t_{RAP} \geq t_{RCD}$.
42. For the -335, -265 and -26A modules, I_{DD3N} is specified to be 35mA at 100 MHz.
43. Random addressing changing 50% of data changing at every transfer.
44. Random addressing changing 100% of data changing at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{REF} later.
46. I_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. I_{DD2Q} is similar to I_{DD2F} except I_{DD2Q} specifies the address and control inputs to remain stable. Although I_{DD2F} , I_{DD2N} , and I_{DD2Q} are similar, I_{DD2F} is "worst case."
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
48. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

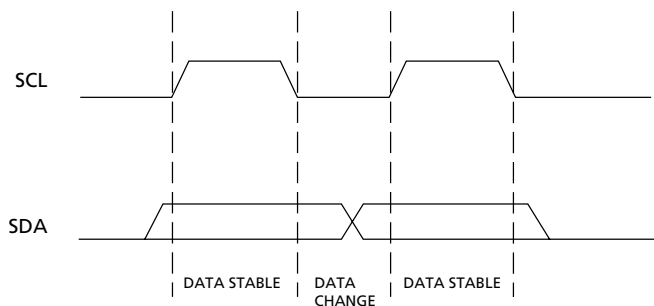
All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

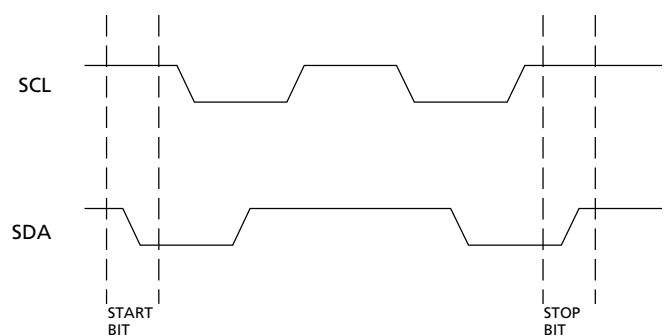
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

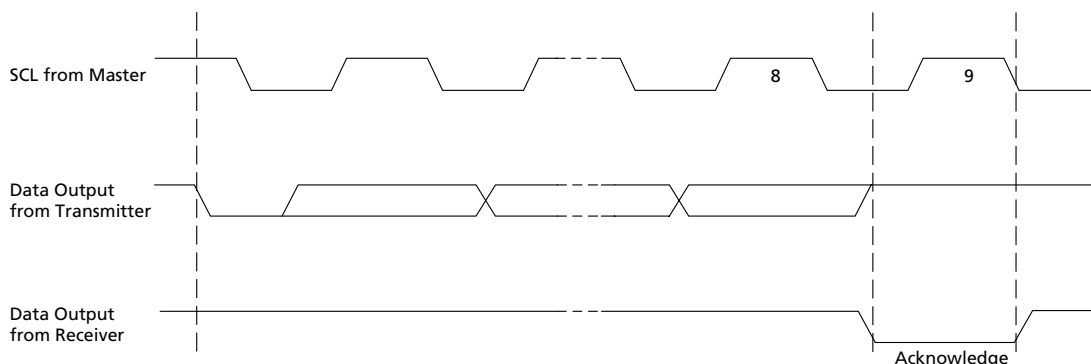
**Figure 1
Data Validity**



**Figure 2
Definition of Start and Stop**



**Figure 3
Acknowledge Response From Receiver**



EEPROM DEVICE SELECT CODE

Note: The most significant bit (b7) is sent first.

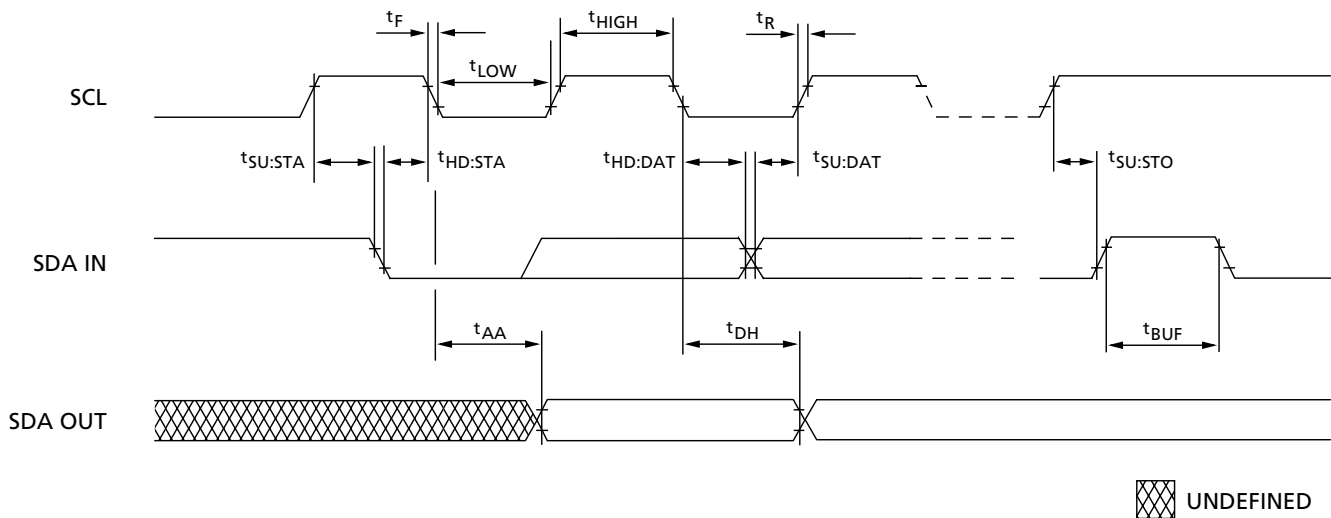
	DEVICE TYPE IDENTIFIER				CHIP ENABLE			R \overline{W}
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	R \overline{W}
Protection Register Select Code	0	1	1	0	E2	E1	E0	R \overline{W}

EEPROM OPERATING MODES

MODE	R \overline{W} BIT	WC ¹	BYTES	INITIAL SEQUENCE
Current Address Read	1	X	1	START, Device Select, R \overline{W} = '1'
Random Address Read	0	X	1	START, Device Select, R \overline{W} = '0', Address
	1	X	1	reSTART, Device Select, R \overline{W} = '1'
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V _{IL}	1	START, Device Select, R \overline{W} = '0'
Page Write	0	V _{IL}	≤ 16	START, Device Select, R \overline{W} = '0'

NOTE: 1. X = V_{IH} or V_{IL}.

SPD EEPROM TIMING DIAGRAM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	μ s
t_{BUF}	4.7		μ s
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		μ s
$t_{HD:STA}$	4		μ s

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		μ s
t_{LOW}	4.7		μ s
t_R		1	μ s
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		μ s
$t_{SU:STO}$	4.7		μ s

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

 (Note: 1) ($V_{DDSPD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 0.5$	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DDSPD} \times 0.3$	V
OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$	V_{OL}	-	0.4	V
INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to V_{DDSPD}	I_{LI}	-	10	μA
OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to V_{DDSPD}	I_{LO}	-	10	μA
STANDBY CURRENT: SCL = SDA = $V_{DD} - 0.3V$; All other inputs = GND or 3.3V +10%	I_{SB}	-	30	μA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	-	2	mA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

 (Notes: 1) ($V_{DDSPD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		μs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_F		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		μs	
Start condition hold time	$t_{HD:STA}$	4		μs	
Clock HIGH period	t_{HIGH}	4		μs	
Noise suppression time constant at SCL, SDA inputs	t_I		100	ns	
Clock LOW period	t_{LOW}	4.7		μs	
SDA and SCL rise time	t_R		1	μs	
SCL clock frequency	t_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		μs	
Stop condition setup time	$t_{SU:STO}$	4.7		μs	
WRITE cycle time	t_{WRC}		10	ms	2

NOTE: 1. All voltages referenced to V_{SS} .

 2. The refresh period is 64ms. This equates to an average refresh rate of 15.625 μs . However, an AUTO REFRESH command must be asserted at least once every 31.2 μs ; burst refreshing or postings greater than 2 are not allowed.



SERIAL PRESENCE-DETECT MATRIX

(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT16VDDT3264A	MT16VDDT6464A
0	NUMBER OF BYTES USED BY MICRON	128	80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	08
2	MEMORY TYPE	SDRAMDDR	07	07
3	NUMBER OF ROW ADDRESSES	12 or 13	0C	0D
4	NUMBER OF COLUMN ADDRESSES	10	0A	0A
5	NUMBER OF BANKS	2	02	02
6	MODULE DATA WIDTH	64	40	40
7	MODULE DATA WIDTH (continued)	0	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	SSTL 2.5V	04	04
9	SDRAM CYCLE TIME, ^t CK (CAS LATENCY = 2.5) (Note 2)	6ns (-335) 7ns (-26A) 7.5ns (-265) 8ns (-202)	60 70 75 80	60 70 75 80
10	SDRAM ACCESS FROM CLOCK, ^t AC (CAS LATENCY = 2.5)	0.70ns (-335) 0.75ns (-26A/-265) 0.8ns (-202)	70 75 80	70 75 80
11	MODULE CONFIGURATION TYPE	None	00	00
12	REFRESH RATE/TYPE	15.6 or 7.81µs/SELF	80	82
13	SDRAM WIDTH (PRIMARY SDRAM)	8	08	08
14	ERROR-CHECKING SDRAM DATA WIDTH	None	00	00
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	1	01	01
16	BURST LENGTHS SUPPORTED	2, 4, 8	0E	0E
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	04
18	CAS LATENCIES SUPPORTED	2, 2.5	0C	0C
19	CS LATENCY	0	01	01
20	WE LATENCY	1	02	02
21	SDRAM MODULE ATTRIBUTES		20	20
22	SDRAM DEVICE ATTRIBUTES: GENERAL	Fast / Concurrent Auto Precharge	00/C0*	C0
23	SDRAM CYCLE TIME, ^t CK (CAS LATENCY = 2)	7.5ns (-335/-26A) 10 ns (-265/-202)	75 A0	75 A0
24	SDRAM CYCLE TIME, ^t CK (CAS LATENCY = 2)	7ns (-335) 7.5ns (-26A/-265) 8ns (-202)	70 75 80	70 75 80
25	SDRAM CYCLE TIME, ^t CK (CAS LATENCY = 1)	-	00	00
26	SDRAM ACCESS FROM CK, ^t AC (CAS LATENCY = 1)	-	00	00
27	MINIMUM ROW PRECHARGE TIME, ^t RP	18ns (-335) 20ns (-26A/-265/-202)	48 50	48 50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^t RRD	12ns (-335) 15ns (-26A/-265/-202)	30 3C	30 3C
29	MINIMUM RAS# TO CAS# DELAY, ^t RCD	18ns (-335) 20ns (-26A/-265/-202)	48 50	48 50

*Supports Fast/Concurrent Auto Precharge. Contact Factory for additional information regarding this option.

- NOTE:**
1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
 2. Value for -26A ^tCK set to 7ns (0x70) for optimum BIOS compatibility. Actual device spec. value is 7.5ns.

SERIAL PRESENCE-DETECT MATRIX (continued)

(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT16VDDT3264A	MT16VDDT6464A
30	MINIMUM RAS# PULSE WIDTH, ^t RAS (Note 3)	42ns (-335) 45ns (-26A/-265) 40ns (-202)	2A 2D 28	2A 2D 28
31	MODULE BANK DENSITY	128MB or 256MB	20	40
32	ADDRESS AND COMMAND SETUP TIME, ^t IS [Value set to slow slew rate (^t IS _s)] (Note 4)	0.8ns (-335) 1.0ns (-26A/-265) 1.1ns (-202)	80 A0 B0	80 A0 B0
33	ADDRESS AND COMMAND HOLD TIME, ^t IH [Value set to slow slew rate (^t IH _s)] (Note 4)	0.8ns (-335) 1.0ns (-26A/-265) 1.1ns (-202)	80 A0 B0	80 A0 B0
34	DATA/DATA MASK INPUT SETUP TIME, ^t DS	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	45 50 60	45 50 60
35	DATA/DATA MASK INPUT HOLD TIME, ^t DH	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	45 50 60	45 50 60
36-40	RESERVED		00	00
41	MINIMUM ACTIVE/AUTO REFRESH TIME, (^t RC)	60ns (-335) 65ns (-26A/-265) 70ns (-202)	3C 41 46	3C 41 46
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (^t RFC)	72ns (-335) 75ns (-26A/-265) 80ns (-202)	48 4B 50	48 4B 50
43	MAXIMUM CYCLE TIME, (^t CK (MAX))	12ns (-335) 13ns (-26A/-265/-202)	30 34	30 34
44	MAXIMUM DQS-DQ SKEW TIME, (^t DQSQ)	0.45ns (-335) 0.5ns (-26A/-265) 0.6ns (-202)	2D 32 3C	2D 32 3C
45	MAXIMUM READ DATA HOLD SKEW FACTOR, (^t QHS)	0.60ns (-335) 0.75ns (-26A/-265) 1ns (-202)	60 75 A0	60 75 A0
46-61	RESERVED		00	00
62	SPD REVISION	Release 0.0	00	00
63	CHECKSUM FOR BYTES 0-62	-335 -26A -265 -202	na/FF* F4/B4* 24/E4* BF/7F*	22 D7 07 A2
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE	(continued)	FF	FF
72	MANUFACTURING LOCATION	1 - 11	01 - 0B	01 - 0B
73-90	MODULE PART NUMBER (ASCII)		x	x
91	PCB IDENTIFICATION CODE	1 - 9	01 - 09	01 - 09

*Supports Fast/Concurrent Auto Precharge. Contact Factory for additional information regarding this option.

- NOTE:**
1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
 2. x = Variable Data.
 3. The value of ^tRAS for -26A and -265 modules is calculated from ^tRC - ^tRP. Actual device spec is 40ns.
 4. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

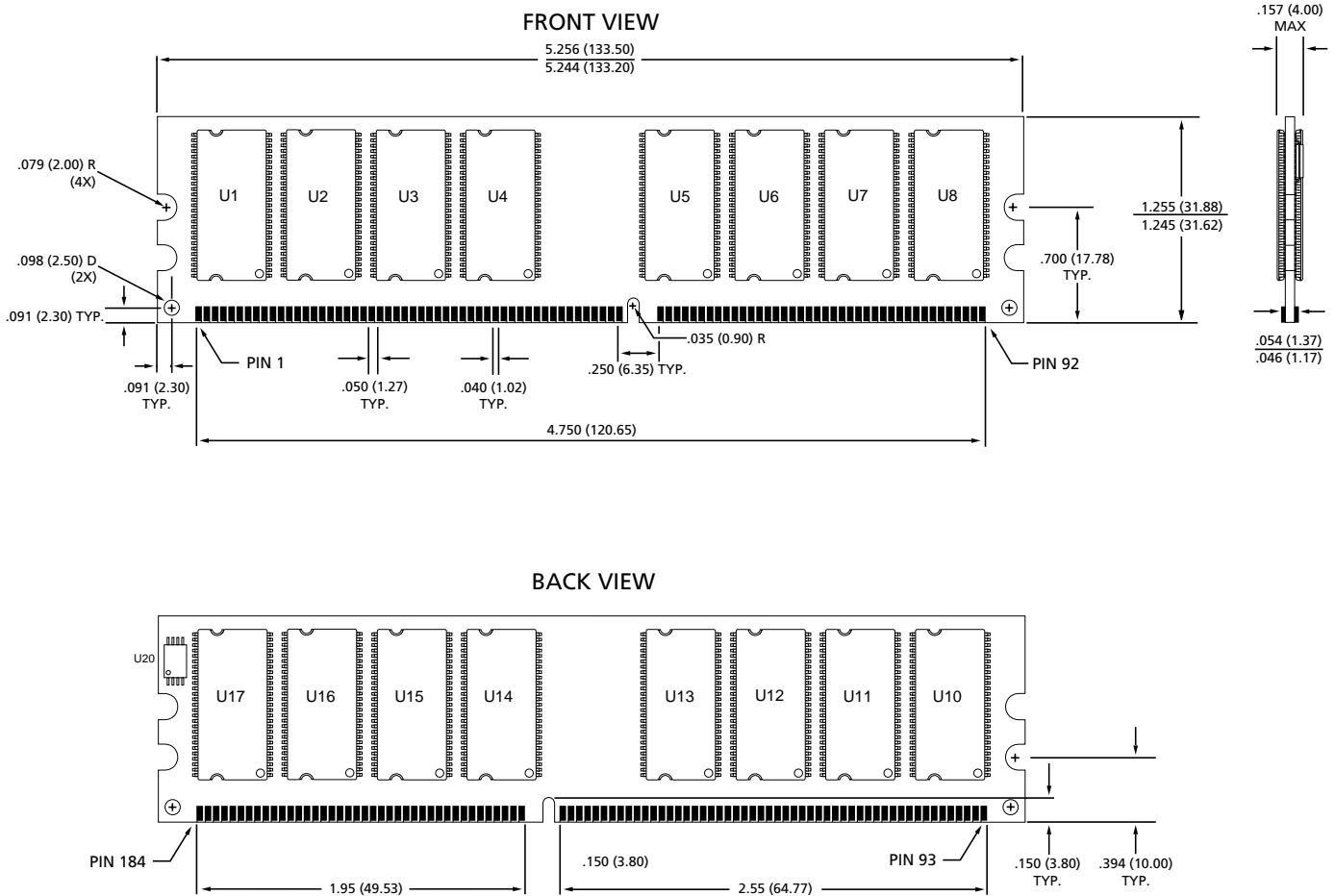
SERIAL PRESENCE-DETECT MATRIX (continued)

(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT16VDDT3264A	MT16VDDT6464A
92	IDENTIFICATION CODE (continued)	0	00	00
93	YEAR OF MANUFACTURE IN BCD		x	x
94	WEEK OF MANUFACTURE IN BCD		x	x
95-98	MODULE SERIAL NUMBER		x	x
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		—	—

- NOTE:**
1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
 2. x = Variable Data.

**184-PIN DIMM
256MB and 512MB Modules**



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



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