# DRAM MODULE

MT8LD864A X, MT16LD1664A X,
MT32LD3264A X

*For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/datasheet.html*

## FEATURES

- Eight-CAS# ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 64MB (8 Meg x 64), 128MB (16 Meg x 64), and 256MB (32 Meg x 64)
- Nonbuffered
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are LVTTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- Extended Data-Out (EDO) PAGE MODE access cycle
- Serial presence-detect (SPD)

## OPTIONS — MARKING

- Package
  168-pin DIMM (gold) — G
- Timing
  50ns access — -5
  60ns access — -6
- Access Cycle
  EDO PAGE MODE — X

## KEY TIMING PARAMETERS

| SPEED | $^tRC$ | $^tRAC$ | $^tPC$ | $^tAA$ | $^tCAC$ | $^tCAS$ |
|---|---|---|---|---|---|---|
| -5 | 84ns | 50ns | 20ns | 25ns | 13ns | 8ns |
| -6 | 104ns | 60ns | 25ns | 30ns | 15ns | 10ns |

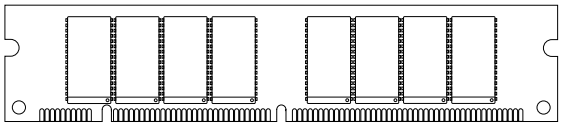
## PART NUMBERS

| PART NUMBER | CONFIGURATION | SPEED |
|---|---|---|
| MT8LD864AG-5X | 8 Meg x 64 | 50ns |
| MT8LD864AG-6X | 8 Meg x 64 | 60ns |
| MT16LD1664AG-5X | 16 Meg x 64 | 50ns |
| MT16LD1664AG-6X | 16 Meg x 64 | 60ns |
| MT32LD3264AG-5X* | 32 Meg x 64 | 50ns |
| MT32LD3264AG-6X* | 32 Meg x 64 | 60ns |

*Contact factory for availability

**NOTE:** Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

## PIN ASSIGNMENT (Front View)
## 168-Pin DIMM
(H-14; 64MB)
(H-17; 128MB)
(H-30; 256MB)



| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | VSS | 43 | VSS | 85 | VSS | 127 | VSS |
| 2 | DQ0 | 44 | OE2# | 86 | DQ32 | 128 | RFU |
| 3 | DQ1 | 45 | RAS2# | 87 | DQ33 | 129 | NC/RAS3#** |
| 4 | DQ2 | 46 | CAS2# | 88 | DQ34 | 130 | CAS6# |
| 5 | DQ3 | 47 | CAS3# | 89 | DQ35 | 131 | CAS7# |
| 6 | VDD | 48 | WE2# | 90 | VDD | 132 | RFU |
| 7 | DQ4 | 49 | VDD | 91 | DQ36 | 133 | VDD |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | NC | 94 | DQ39 | 136 | NC |
| 11 | DQ8 | 53 | NC | 95 | DQ40 | 137 | NC |
| 12 | VSS | 54 | VSS | 96 | VSS | 138 | VSS |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | VDD | 101 | DQ45 | 143 | VDD |
| 18 | VDD | 60 | DQ20 | 102 | VDD | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | RFU | 104 | DQ47 | 146 | RFU |
| 21 | NC | 63 | NC | 105 | NC | 147 | NC |
| 22 | NC | 64 | VSS | 106 | NC | 148 | VSS |
| 23 | VSS | 65 | DQ21 | 107 | VSS | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | VDD | 68 | VSS | 110 | VDD | 152 | VSS |
| 27 | WE0# | 69 | DQ24 | 111 | RFU | 153 | DQ56 |
| 28 | CAS0# | 70 | DQ25 | 112 | CAS4# | 154 | DQ57 |
| 29 | CAS1# | 71 | DQ26 | 113 | CAS5# | 155 | DQ58 |
| 30 | RAS0# | 72 | DQ27 | 114 | NC/RAS1#** | 156 | DQ59 |
| 31 | OE0# | 73 | VDD | 115 | RFU | 157 | VDD |
| 32 | VSS | 74 | DQ28 | 116 | VSS | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | VSS | 120 | A7 | 162 | VSS |
| 37 | A8 | 79 | NC | 121 | A9 | 163 | NC |
| 38 | A10 | 80 | NC | 122 | A11 | 164 | NC |
| 39 | NC (A12) | 81 | NC | 123 | NC (A13) | 165 | SA0 |
| 40 | VDD | 82 | SDA | 124 | VDD | 166 | SA1 |
| 41 | VDD | 83 | SCL | 125 | RFU | 167 | SA2 |
| 42 | RFU | 84 | VDD | 126 | RFU | 168 | VDD |

** 256MB version only

## GENERAL DESCRIPTION

The Micron® MT8LD864A X, MT16LD1664A X and MT32LD3264A X are randomly accessed 64MB, 128MB and 256MB memories organized in a x64 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 22/23 address bits, which are entered 12 bits (A0-A11) at RAS# time and 11/12 bits (A0-A11) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

## EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time ($^{t}$CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after $^{t}$OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 16 Meg x 4 [MT4LC16M4H9] DRAM data sheet for additional information on EDO functionality.)

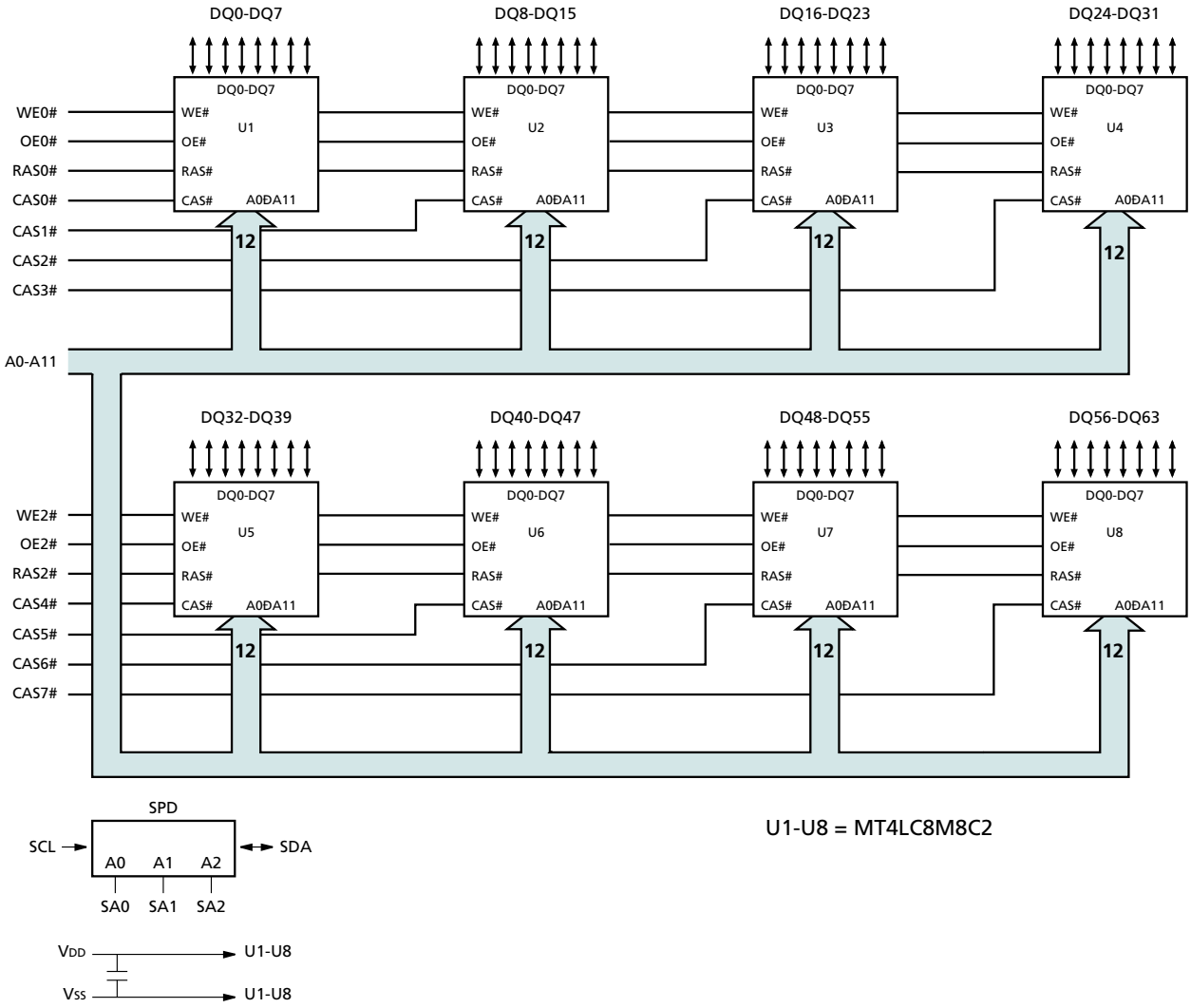
## REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A10/A11) are executed at least every $^{t}$REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

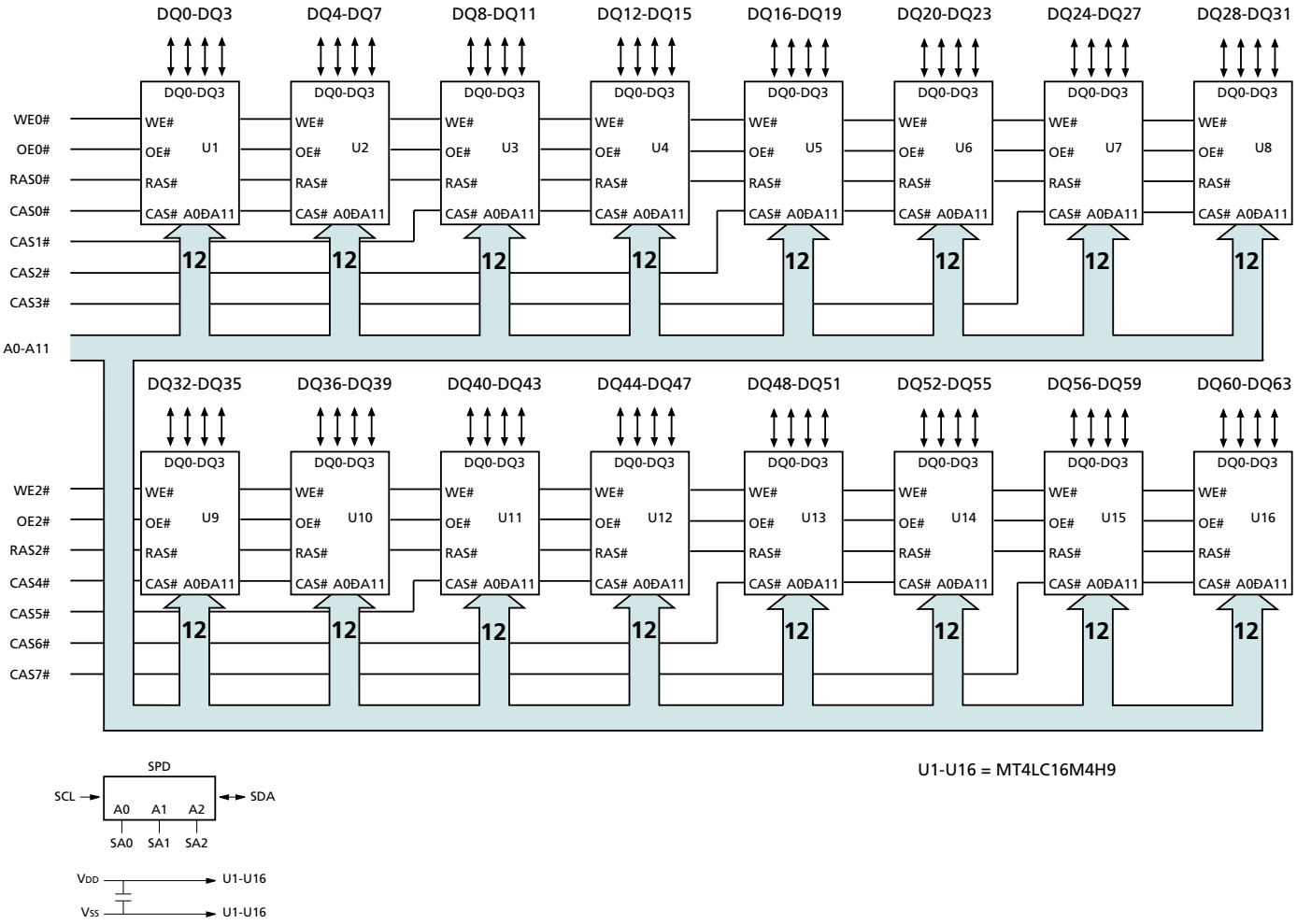
## SERIAL PRESENCE-DETECT OPERATION

This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide 8 unique DIMM/EEPROM addresses.

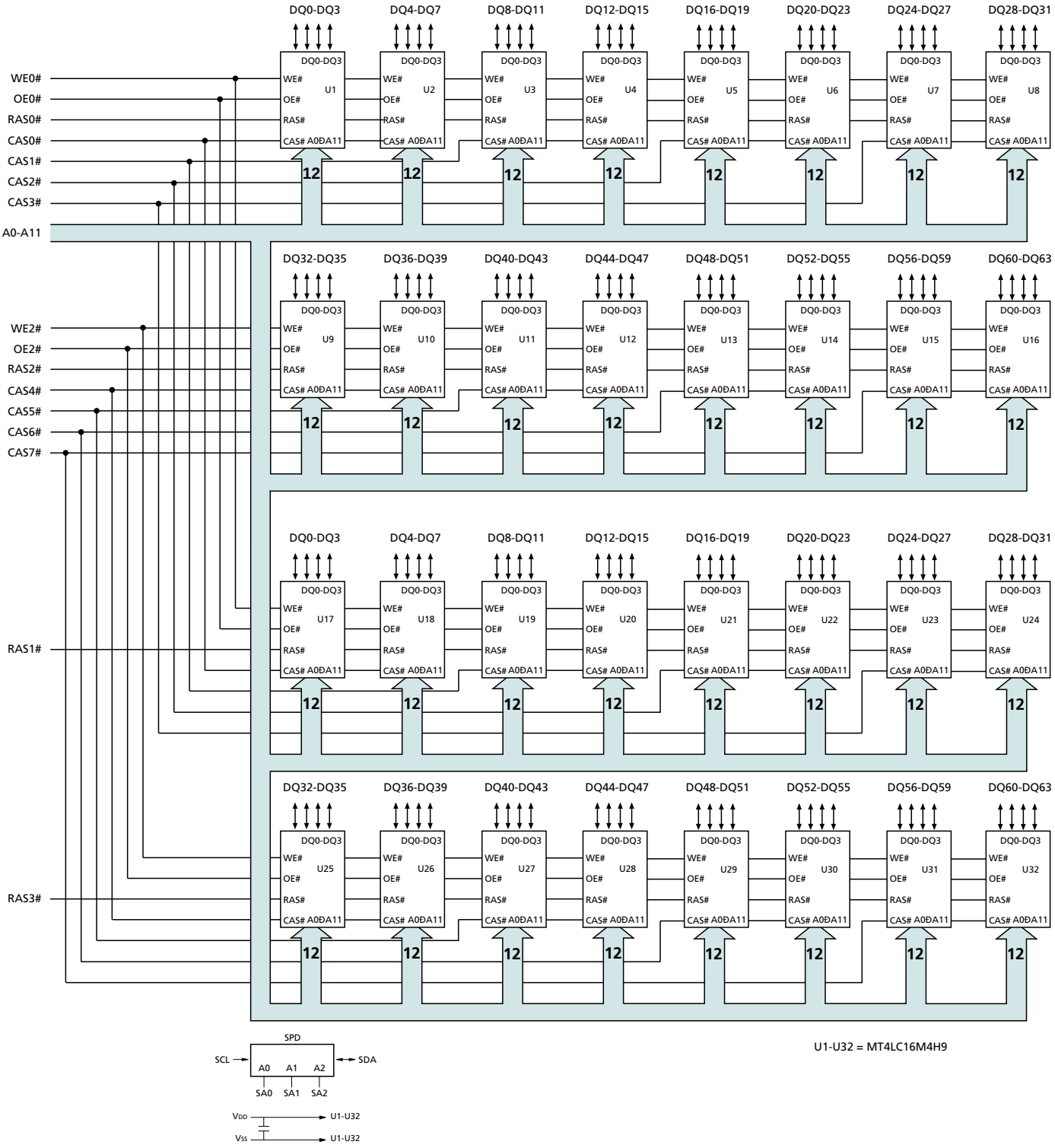
## FUNCTIONAL BLOCK DIAGRAM
## MT8LD864A X (64MB)



# FUNCTIONAL BLOCK DIAGRAM
# MT16LD1664A X (128MB)



# FUNCTIONAL BLOCK DIAGRAM
# MT32LD3264A X (256MB)



## PIN DESCRIPTIONS

| PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 30, 45, 114, 129 | RAS0#-RAS3# | Input | Row-Address Strobe: RAS# is used to clock-in the row-address bits. Two RAS# inputs allow for one x64 bank or two x32 banks. |
| 28, 29, 46, 47, 112, 113, 130, 131 | CAS0#-CAS7# | Input | Column-Address Strobe: CAS# is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS# inputs allow byte access control for any memory bank configuration. |
| 27, 48 | WE0#, WE2# | Input | Write Enable: WE# is the READ/WRITE control for the DQ pins. WE0# controls DQ0-DQ31. WE2# controls DQ32-DQ63. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle. |
| 31, 44 | OE0#, OE2# | Input | Output Enable: OE# is the input/output control for the DQ pins. OE0# controls DQ0-DQ31. OE2# controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles. |
| 33-38, 117-122 | A0-A11 | Input | Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#. |
| 2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89,91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161 | DQ0-DQ63 | Input/ Output | Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS# select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location. |
| 42, 62, 111, 115, 125-126, 128, 132, 146 | RFU | – | Reserved for Future Use: These pins should be left unconnected. |
| 6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168 | $V_{DD}$ | Supply | Power Supply: +3.3V ±0.3V. |
| 1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162 | $V_{SS}$ | Supply | Ground. |
| 82 | SDA | Input/Output | Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module. |
| 83 | SCL | Input | Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module. |
| 165-167 | SA0-SA2 | Input | Presence-Detect Address Inputs. These pins are used to configure the presence-detect device. |

### SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

### SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

### SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

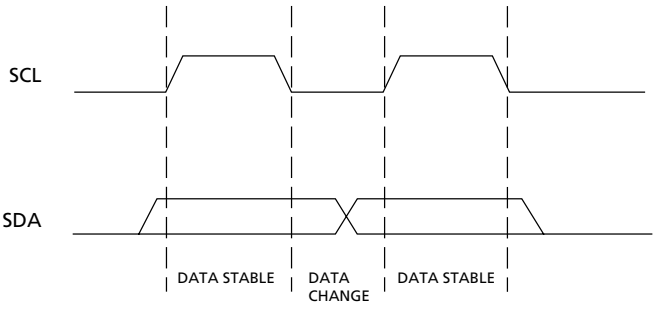



**Figure 1**
**Data Validity**

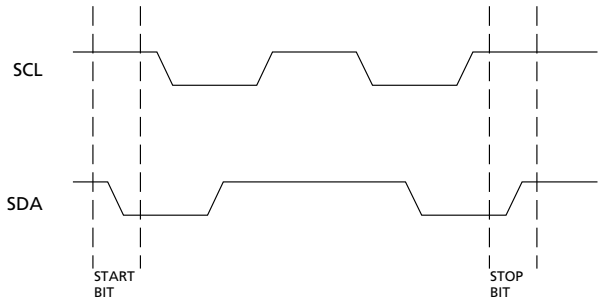



**Figure 2**
**Definition of Start and Stop**

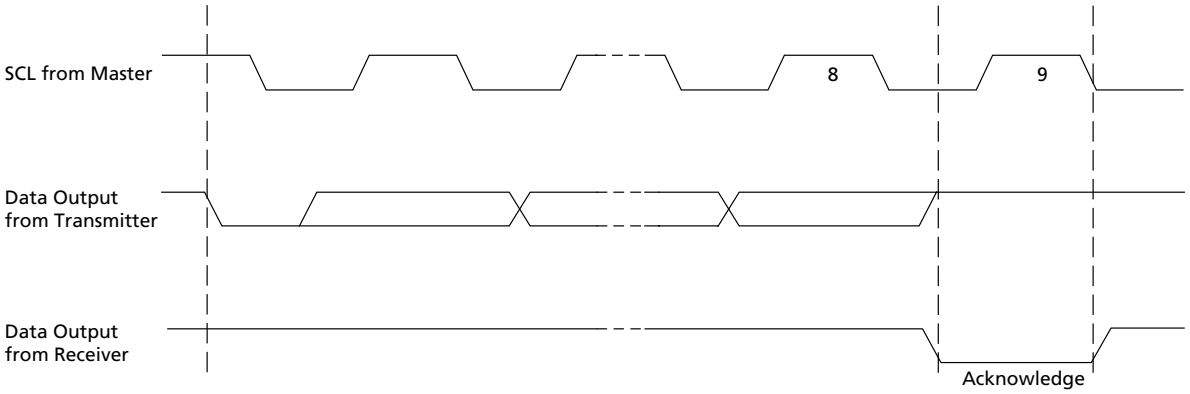



**Figure 3**
**Acknowledge Response From Receiver**

## SERIAL PRESENCE-DETECT MATRIX

| BYTE | DESCRIPTION | ENTRY (VERSION) | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | NUMBER OF BYTES USED BY MICRON | 128 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 |
| 1 | TOTAL NUMBER OF SPD MEMORY BYTES | 256 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 |
| 2 | MEMORY TYPE | EDO PAGE MODE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| 3 | NUMBER OF ROW ADDRESSES | 12 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C |
| 4 | NUMBER OF COLUMN ADDRESSES | 11 (64MB) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |
| | | 12 (128MB, 256MB) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C |
| 5 | NUMBER OF BANKS | 1 (64MB, 128MB) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| | | 2 (256MB) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| 6 | DATA WIDTH | x64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 |
| 7 | DATA WIDTH (continued) | NONE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 8 | VOLTAGE INTERFACE | LVTTL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| 9 | RAS# ACCESS TIME ($^{t}$RAC) | 50ns (-5) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 |
| | | 60ns (-6) | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C |
| 10 | CAS# ACCESS TIME ($^{t}$CAC) | 13ns (-5) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| | | 15ns (-6) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| 11 | MODULE CONFIGURATION TYPE | NONPARITY | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 12 | REFRESH RATES | 15.625µs/NORMAL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 13 | DRAM WIDTH (PRIMARY DRAM) | x8 (64MB) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 |
| | | x4 (128MB, 256MB) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| 14 | ERROR CHECKING DRAM DATA WIDTH | NONE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 15-61 | RESERVED | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 62 | SPD REVISION | REV. 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 63 | CHECKSUM FOR BYTES 0-62 | 64MB -5 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A |
| | | 64MB -6 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 |
| | | 128MB -5 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33 |
| | | 128MB -6 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 3F |
| | | 256MB -5 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 |
| | | 256MB -6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 |
| 64 | MANUFACTURER'S JEDEC ID CODE | MICRON | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C |
| 65-71 | MANUFACTURER'S JEDEC CODE (CONT.) | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| 72 | MANUFACTURING LOCATION | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 73-90 | MODULE PART NUMBER (ASCII) | | x | x | x | x | x | x | x | x | xx |
| 91 | PCB IDENTIFICATION CODE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| | | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| | | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| | | 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 92 | IDENTIFICATION CODE (CONT.) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 93 | YEAR OF MANUFACTURE IN BCD | | x | x | x | x | x | x | x | x | xx |
| 94 | WEEK OF MANUFACTURE IN BCD | | x | x | x | x | x | x | x | x | xx |
| 95-98 | MODULE SERIAL NUMBER | | x | x | x | x | x | x | x | x | xx |
| 99-125 | MANUFACTURE SPECIFIC DATA (RSVD) | | – | – | – | – | – | – | – | – | – |

**NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{DD}$ Pin Relative to $V_{SS}$ .....-1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to $V_{SS}$ .....-1V to +4.6V
Operating Temperature, $T_A$ (ambient) .. 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation ..... 8W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) ($V_{DD}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | | SYMBOL | SIZE | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| SUPPLY VOLTAGE | | $V_{DD}$ | ALL | 3 | 3.6 | V | |
| INPUT HIGH VOLTAGE: Logic 1; All inputs | | $V_{IH}$ | ALL | 2 | $V_{DD}$ + 0.3 | V | 30 |
| INPUT LOW VOLTAGE: Logic 0; All inputs | | $V_{IL}$ | ALL | -0.5 | 0.8 | V | 30 |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$ + 0.3V<br>(All other pins not under test = 0V) | CAS0#-CAS7# | $I_{I1}$ | 64MB<br>128MB<br>256MB | -2<br>-4<br>-8 | 2<br>4<br>8 | µA | |
| | A0-A11 | $I_{I2}$ | 64MB<br>128MB<br>256MB | -16<br>-32<br>-64 | 16<br>32<br>64 | µA | |
| | WE0#, WE2#,<br>OE0#, OE2# | $I_{I3}$ | 64MB<br>128MB<br>256MB | -8<br>-16<br>-32 | 8<br>16<br>32 | µA | |
| | RAS0#-RAS3# | $I_{I4}$ | 64MB<br>128MB<br>256MB | -8<br>-16<br>-16 | 8<br>16<br>16 | µA | |
| OUTPUT LEAKAGE CURRENT:<br>DQ is disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DD}$ + 0.3V | DQ0-DQ63 | $I_{OZ}$ | 64MB<br>128MB<br>256MB | -5<br>-5<br>-10 | 5<br>5<br>10 | µA | |
| OUTPUT LEVELS:<br>Output High Voltage ($I_{OUT}$ = -2mA) | | $V_{OH}$ | ALL | 2.4 | – | V | |
| Output Low Voltage ($I_{OUT}$ = 2mA) | | $V_{OL}$ | ALL | – | 0.4 | V | |

## $I_{CC}$ OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) ($V_{DD}$ = +3.3V ±0.3V)

| | | | MAX | | | |
|---|---|---|---|---|---|---|
| PARAMETER/CONDITION | SYMBOL | SIZE | -5 | -6 | UNITS | NOTES |
| STANDBY CURRENT: TTL<br>(RAS# = CAS# = $V_{IH}$) | $I_{CC1}$ | 64MB<br>128MB<br>256MB | 8<br>16<br>32 | 8<br>16<br>32 | mA | |
| STANDBY CURRENT: CMOS<br>(RAS# = CAS# = $V_{DD}$ - 0.2V) | $I_{CC2}$ | 64MB<br>128MB<br>256MB | 4<br>8<br>16 | 4<br>8<br>16 | mA | |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^{t}RC$ = $^{t}RC$ [MIN]) | $I_{CC3}$ | 64MB<br>128MB<br>256MB | 1,400<br>2,720<br>2,736 | 1,320<br>2,560<br>2,576 | mA | 3, 24 |
| OPERATING CURRENT: EDO PAGE MODE<br>Average power supply current<br>(RAS# = $V_{IL}$, CAS#, address cycling: $^{t}PC$ = $^{t}PC$ [MIN]) | $I_{CC4}$ | 64MB<br>128MB<br>256MB | 1,240<br>2,400<br>2,416 | 1,000<br>1,920<br>1,936 | mA | 3, 24 |
| REFRESH CURRENT: RAS#-ONLY<br>Average power supply current<br>(RAS# cycling, CAS# = $V_{IH}$: $^{t}RC$ = $^{t}RC$ [MIN]) | $I_{CC5}$ | 64MB<br>128MB<br>256MB | 1,400<br>2,720<br>2,736 | 1,320<br>2,560<br>2,576 | mA | 3, 24 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^{t}RC$ = $^{t}RC$ [MIN]) | $I_{CC6}$ | 64MB<br>128MB<br>256MB | 1,320<br>2,560<br>2,576 | 1,240<br>2,400<br>2,416 | mA | 3, 4 |

## CAPACITANCE

| | | MAX | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | 64MB | 128MB | 256MB | UNITS | NOTES |
| Input Capacitance: A0-A11 | $C_{I1}$ | 46 | 86 | 168 | pF | 2 |
| Input Capacitance: WE0#, WE2#, OE0#, OE2# | $C_{I2}$ | 32 | 60 | 118 | pF | 2 |
| Input Capacitance: RAS0#-RAS3# | $C_{I3}$ | 32 | 60 | 60 | pF | 2 |
| Input Capacitance: CAS0#-CAS7# | $C_{I4}$ | 10 | 18 | 32 | pF | 2 |
| Input Capacitance: SCL, SA0-SA2 | $C_{I5}$ | 6 | 6 | 6 | pF | 2 |
| Input/Output Capacitance: DQ0-DQ63, SDA | $C_{IO}$ | 12 | 12 | 22 | pF | 2 |

## EDO PAGE MODE
## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{DD}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS | | -5 | | -6 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column address | $^tAA$ | | 25 | | 30 | ns | |
| Column-address setup to CAS# precharge during writes | $^tACH$ | 12 | | 15 | | ns | |
| Column-address hold time (referenced to RAS#) | $^tAR$ | 38 | | 45 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | 0 | | ns | |
| Row-address setup time | $^tASR$ | 0 | | 0 | | ns | |
| Column address to WE# delay time | $^tAWD$ | 42 | | 49 | | ns | 23 |
| Access time from CAS# | $^tCAC$ | | 13 | | 15 | ns | 14 |
| Column-address hold time | $^tCAH$ | 8 | | 10 | | ns | |
| CAS# pulse width | $^tCAS$ | 8 | 10,000 | 10 | 10,000 | ns | |
| CAS# hold time (CBR Refresh) | $^tCHR$ | 8 | | 10 | | ns | 4 |
| CAS# to output in Low-Z | $^tCLZ$ | 0 | | 0 | | ns | |
| Data output hold after CAS# LOW | $^tCOH$ | 3 | | 3 | | ns | |
| CAS# precharge time | $^tCP$ | 8 | | 10 | | ns | 15 |
| Access time from CAS# precharge | $^tCPA$ | | 28 | | 35 | ns | |
| CAS# to RAS# precharge time | $^tCRP$ | 5 | | 5 | | ns | |
| CAS# hold time | $^tCSH$ | 38 | | 45 | | ns | |
| CAS# setup time (CBR Refresh) | $^tCSR$ | 5 | | 5 | | ns | 4 |
| CAS# to WE# delay time | $^tCWD$ | 30 | | 35 | | ns | 23 |
| WRITE command to CAS# lead time | $^tCWL$ | 8 | | 10 | | ns | |
| Data-in hold time | $^tDH$ | 8 | | 10 | | ns | 22 |
| Data-in setup time | $^tDS$ | 0 | | 0 | | ns | 22 |
| Output disable | $^tOD$ | 0 | 12 | 0 | 15 | ns | |
| Output enable | $^tOE$ | | 12 | | 15 | ns | |
| OE# hold time from WE# during READ-MODIFY-WRITE cycle | $^tOEH$ | 8 | | 10 | | ns | |
| OE# HIGH hold time from CAS# HIGH | $^tOEHC$ | 5 | | 10 | | ns | |
| OE# HIGH pulse width | $^tOEP$ | 5 | | 5 | | ns | |
| OE# LOW to CAS# HIGH setup time | $^tOES$ | 4 | | 5 | | ns | |
| Output buffer turn-off delay | $^tOFF$ | 0 | 12 | 0 | 15 | ns | 19, 27 |
| OE# setup prior to RAS# during HIDDEN REFRESH cycle | $^tORD$ | 0 | | 0 | | ns | 19 |
| EDO-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 20 | | 25 | | ns | |
| EDO-PAGE-MODE READ-WRITE cycle time | $^tPRWC$ | 47 | | 56 | | ns | |
| Access time from RAS# | $^tRAC$ | | 50 | | 60 | ns | 13 |
| RAS# to column-address delay time | $^tRAD$ | 9 | | 12 | | ns | 17 |
| Row-address hold time | $^tRAH$ | 9 | | 10 | | ns | |
| RAS# pulse width | $^tRAS$ | 50 | 10,000 | 60 | 10,000 | ns | |
| RAS# pulse width (EDO PAGE MODE) | $^tRASP$ | 50 | 125,000 | 60 | 125,000 | ns | |
| Random READ or WRITE cycle time | $^tRC$ | 84 | | 104 | | ns | |
| RAS# to CAS# delay time | $^tRCD$ | 11 | | 14 | | ns | 16 |
| READ command hold time (referenced to CAS#) | $^tRCH$ | 0 | | 0 | | ns | 18 |
| READ command setup time | $^tRCS$ | 0 | | 0 | | ns | |

## EDO PAGE MODE
## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{DD}$ = +3.3V ±0.3V)

| AC CHARACTERISTICS | | -5 | | -6 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Refresh period (4,096 cycles) | $^{t}$REF | | 64 | | 64 | ms | |
| RAS# precharge time | $^{t}$RP | 30 | | 40 | | ns | |
| RAS# to CAS# precharge time | $^{t}$RPC | 5 | | 5 | | ns | |
| READ command hold time (referenced to RAS#) | $^{t}$RRH | 0 | | 0 | | ns | 18 |
| RAS# hold time | $^{t}$RSH | 13 | | 15 | | ns | |
| READ-WRITE cycle time | $^{t}$RWC | 116 | | 140 | | ns | |
| RAS# to WE# delay time | $^{t}$RWD | 67 | | 79 | | ns | 23 |
| WRITE command to RAS# lead time | $^{t}$RWL | 13 | | 15 | | ns | |
| Transition time (rise or fall) | $^{t}$T | 2 | 50 | 2 | 50 | ns | |
| WRITE command hold time | $^{t}$WCH | 8 | | 10 | | ns | |
| WRITE command hold time (referenced to RAS#) | $^{t}$WCR | 38 | | 45 | | ns | |
| WE# command setup time | $^{t}$WCS | 0 | | 0 | | ns | |
| Output disable delay from WE# (CAS# HIGH) | $^{t}$WHZ | | 12 | | 15 | ns | |
| WRITE command pulse width | $^{t}$WP | 5 | | 5 | | ns | |
| WE# pulse width for output disable when CAS# HIGH | $^{t}$WPZ | 10 | | 10 | | ns | |
| WE# hold time (CBR Refresh) | $^{t}$WRH | 8 | | 10 | | ns | |
| WE# setup time (CBR Refresh) | $^{t}$WRP | 8 | | 10 | | ns | |

## SERIAL PRESENCE-DETECT EEPROM OPERATING CONDITIONS

(Notes: 1) ($V_{DD}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| SUPPLY VOLTAGE | $V_{DD}$ | 3 | 3.6 | V | |
| INPUT HIGH VOLTAGE: Logic 1; All inputs | $V_{IH}$ | $V_{DD}$ x 0.7 | $V_{DD}$ + 0.5 | V | |
| INPUT LOW VOLTAGE: Logic 0; All inputs | $V_{IL}$ | -1 | $V_{DD}$ x 0.3 | V | |
| OUTPUT LOW VOLTAGE: $I_{OUT}$ = 3mA | $V_{OL}$ | – | 0.4 | V | |
| INPUT LEAKAGE CURRENT: $V_{IN}$ = GND to $V_{DD}$ | $I_{LI}$ | – | 10 | µA | |
| OUTPUT LEAKAGE CURRENT: $V_{OUT}$ = GND to $V_{DD}$ | $I_{LO}$ | – | 10 | µA | |
| STANDBY CURRENT:<br>SCL = SDA = $V_{DD}$ - 0.3V; All other inputs = GND or 3.3V +10% | $I_{SB}$ | – | 30 | µA | |
| POWER SUPPLY CURRENT:<br>SCL clock frequency = 100 KHz | $I_{CC}$ | – | 2 | mA | |

## SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

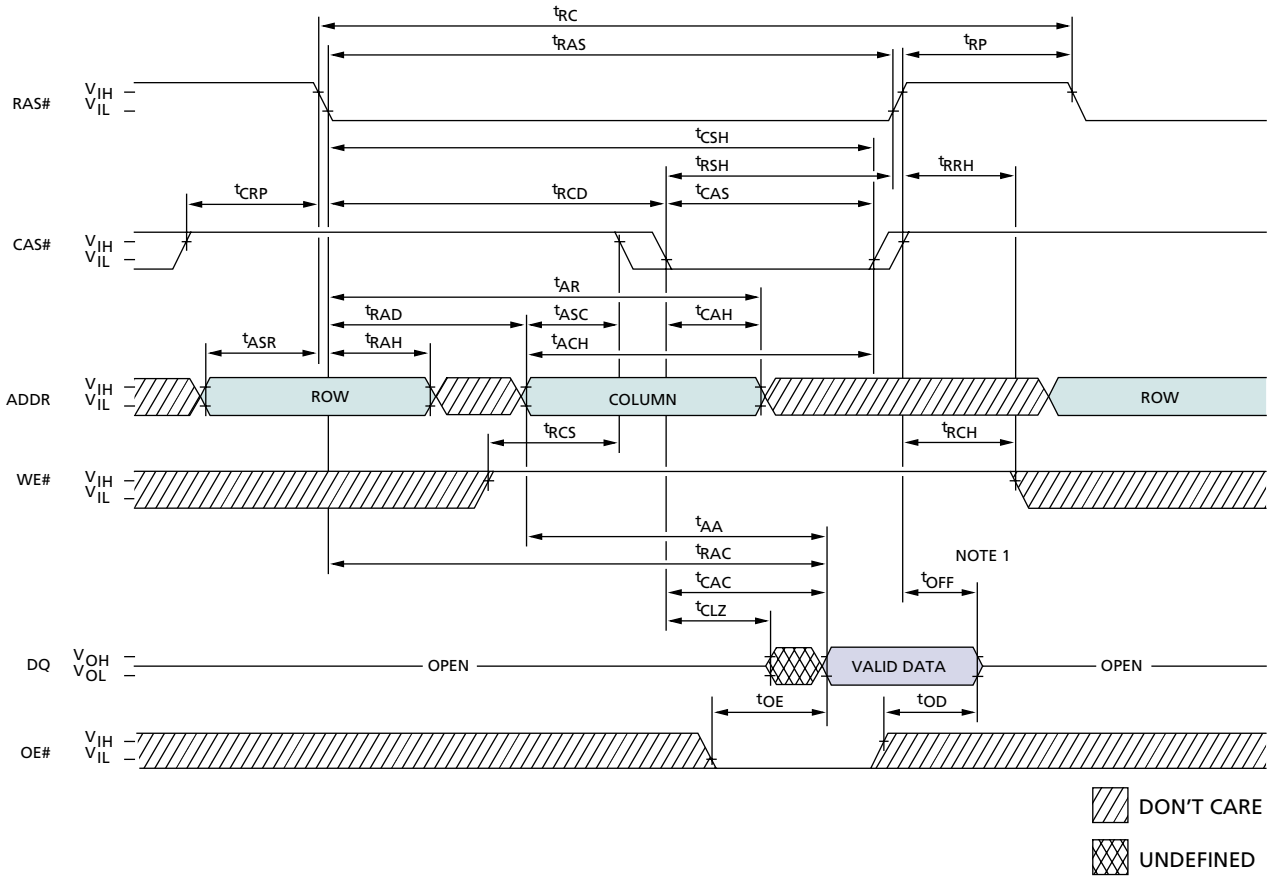
(Notes: 1) ($V_{DD}$ = +3.3V ±0.3V)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| SCL LOW to SDA data-out valid | $^{t}AA$ | 0.3 | 3.5 | µs | |
| Time the bus must be free before a new transition can start | $^{t}BUF$ | 4.7 | | µs | |
| Data-out hold time | $^{t}DH$ | 300 | | ns | |
| SDA and SCL fall time | $^{t}F$ | | 300 | ns | |
| Data-in hold time | $^{t}HD:DAT$ | 0 | | µs | |
| Start condition hold time | $^{t}HD:STA$ | 4 | | µs | |
| Clock HIGH period | $^{t}HIGH$ | 4 | | µs | |
| Noise suppression time constant at SCL, SDA inputs | $^{t}I$ | | 100 | ns | |
| Clock LOW period | $^{t}LOW$ | 4.7 | | µs | |
| SDA and SCL rise time | $^{t}R$ | | 1 | µs | |
| SCL clock frequency | $^{t}SCL$ | | 100 | KHz | |
| Data-in setup time | $^{t}SU:DAT$ | 250 | | ns | |
| Start condition setup time | $^{t}SU:STA$ | 4.7 | | µs | |
| Stop condition setup time | $^{t}SU:STO$ | 4.7 | | µs | |
| WRITE cycle time | $^{t}WR$ | | 10 | ms | 28 |

## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{DD}$ = +3.3V; f = 1 MHz.
3. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the $^{t}$REF refresh requirement is exceeded.
7. AC characteristics assume $^{t}$T = 2ns for -5 and 2.5ns for -6.
8. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
9. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
10. If CAS# and RAS# = $V_{IH}$, data output is High-Z.
11. If CAS# = $V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and $V_{OL}$ = 0.8V and $V_{OH}$ = 2V.
13. Requires that $^{t}$AA and $^{t}$CAC are not violated.
14. Requires that $^{t}$AA and $^{t}$RAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for $^{t}$CP.
16. The $^{t}$RCD (MAX) limit is no longer specified. $^{t}$RCD (MAX) was specified as a reference point only. If $^{t}$RCD was greater than the specified $^{t}$RCD (MAX) limit, then access time was controlled exclusively by $^{t}$CAC ($^{t}$RAC [MIN] no longer applied). With or without the $^{t}$RCD (MAX) limit, $^{t}$AA and $^{t}$CAC must always be met.
17. The $^{t}$RAD (MAX) limit is no longer specified. $^{t}$RAD (MAX) was specified as a reference point only. If $^{t}$RAD was greater than the specified $^{t}$RAD (MAX) limit, then access time was controlled exclusively by $^{t}$AA ($^{t}$RAC and $^{t}$CAC no longer applied). With or without the $^{t}$RAD (MAX) limit, $^{t}$AA, $^{t}$RAC and $^{t}$CAC must always be met.
18. Either $^{t}$RCH or $^{t}$RRH must be satisfied for a READ cycle.
19. $^{t}$OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. $^{t}$WCS, $^{t}$RWD, $^{t}$AWD and $^{t}$CWD are not restrictive operating parameters. $^{t}$WCS applies to EARLY WRITE cycles. If $^{t}$WCS > $^{t}$WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. $^{t}$RWD, $^{t}$AWD and $^{t}$CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. $^{t}$WCS, $^{t}$RWD, $^{t}$CWD and $^{t}$AWD are not applicable in a LATE WRITE cycle.
24. Column address changed once each cycle.
25. The 3ns minimum parameter guaranteed by design.
26. Measured with the specified current load and 100pF.
27. $^{t}$OFF on an EDO module is determined by the latter of the RAS# and CAS# signals to transition HIGH.
28. The SPD EEPROM WRITE cycle time ($^{t}$WR) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
30. $V_{IH}$ overshoot: $V_{IH}$ (MAX) = $V_{DD}$ + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. $V_{IL}$ undershoot: $V_{IL}$ (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

## READ CYCLE



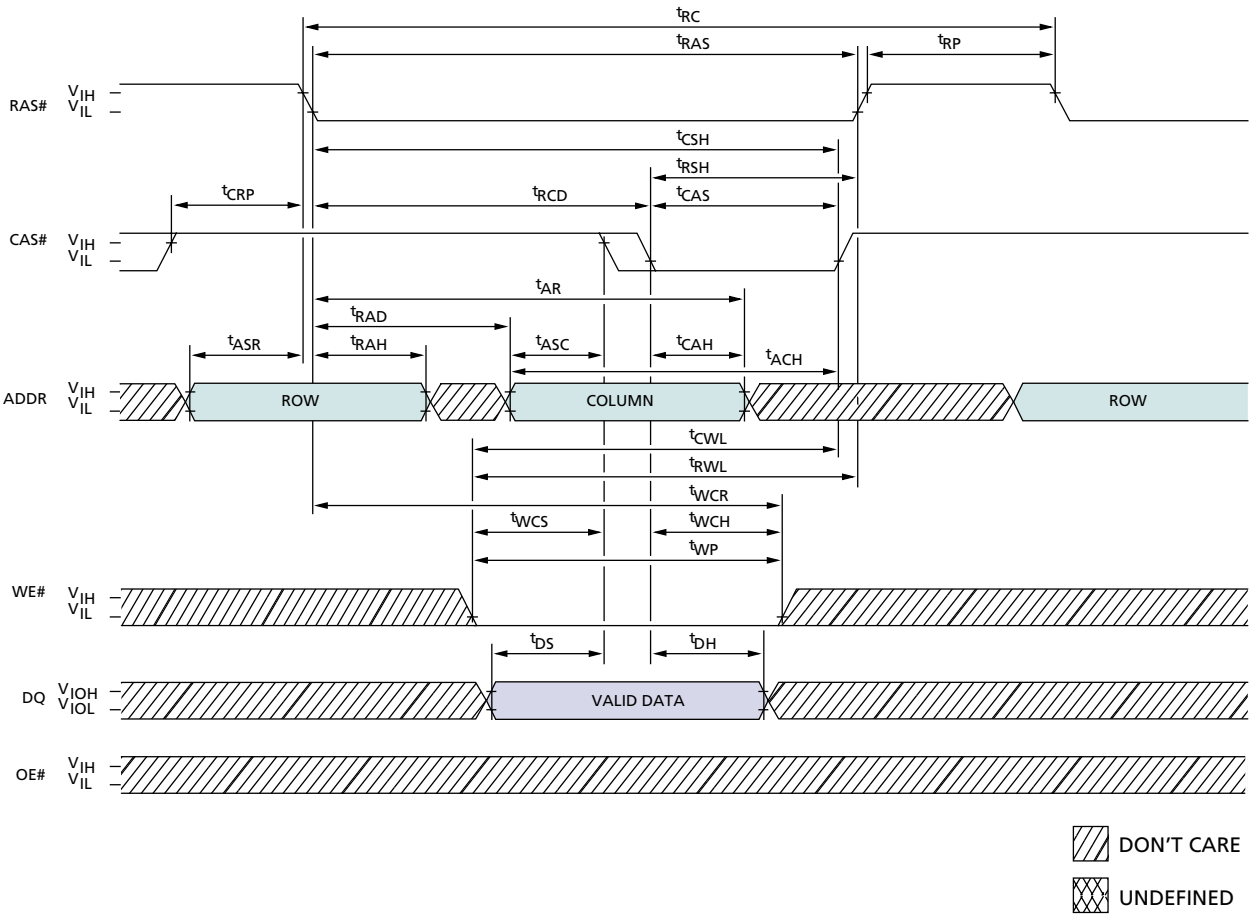

## TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOFF | 0 | 12 | 0 | 15 | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |

**NOTE:** 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

## EARLY WRITE CYCLE

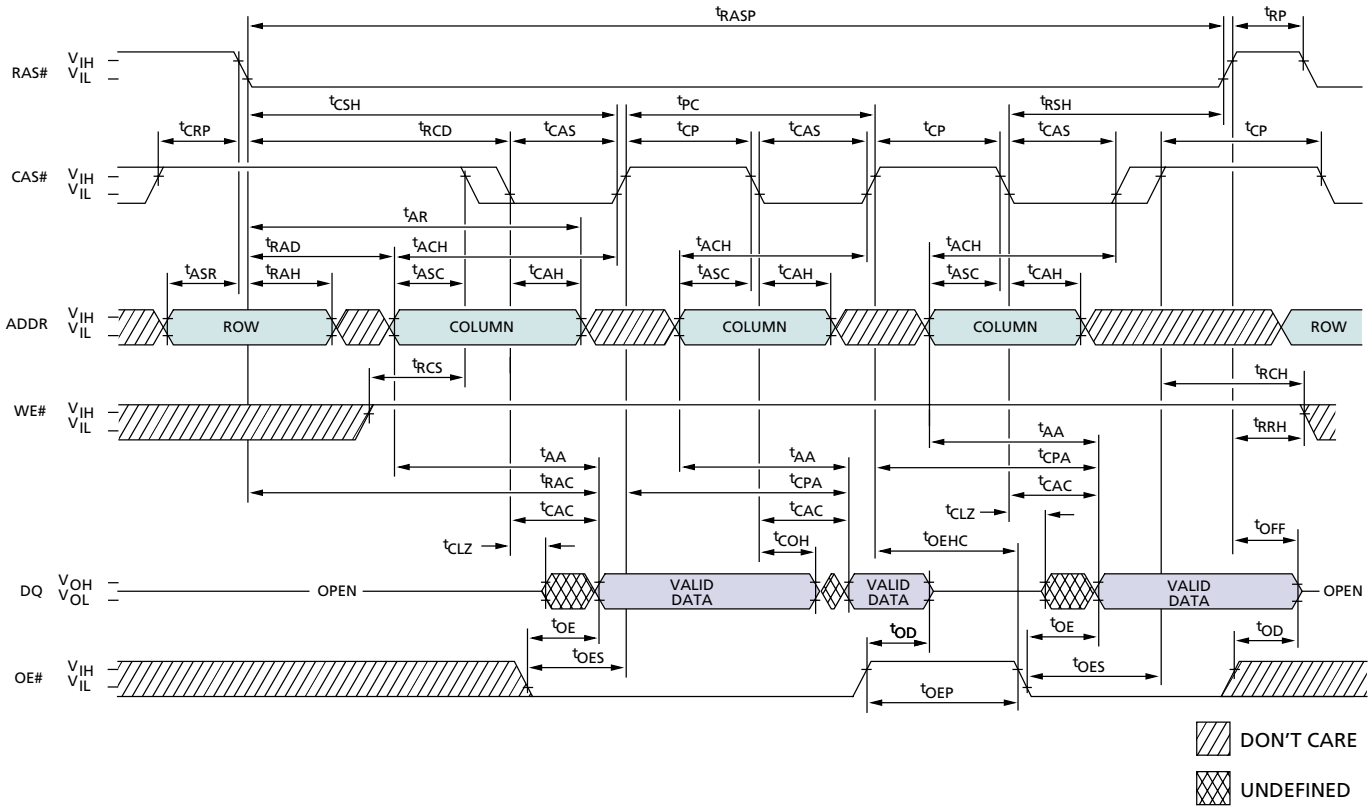



## TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |
| tRAD | 9 | | 12 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCR | 38 | | 45 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 5 | | 5 | | ns |

## EDO-PAGE-MODE READ CYCLE

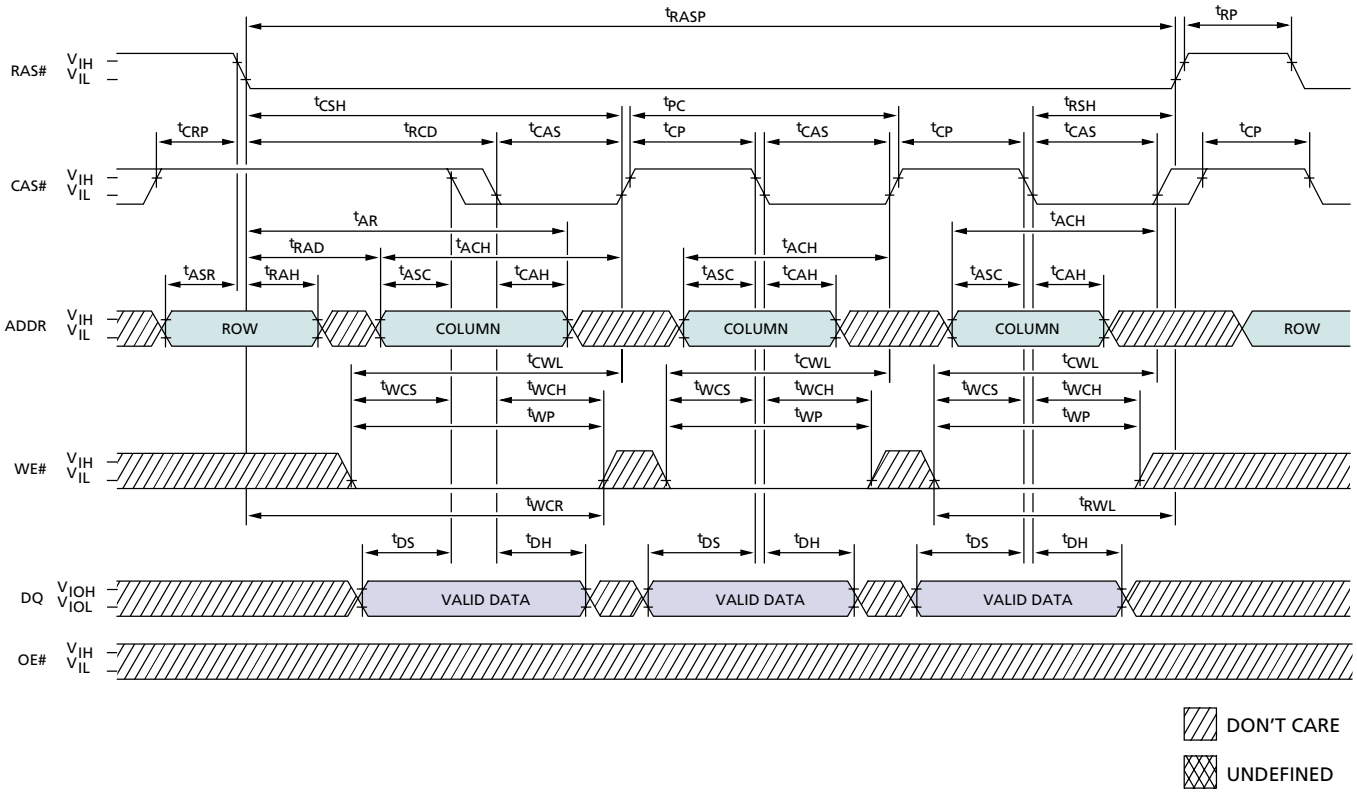



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOEHC | 5 | | 10 | | ns |
| tOEP | 5 | | 5 | | ns |
| tOES | 4 | | 5 | | ns |
| tOFF | 0 | 12 | 0 | 15 | ns |
| tPC | 20 | | 25 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |

## EDO-PAGE-MODE EARLY WRITE CYCLE

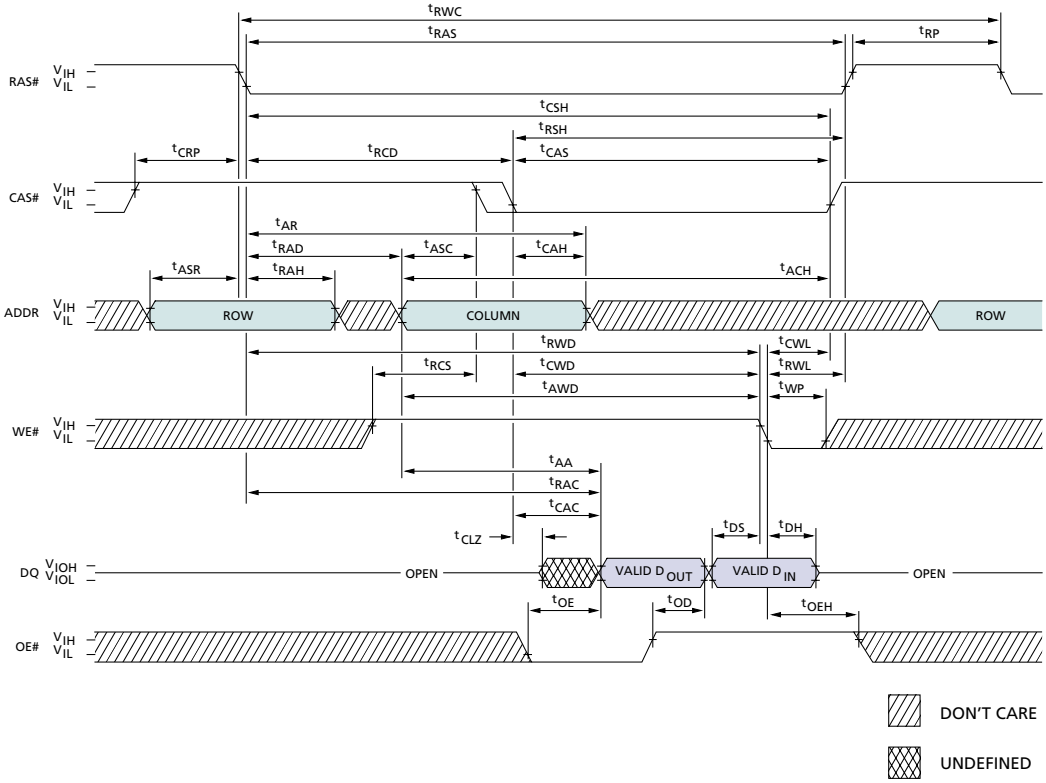



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tPC | 20 | | 25 | | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCR | 38 | | 45 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 5 | | 5 | | ns |

## READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

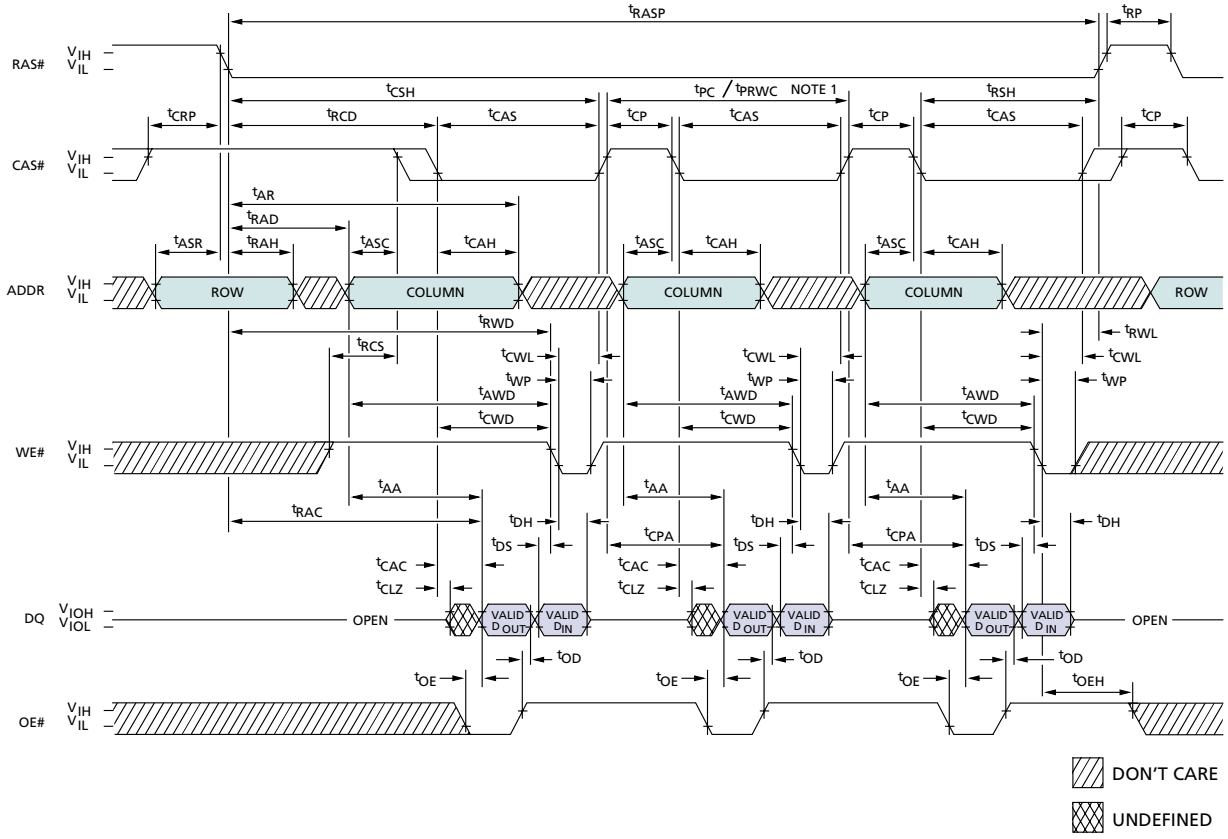



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 42 | | 49 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWD | 30 | | 35 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |
| tOEH | 8 | | 10 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWC | 116 | | 140 | | ns |
| tRWD | 67 | | 79 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWP | 5 | | 5 | | ns |

## EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



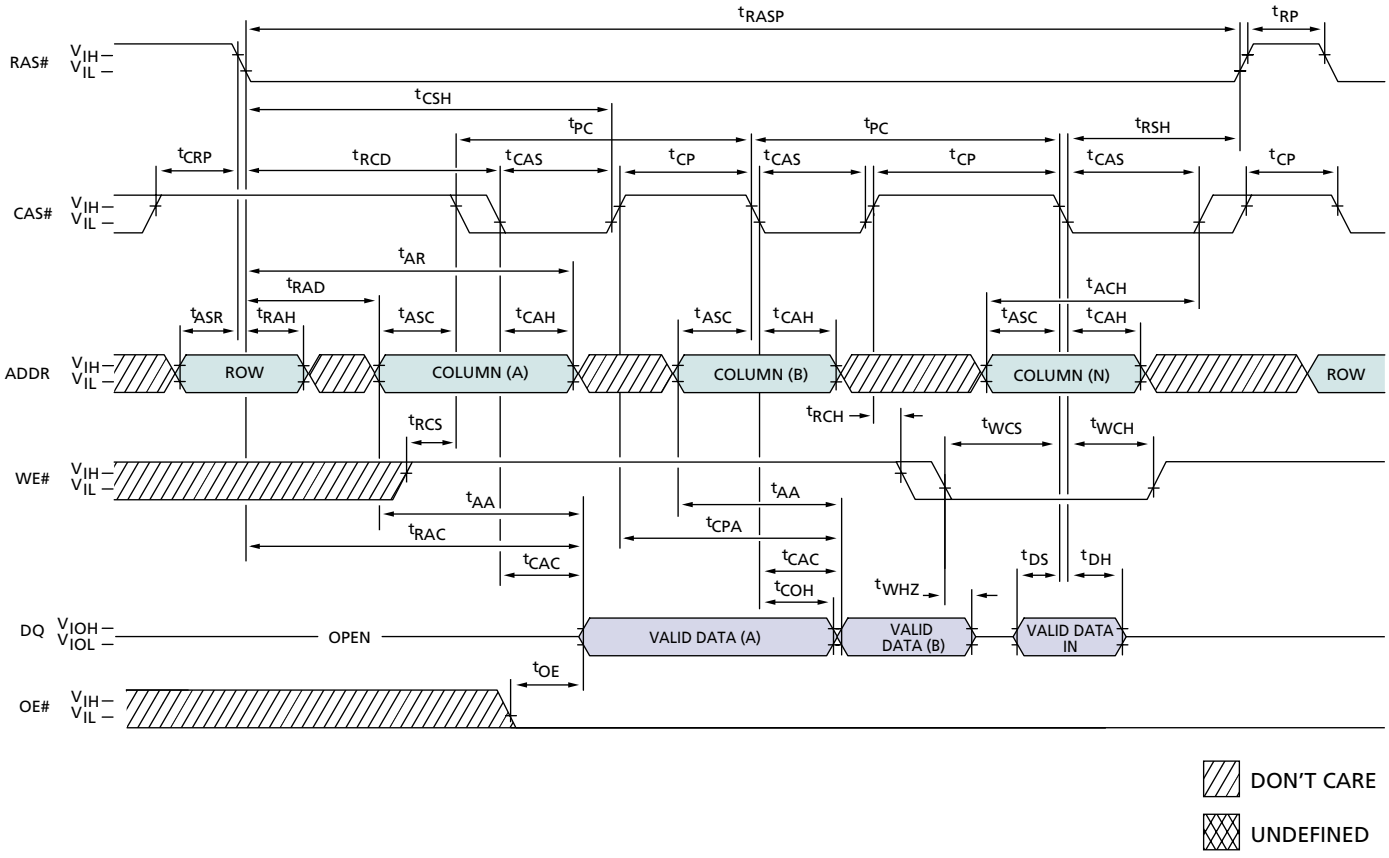

### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 42 | | 49 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWD | 30 | | 35 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |
| tOEH | 8 | | 10 | | ns |
| tPC | 20 | | 25 | | ns |
| tPRWC | 47 | | 56 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWD | 67 | | 79 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWP | 5 | | 5 | | ns |

**NOTE:** 1. tPC is for LATE WRITE cycles only.

## EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

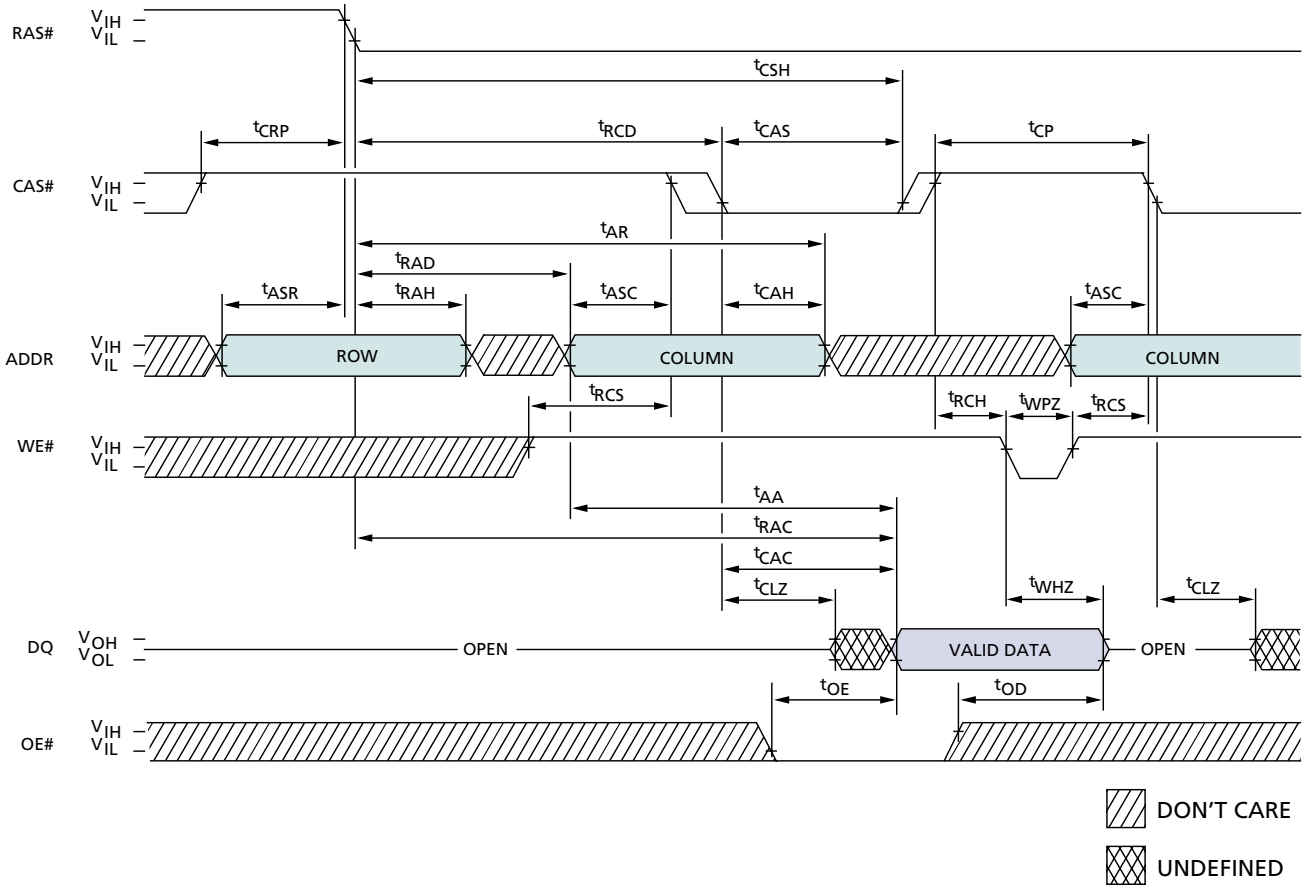



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOE | | 12 | | 15 | ns |
| tPC | 20 | | 25 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWHZ | | 12 | | 15 | ns |

## EDO READ CYCLE
(with WE#-controlled disable)

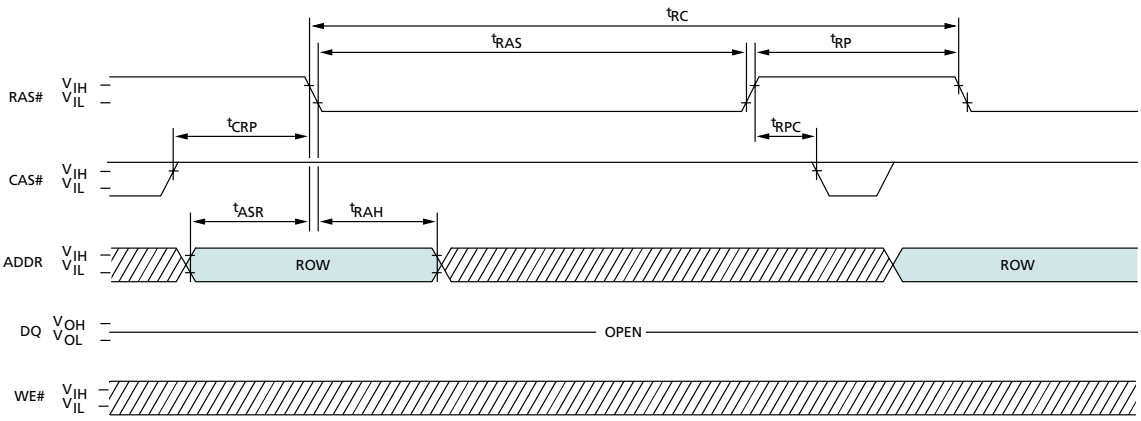



### TIMING PARAMETERS

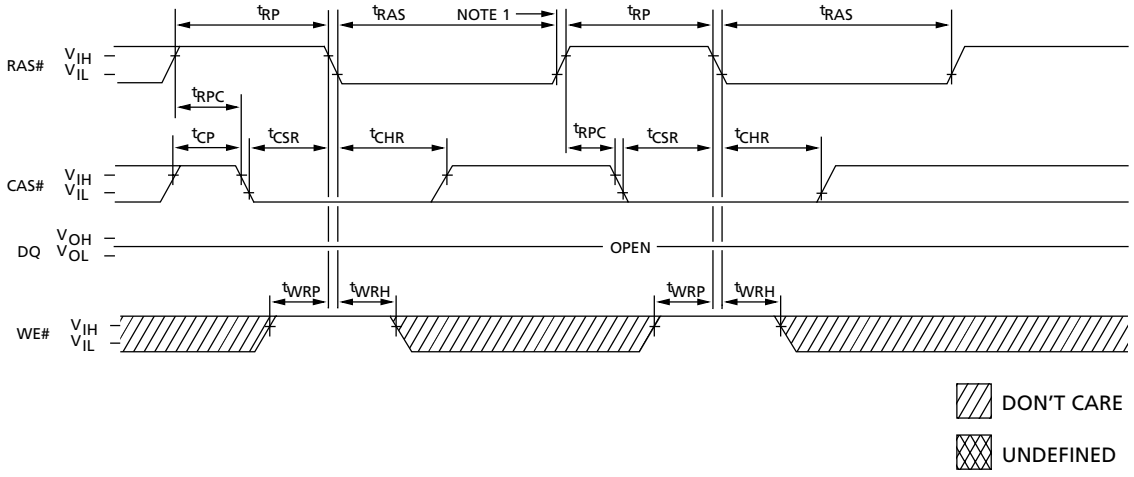
| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tWHZ | | 12 | | 15 | ns |
| tWPZ | 10 | | 10 | | ns |

## RAS#-ONLY REFRESH CYCLE




## CBR REFRESH CYCLE
(Addresses, OE# = DON'T CARE)

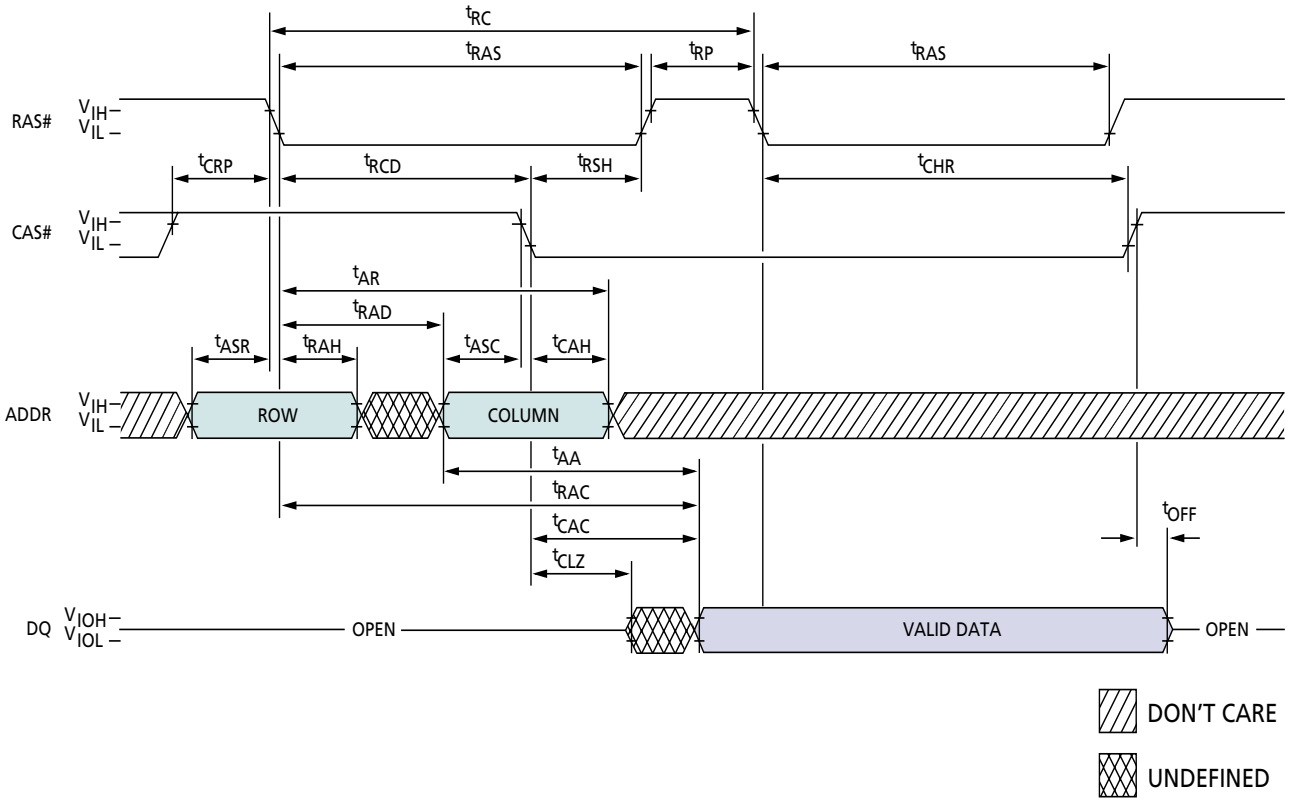



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tASR | 0 | | 0 | | ns |
| tCHR | 8 | | 10 | | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSR | 5 | | 5 | | ns |
| tRAH | 9 | | 10 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRP | 30 | | 40 | | ns |
| tRPC | 5 | | 5 | | ns |
| tWRH | 8 | | 10 | | ns |
| tWRP | 8 | | 10 | | ns |

## HIDDEN REFRESH CYCLE [20]
(WE# = HIGH; OE# = LOW)

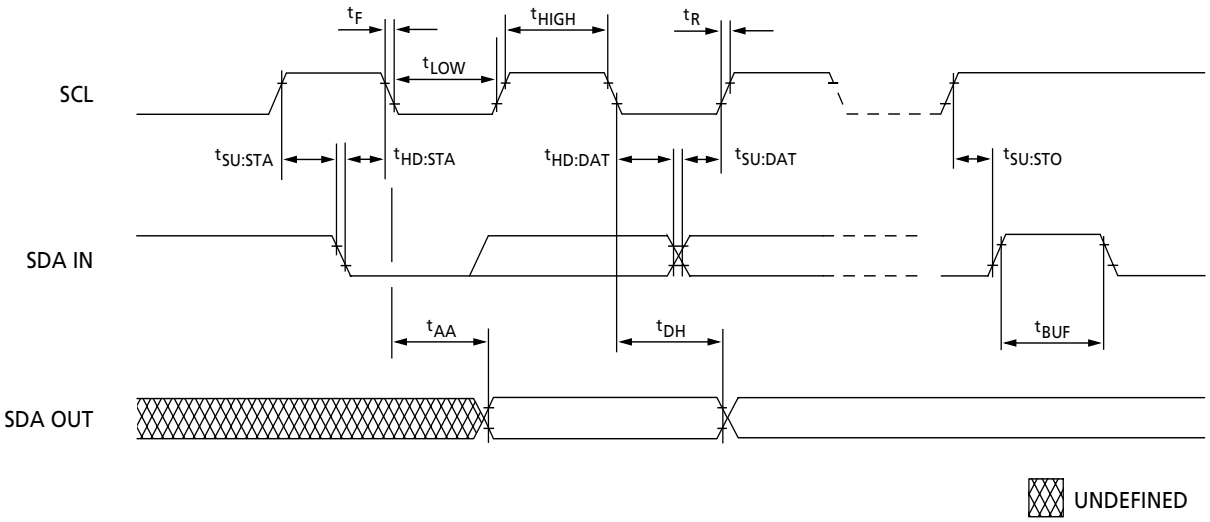



### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCHR | 8 | | 10 | | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tOD | 0 | 12 | 0 | 15 | ns |
| tOE | | 12 | | 15 | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tOFF | 0 | 12 | 0 | 15 | ns |
| tORD | 0 | | 0 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |

## SPD EEPROM

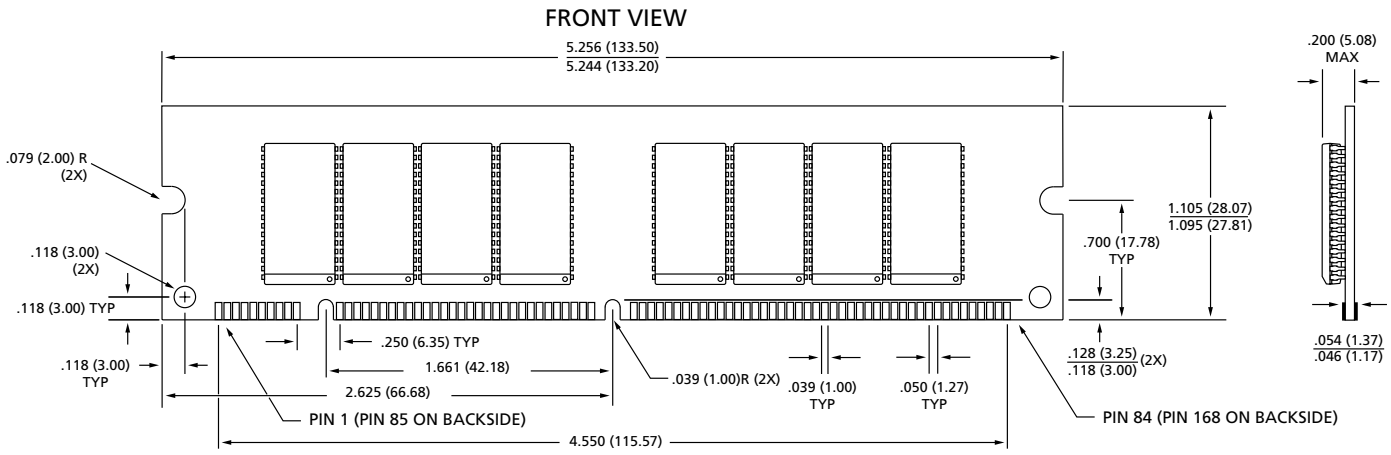



## SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

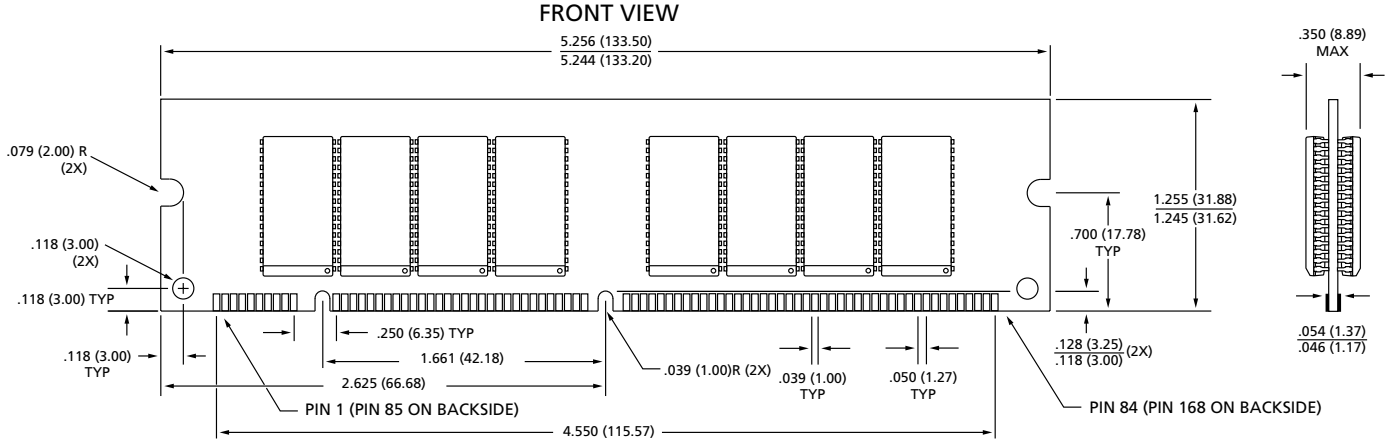
| SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|
| tAA | 0.3 | 3.5 | µs |
| tBUF | 4.7 | | µs |
| tDH | 300 | | ns |
| tF | | 300 | ns |
| tHD:DAT | 0 | | µs |
| tHD:STA | 4 | | µs |

| SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|
| tHIGH | 4 | | µs |
| tLOW | 4.7 | | µs |
| tR | | 1 | µs |
| tSU:DAT | 250 | | ns |
| tSU:STA | 4.7 | | µs |
| tSU:STO | 4.7 | | µs |

## 168-PIN DIMM
DF-16 (64MB)

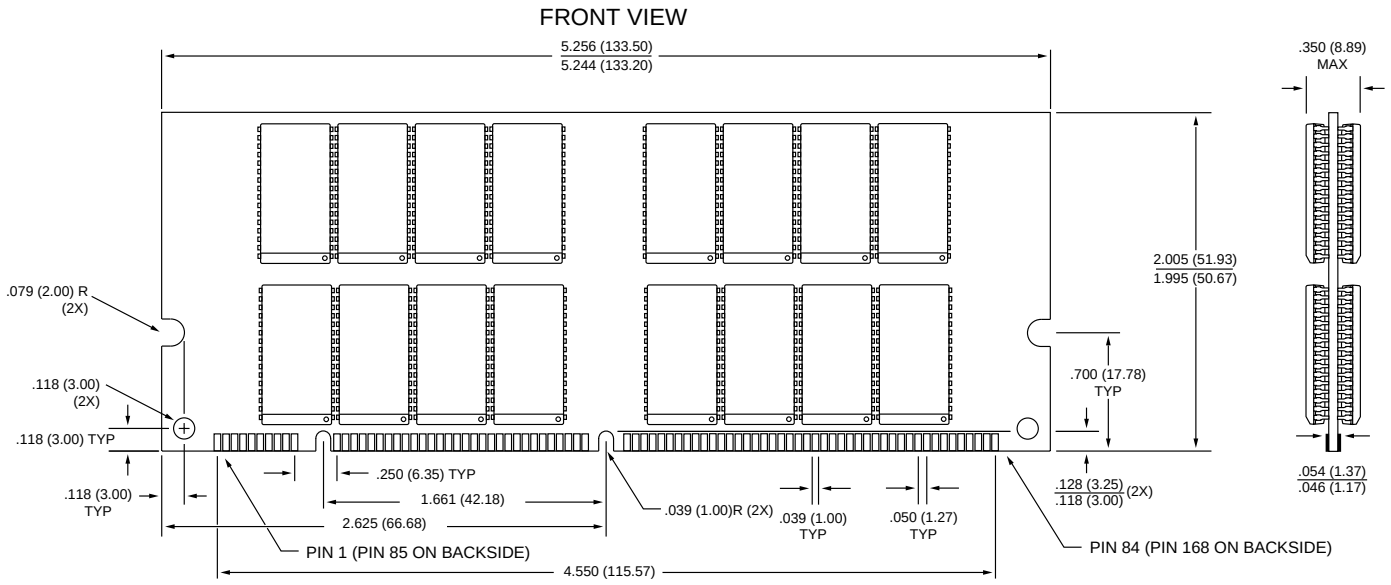



## 168-PIN DIMM
DF-27 (128MB)




**NOTE:** All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

## 168-PIN DIMM
DF-41 (256MB)




**NOTE:** All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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