

ntertace

## Synchronous Boost Converter with 600mA High Side LED Driver and I<sup>2</sup>C-Compatible Interface

### **General Description**

The LM3561 is a 2 MHz fixed-frequency, current mode synchronous boost converter. The device is designed to operate as a single 600mA constant current driver for high-current white LEDs. The high side current source allows for grounded cathode LED operation while the 250mV regulated headroom voltage ensures that the LED current is well regulated and efficiency remains high.

The main features of the LM3561 include: an I<sup>2</sup>C-compatible interface for controlling the LED current, a hardware Flash enable input for direct triggering of the Flash pulse, dual TX inputs (TX1 and TX2) which force the Flash pulse into a lowcurrent Torch mode during high battery current instances, an active high hardware enable (HWEN) allowing for fast hardware shutdown during system software failures, a dual mode pin which serves as either an indicator LED driver at up to 18mA or as a dedicated comparator input with an internal 1V reference, designed to monitor the voltage across a negative temperature coefficient thermistor (NTC), and a programmable input voltage monitor which monitors IN and can reduce the flash current or shutdown the device during low battery conditions.

Seven fault flags are available for read back over the I2Ccompatible bus. These include: a flash timeout flag indicating the flash pulse has reached the end of the programmable timeout duration, a thermal shutdown flag indicating the LM3561's die temperature has exceeded 150°C, an LED fault flag indicating the output voltage has tripped the over-voltage threshold, or the LED has become shorted, TX1 and TX2 interrupt flags indicating if either of the TX inputs have been triggered, an NTC flag indicating the LED has experienced an over temperature condition, and a VIN Monitor flag indicating the input voltage has fallen below the VIN Monitor threshold.

The LM3561 is available in a tiny (1.6mm × 1.2mm × 0.6mm) 12-bump micro-SMD and operates over the -40°C to +85°C temperature range.

### Features

- High Side Current Source allowing for Grounded LED Cathode
- Up to 90% Efficient
- Ultra-Small Solution Size: < 16mm<sup>2</sup>
- . Three Operating Modes: Torch, Flash, and LED Indicator
- Accurate and Programmable LED Current from 18mA to -600mA
- Hardware Flash and Torch Enable
- LED Thermal Sensing and Current Scaleback
- Software Selectable Input Voltage Monitor
- Programmable Flash Timeout
- Dual Synchronization Inputs for RF Power Amplifier Pulse **Events**

COUT

- Open and Short LED Detection
- Active High Hardware Enable for Protection Against System Faults
- 400kHz I<sup>2</sup>C-compatible Interface
- 12-Bump (1.6mm × 1.2mm × 0.6mm) µSMD

## Applications

- Camera Phone LED Flash Controller
- LED Current Source Biasing

## **Typical Application Circuits**



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30113902

## **Application Circuit Component List**

Component	Manufacturer	Value	Part Number	Size (mm)	Rating
L	TDK	1µH	MLP2520-1R0	2x2.5x1.2	1.5A
COUT	Murata	10µF	GRM188R60J106M	1.6×0.8×0.8 (0603)	6.3V
CIN	Murata	10µF	GRM188R60J106M	1.6×0.8×0.8 (0603)	6.3V
LEDs	Lumiled	3.6V@1A	LXCL-PWF4		1.5A

## **Connection Diagram**



## **Pin Descriptions**

Pin	Name	Function
A1	GND	Ground
A2	IN	Input Voltage Connection. Connect IN to the input supply and bypass to GND with a minimum $10\mu F$ ceramic capacitor.
A3	HWEN	Active Low Hardware Reset Input. This input is high impedance and cannot be left floating. Typically this would be tied to a pullup resistor and to a logic high voltage, or VIN, in order to enable the LM3561.
B1	SW	Drain Connection for Internal NMOS and Synchronous PMOS Switches
B2	STROBE	Active High Hardware Flash Enable. Drive STROBE high to turn on the Flash pulse. STROBE has an internal $300k\Omega$ pulldown to GND.
B3	SCL	Serial Clock Input.
C1	OUT	Step-Up DC/DC Converter Output. Bypass OUT to GND with a 10µF Ceramic Capacitor.
C2	TX1/TORCH/ GPIO	Configurable as a Flash Interrupt Input, a Hardware Torch Enable, or a Programmable General Purpose Logic Input/Output. This pin has an internal $300k\Omega$ pulldown to GND.
C3	SDA	Serial Data Input/Output.
D1	LED	High Side Current Source Output for Flash LED.
D2	LEDI/NTC	Configurable as a High Side Current Source Output for Indicator LEDs or as a Threshold Detector for LED Temperature Sensing.
D3	TX2/GPIO2/INT	Configurable as a Flash Interrupt Input, a Programmable General Purpose Logic Input/Output, or as an Interrupt output for fault notification. This pin has an internal $300 k\Omega$ pulldown to GND.

Ordering Information							
Order Number	Package	Top Marking 2 Lines: First line XY, where X is the single digit date code and Y is the die run code, Second line has the letters DV	Supplied As	No-Lead			
LM3561TME	TMD12AAA	XY	250 units, Tape-and-Reel				
LM3561TMX	TMD12AAA	XY	3000 units, Tape-and-Reel	TES (NOPB)			

## Absolute Maximum Ratings (Note 1, Note

### <u>2</u>)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN, VSW, VOLT	-0.3V to 6V
V <sub>SCL</sub> , V <sub>SDA</sub> , V <sub>HWEN</sub> , V <sub>STROBE</sub> , V <sub>TX1</sub> ,	-0.3V to (V <sub>IN</sub>
V <sub>TX2</sub> , V <sub>LED</sub> , V <sub>LEDI/NTC</sub>	+0.3V) w/ 6.0V
	max
Continuous Power Dissipation( <i>Note 3</i> )	Internally Limited
Junction Temperature (T <sub>J-MAX</sub> )	+150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature	
(Soldering)	(Note 4)

### Operating Ratings (Note 1, Note 2)

V <sub>IN</sub>	2.5V to 5.5V
Junction Temperature (T <sub>J</sub> )	-40°C to +125°C
Ambient Temperature (T <sub>A</sub> ) ( <i>Note 5</i> )	-40°C to +85°C
< - / / / / / / / / / / / / / / / / / /	

## **Thermal Properties**

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ), TMD12 Package(*Note 6*)

68°C/W

**ESD Caution Notice** National Semiconductor recommends that all integrated circuits be handled with appropriate ESD precautions. Failure to observe proper ESD handling techniques can result in damage to the device.

## **Electrical Characteristics**

Limits in standard typeface are for  $T_A = +25^{\circ}$ C. Limits in **boldface** type apply over the full operating ambient temperature range (-40°C  $\leq T_A \leq +85^{\circ}$ C). Unless otherwise specified,  $V_{IN} = 3.6$ V,  $V_{HWEN} = V_{IN}$ . (*Note 2, Note 7*)

Symbol	Parameter	Conditio	ons	Min	Тур	Max	Units
Current Source	ce Specifications						
		600mA Flash LED Setting, V <sub>OUT</sub> = 4.5V,	-40C ≤ T <sub>A</sub> ≤ +85C	-5%	600	+6%	
I <sub>LED</sub>	Current Source Accuracy	$3V \le V_{IN} \le 4.2V$	T <sub>A</sub> = +25C	-3%	600	+6%	mA
		18mA Torch Current Se $3V \le V_{IN} \le 4.2V$	etting, V <sub>OUT</sub> = 4.5V,	-10%	18	+10%	
V <sub>HR</sub>	Current Source Regulation Voltage (V <sub>OUT</sub> - V <sub>LED</sub> )	600mA setting, V <sub>OUT</sub> =	4.5V		240		mV
Step-Up DC/D	C Converter Specifications	6				3	
	Output Over-Voltage	On Threshold		4.90	5	5.05	
V <sub>OVP</sub>	Protection Trip Point( <i>Note</i> 8)	Off Threshold			4.88		V
R <sub>PMOS</sub>	PMOS Switch On- Resistance	I <sub>PMOS</sub> = 500mA			270		mΩ
R <sub>NMOS</sub>	NMOS Switch On- Resistance	I <sub>NMOS</sub> = 500mA			250		mΩ
	Switch Current Limit(Note		Flash Duration Register Bit [5] = 0	0.88	1	1.12	
ICL	9)	$3.0V \leq V_{\rm IN} \leq 4.2V$	Flash Duration Register Bit [5] = '1'	1.35	1.5	1.65	A
I <sub>OUT_SC</sub>	Output Short Circuit Current Limit	V <sub>OUT</sub> < 2.3V			200		mA
I <sub>LED/NTC</sub>	Indicator Current	Indicator Register = 0xFF, $V_{LEDI/NTC}$ = 2V, 2.7V $\leq V_{IN} \leq 4.2V$		16	18	20	mA
V <sub>TRIP</sub>	Comparator Trip Threshold	Configuration Register 1 Bit [4] = '1', 3.0V $\leq V_{IN} \leq 4.2V$		0.97	1	1.03	V
f <sub>SW</sub>	Switching Frequency	$2.7V \le V_{\rm IN} \le 5.5V$		1.8	2	2.2	MHz
t <sub>TIMEOUT</sub> ( <i>Note</i> <i>10</i> ), ( <i>Note 11</i> )	Timeout Duration	$2.7V \le V_{\rm IN} \le 5.5V$		-10		+10	%

	Symbol	Parameter	Conditions	Min	Тур	Max	Units
			Device Not Switching		676		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	۱ <sub>Q</sub>	Quiescent Supply Current	Device Switching		1140		μA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			Indicate Mode, Indicator Register = 0x07		560		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	I <sub>SHDN</sub>	Shutdown Supply Current	$2.7V \le V_{IN} \le 5.5V$ , HWEN = GND		0.02	1	μA
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	I <sub>STBY</sub>	Standby Supply Current	$2.7V \le V_{IN} \le 5.5V$ , HWEN = IN, Enable Register bit [1:0] = 00		1.1	2.3	μA
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		Flash-to-Torch LED Current Settling Time	TX_Low-to-High, I <sub>LED</sub> = 600mA to 93.2mA		2		
	t <sub>TX</sub>	Torch-to-Flash LED Current Settling Time	TX_Low-to-High, I <sub>LED</sub> = 93.2mA to 600mA		80		μs
HWEN, STROBE, TX1/TORCH/GPI01, TX2/INT/GPI02 Voltage Specifications $V_{IL}$ Input Logic Low $2.7V \le V_{IN} \le 5.5V$ 00.4 $V_{H1}$ Input Logic High $2.7V \le V_{IN} \le 5.5V$ 1.2 $V_{IN}$ $V_{OL}$ Output Logic Low(GPI01, GPI02, INT) $I_{LOAD} = 3mA, 2.7V \le V_{IN} \le 5.5V$ 0.4 $R_{TX1}$ Resistance at TX1/30030010 $DRCH/GPI01$ 3001010 $R_{TX2}$ Internal Pulldown300300 $R_{TX2}$ Internal Pulldown30010Resistance at TX2/GPI0230030010 $R_{TX2}$ Internal Pulldown30010Resistance at STROBE3001010 <b>PC-Compatible Voltage Specifications (SCL, SDA)</b> 00.4 $V_{IL}$ Input Logic Low $2.7V \le V_{IN} \le 5.5V$ 00 $V_{IL}$ Input Logic Clow $2.7V \le V_{IN} \le 5.5V$ 1.3 $V_{IN}$ $V_{UL}$ Input Logic Clow $2.7V \le V_{IN} \le 5.5V$ 40010 $V_{IL}$ Input Logic Clow $2.7V \le V_{IN} \le 5.5V$ 1.3 $V_{IN}$ $V_{IL}$ Input Logic Clow $2.7V \le V_{IN} \le 5.5V$ 40010 $V_{IL}$ Input Logic Clow $2.7V \le V_{IN} \le 5.5V$ 1.3 $V_{IN}$ $V_{IL}$ Input Logic Clow $2.7V \le V_{IN} \le 5.5V$ 40010 $V_{IL}$ ScLSCLSCLScLScL $I_{SCL}$ SCL(Clock Frequency)040014 $I_{SCL}$ ScLScL <td>V<sub>IN_TH</sub></td> <td>VIN Monitor Trip Threshold</td> <td>V<sub>IN</sub> Falling, VIN Monitor Register = 0x01 (Enabled with V<sub>IN TH</sub> = 2.9V)</td> <td>2.84</td> <td>2.90</td> <td>2.95</td> <td>V</td>	V <sub>IN_TH</sub>	VIN Monitor Trip Threshold	V <sub>IN</sub> Falling, VIN Monitor Register = 0x01 (Enabled with V <sub>IN TH</sub> = 2.9V)	2.84	2.90	2.95	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	HWEN, STRO	BE, TX1/TORCH/GPIO1, TX	2/INT/GPIO2 Voltage Specifications	LL			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	V <sub>IL</sub>	Input Logic Low	$2.7V \le V_{\rm IN} \le 5.5V$	0		0.4	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V <sub>IH</sub>	Input Logic High	$2.7V \le V_{\rm IN} \le 5.5V$	1.2		V <sub>IN</sub>	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	V <sub>OL</sub>	Output Logic Low (GPIO1,GPIO2, INT)	$I_{LOAD} = 3$ mA, 2.7V $\leq V_{IN} \leq 5.5$ V			0.4	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	R <sub>TX1</sub>	Internal Pulldown Resistance at TX1/ TORCH/GPIO1			300		kΩ
$ \begin{array}{ c c c c c c } \hline R_{STROBE} & Internal Pulldown \\ \hline Resistance at STROBE \\ \hline PC-Compatible Voltage Specifications (SCL, SDA) \\ \hline V_{L} & Input Logic Low & 2.7V \leq V_{IN} \leq 5.5V & 0 & 0.4 \\ \hline V_{H} & Input Logic Low (SDA) & 1_{LOAD} = 3mA, 2.7V \leq V_{IN} \leq 5.5V & 1.3 & V_{IN} \\ \hline V_{OL} & Output Logic Low (SDA) & 1_{LOAD} = 3mA, 2.7V \leq V_{IN} \leq 5.5V & 400 & 1 \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 \\ \hline f_{SCL} & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & ScL & SDA and \\ SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 400 & F \\ \hline t_{hise}(Note 12) & SCL & SCL(Clock Frequency) & 0 & 0 & 0 & 0 \\ \hline t_{LOW} & Low Period of SCL Clock & 1.3 & 0 & 0 \\ \hline t_{LOW} & Low Period of SCL Clock & 1.3 & 0 & 0 \\ \hline t_{high} & High Period of SCL Clock & 600 & 0 & 0 & 0 \\ \hline t_{high} & Start & 600 & 0 & 0 & 0 \\ \hline t_{high} & Start & 0 & 0 & 0 & 0 & 0 \\ \hline t_{high} & Data Hold Time & 0 & 0 & 0 & 0 & 0 \\ \hline t_{bu;DAT} & Data Setup Time & 100 & 0 & 0 & 0 \\ \hline t_{bu;DAT} & Data Valid Time & 0 & 0 & 0 & 0 & 0 \\ \hline t_{vD,OAT} & Data Valid Time & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline t_{vD,OACK} & Data Valid Acknowledge & 0 & 000 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $	R <sub>TX2</sub>	Internal Pulldown Resistance at TX2/GPIO2			300		kΩ
P2-Compatible Voltage Specifications (SCL, SDA) $V_{IL}$ Input Logic Low $2.7V \le V_{IN} \le 5.5V$ 00.4 $V_{H}$ Input Logic High $2.7V \le V_{IN} \le 5.5V$ 1.3 $V_{IN}$ $V_{OL}$ Output Logic Low (SDA) $I_{LOAD} = 3mA, 2.7V \le V_{IN} \le 5.5V$ 4000P2-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 $f_{SCL}$ SCL(Clock Frequency)0400 $f_{nISE}(Note 12)$ SCLSCL04000 $t_{nISE}(Note 12)$ SCLClock1.3300 $t_{FALL}(Note 12)$ Fall Time of Both SDA and SCL $20 + 0.1 \times$ CBUS $300$ $t_{raise}(Note 12)$ Fall Time of SCL Clock1.30 $t_{IOW}$ Low Period of SCL Clock1.30 $t_{HIGH}$ High Period of SCL Clock6000 $t_{HO,STA}$ Set-up Time for a Repeated Start6000 $t_{HO,DAT}$ Data Hold Time00 $t_{ND,DAT}$ Data Valid Time6000 $t_{VD,DACK}$ Data Valid Acknowledge Time500900	R <sub>STROBE</sub>	Internal Pulldown Resistance at STROBE			300		kΩ
$ \begin{array}{ c c c c c } \hline V_{IL} & Input Logic Low & 2.7V \leq V_{IN} \leq 5.5V & 0 & 0.4 \\ \hline V_{IH} & Input Logic High & 2.7V \leq V_{IN} \leq 5.5V & 1.3 & V_{IN} \\ \hline V_{OL} & Output Logic Low (SDA) & I_{LOAD} = 3mA, 2.7V \leq V_{IN} \leq 5.5V & 400 & 10 \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline PC-Compatible Time of Both SDA and SCL & & 0 & 400 & Identification & \\ \hline Prating (Note 12) Scl & SCL Clock & 1.3 & \\ \hline Prating H & High Period of SCL Clock & 1.3 & \\ \hline Prating H & High Period of SCL Clock & 1.3 & \\ \hline Prating H & High Period of SCL Clock & 600 & \\ \hline \hline Prating For Start (or Repeated Start) Condition & \\ \hline \hline Prating For a Repeated Start & \\ \hline Prating H & Data Hold Time & 0 & \\ \hline \hline Prating For a Repeated Start & \\ \hline \hline Prating For a Repeated Start & \\ \hline \hline Prating For a Repeated Start & \\ \hline \hline Prating For a Repeated Start & \\ \hline \hline \hline Prating For a Repeated Start & \\ \hline \hline \hline \hline Prating For a Repeated Start & \\ \hline \hline \hline \hline Prating For Stop Condition & \\ \hline \hline \hline \hline \hline Prating For Stop Condition & \\ \hline \hline \hline \hline \hline Prating For Stop Condition & \\ \hline \hline \hline \hline \hline \hline Prating For Stop Condition & \\ \hline \hline \hline \hline \hline \hline \hline \hline Prating For Stop Condition & \\ \hline \hline$	I <sup>2</sup> C-Compatib	le Voltage Specifications (	SCL, SDA)				
$ \begin{array}{ c c c c c } \hline V_{\rm  H} & \mbox{ Input Logic High} & 2.7 \forall \leq V_{\rm IN} \leq 5.5 \forall & 1.3 & V_{\rm IN} & \\ \hline V_{OL} & \mbox{ Output Logic Low (SDA)} & \mbox{ I_{LOAD}} = 3mA, 2.7 \forall \leq V_{\rm IN} \leq 5.5 \lor & 400 & 10 & \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & \\ \hline f_{SCL} & SCL(Clock Frequency) & 0 & 400 & 10 & \\ \hline f_{RISE}(Note 12) & \mbox{ Rise Time of Both SDA and SCL} & 20 + 0.1 \times & \\ \hline c_{BUS} & 300 & \\ \hline c_{RUS} & SCL & SCL & \\ \hline c_{RUS} & \\ \hline c_{RUS} & ScL & \\ \hline c_{RUS} &$	V <sub>IL</sub>	Input Logic Low	$2.7V \le V_{IN} \le 5.5V$	0		0.4	V
$\begin{array}{ c c c c c c }\hline V_{OL} & Output Logic Low (SDA) & I_{LOAD} = 3mA, 2.7V \leq V_{IN} \leq 5.5V & 0 & 400 & 10 \\ \hline PC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1 & 100 $	V <sub>IH</sub>	Input Logic High	$2.7V \le V_{IN} \le 5.5V$	1.3		V <sub>IN</sub>	V
IPC-Compatible Timing Specifications (SCL, SDA) (Note 10) see Figure 1           f <sub>SCL</sub> SCL(Clock Frequency)         0         400         if           t <sub>RISE</sub> (Note 12)         Rise Time of Both SDA and SCL         20 + 0.1 × C <sub>BUS</sub> 300         20 + 0.1 × C <sub>BUS</sub> 300           t <sub>RISE</sub> (Note 12)         Fall Time of Both SDA and SCL         20 + 0.1 × C <sub>BUS</sub> 300         300           t <sub>FALL</sub> (Note 12)         Fall Time of Both SDA and SCL         20 + 0.1 × C <sub>BUS</sub> 300         300           t <sub>LOW</sub> Low Period of SCL Clock         1.3         1         1           t <sub>LOW</sub> Low Period of SCL Clock         600         1         1           t <sub>HIGH</sub> High Period of SCL Clock         600         1         1           t <sub>HIGH</sub> High Period of SCL Clock         600         1         1           t <sub>HIGH</sub> High Period of SCL Clock         600         1         1           t <sub>HIGH</sub> High Period of SCL Clock         600         1         1           t <sub>HIGH</sub> High Period of SCL Clock         600         1         1           t <sub>HD,STA</sub> Set-up Time for a Repeated Start) Condition         600         1         1           t <sub>SU,DAT</sub> Data	V <sub>OL</sub>	Output Logic Low (SDA)	$I_{LOAD} = 3mA, 2.7V \le V_{IN} \le 5.5V$			400	mV
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	I <sup>2</sup> C-Compatib	le Timing Specifications (S	CL, SDA) (Note 10) see Figure 1	-		-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	f <sub>SCL</sub>	SCL(Clock Frequency)		0		400	kHz
t       Fall Time of Both SDA and SCL       20 + 0.1 × C <sub>BUS</sub> 300         t       Low Period of SCL Clock       1.3       -         t       High       High Period of SCL Clock       600       -         t       High       High Period of SCL Clock       600       -         t       Hold Time for Start (or Repeated Start) Condition       600       -       -         t       Set-up Time for a Repeated Start) Condition       600       -       -         t       Set-up Time for a Repeated Start)       600       -       -         t       Set-up Time for a Repeated Start       600       -       -         t       Set-up Time for a Repeated Start       600       -       -         t       Set-up Time for Stop Condition       0       -       -         t       Set-up Time for Stop Condition       600       -       -         t       Set-up Time for Stop Condition       600       -       -       -         t       Set-up Time for Stop Condition       600       -       -       -         t       VD;DAT       Data Valid Acknowledge Time       -       900       -       -         t       VD;ACK       Data Valid	t <sub>RISE</sub> ( <i>Note 12</i> )	Rise Time of Both SDA and SCL		20 + 0.1 × C <sub>BUS</sub>		300	ns
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	t <sub>FALL</sub> ( <i>Note 12</i> )	Fall Time of Both SDA and SCL		20 + 0.1 × C <sub>BUS</sub>		300	ns
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	t <sub>LOW</sub>	Low Period of SCL Clock		1.3			μs
t_{HD;STAHold Time for Start (or Repeated Start) Condition600t_{SU;STASet-up Time for a Repeated Start600t_{HD;DATData Hold Time0t_{SU;DATData Setup Time100t_{SU;STOSet-up Time for Stop Condition600t_{SU;STOSet-up Time for Stop Condition600t_{VD;DATData Valid Time900t_VD;ACKData Valid Acknowledge Time900	t <sub>HIGH</sub>	High Period of SCL Clock		600			ns
$ \begin{array}{c c c c c c c c c } \hline t_{SU;STA} & Set-up Time for a Repeated \\ \hline Start & \\ \hline Start & \\ \hline Start & \\ \hline Data Hold Time & & & & & & & \\ \hline t_{HD;DAT} & Data Hold Time & & & & & & & \\ \hline t_{SU;DAT} & Data Setup Time & & & & & & & \\ \hline t_{SU;STO} & Set-up Time for Stop \\ \hline Condition & & & & & & & & \\ \hline t_{VD;DAT} & Data Valid Time & & & & & & & & & \\ \hline t_{VD;ACK} & & & & & & & & & & \\ \hline t_{VD;ACK} & & & & & & & & & & \\ \hline t_{VD;ACK} & & & & & & & & & & \\ \hline t_{VD;ACK} & & & & & & & & & & & \\ \hline \end{array} $	t <sub>HD;STA</sub>	Hold Time for Start (or Repeated Start) Condition		600			ns
$ \begin{array}{c c c c c c c c c } \hline t_{HD;DAT} & Data Hold Time & 0 & & & \\ \hline t_{SU;DAT} & Data Setup Time & 100 & & & \\ \hline t_{SU;STO} & Set-up Time for Stop & 600 & & & \\ \hline t_{VD;DAT} & Data Valid Time & & 900 & \\ \hline t_{VD;ACK} & Data Valid Acknowledge & & & 900 & \\ \hline \end{array} $	t <sub>SU;STA</sub>	Set-up Time for a Repeated Start		600			ns
t <sub>SU;DAT</sub> Data Setup Time     100       t <sub>SU;STO</sub> Set-up Time for Stop Condition     600     600       t <sub>VD;DAT</sub> Data Valid Time     900       t <sub>VD;ACK</sub> Data Valid Acknowledge Time     900	t <sub>HD;DAT</sub>	Data Hold Time		0			ns
t <sub>SU;STO</sub> Set-up Time for Stop Condition     600       t <sub>VD;DAT</sub> Data Valid Time     900       t <sub>VD;ACK</sub> Data Valid Acknowledge Time     900	t <sub>SU;DAT</sub>	Data Setup Time		100			ns
t <sub>VD;DAT</sub> Data Valid Time     900       t <sub>VD;ACK</sub> Data Valid Acknowledge     900	t <sub>su;sto</sub>	Set-up Time for Stop Condition		600			ns
Data Valid Acknowledge 900	t <sub>VD;DAT</sub>	Data Valid Time				900	ns
	t <sub>VD;ACK</sub>	Data Valid Acknowledge Time				900	ns
tBUF     Bus Free Time Between a Start and a Stop Condition     1.3	t <sub>BUF</sub>	Bus Free Time Between a Start and a Stop Condition		1.3			μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics table.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J=150^{\circ}C$  (typ.) and disengages at  $T_J=135^{\circ}C$  (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1112: Micro SMD Wafer Level chip Scale Package (AN-1112)

**Note 5:** In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature  $(T_{A-MAX})$  is dependent on the maximum operating junction temperature  $(T_{J-MAX-OP} = +125^{\circ}C)$ , the maximum power dissipation of the device in the application  $(P_{D-MAX})$ , and the junction-to-ambient thermal resistance of the part/package in the application  $(\theta_{JA})$ , as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$ .

**Note 6:** Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102mm x 76mm x 1.6mm with a 2x1 array of thermal via's. The ground plane on the board is 50mm x 50mm. Thickness of copper layers are 36µm/18µm/36µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical (Typ) numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are:  $V_{IN} = 3.6V$  and  $T_A = +25^{\circ}C$ .

**Note 8:** The typical curve for Over-Voltage Protection (OVP) is measured in closed loop using the typical application circuit . The OVP value is found by forcing an open circuit in the LED current path and recording the peak value of  $V_{OUT}$ . The value given in the Electrical Table is found in an open loop configuration by ramping the voltage at OUT until the OVP comparator trips. The closed loop data can appear higher due to the stored energy in the inductor being dumped into the output capacitor after the OVP comparator trips. This results in an open circuit condition where the output voltage can continue to rise after the OVP comparator trips by approximately  $I_{IN} \times \text{sqrt}(L/C_{OUT})$ .

**Note 9:** The typical curve for Current Limit is measured in closed loop using the typical application circuit by increasing  $I_{OUT}$  until the peak inductor current stops increasing. The value given in the Electrical Table is measured open loop and is found by forcing current into SW until the current limit comparator threshold is reached. Closed loop data appears higher due to the delay between the comparator trip point and the NFET turning off. This delay allows the closed loop inductor current to ramp higher after the trip point by approximately  $40n \times V_{IN}/L$ 

Note 10: Guaranteed by design. Not production tested.

Note 11: The timeout duration period is a divided down representation of the 2MHz clock and thus the accuracy spec. is the same as the switching frequency. This accuracy spec. applies to all settings in *Table 8*.

Note 12: Min rise and fall times on SDA and SCL can typically be less than 20ns.



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**Typical Performance Characteristics**  $V_{IN} = 3.6V$ , LEDs are Lumiled PWF-4,  $C_{OUT} = 10\mu$ F,  $C_{IN} = 10\mu$ F, L = MLP2520-1R0 (1 $\mu$ H,  $R_L = 0.085\Omega$ ),  $T_A = +25^{\circ}C$  unless otherwise specified.





LED Efficiency vs V<sub>IN</sub> Flash Brightness Codes (0011 - 0000)



LED Current vs V<sub>IN</sub> Flash Brightness Codes (1011 - 1000)











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LM3561

LM3561



## **Circuit Description**

### **OVERVIEW**

The LM3561 is a high power white LED flash driver capable of delivering up to 600mA of LED current into a single white LED. The device incorporates a 2MHz constant frequency, synchronous boost converter, and a high side current source to regulate the LED current over the 2.5V to 5.5V input voltage range.

When the LM3561 is enabled and the output voltage is greater than  $V_{IN}$  – 150mV, the PWM converter switches and maintains at least 250mV ( $V_{HR}$ ) across the current source ( $V_{OUT}$  -V<sub>LED</sub>). This minimum headroom voltage ensures that the current sinks remain in regulation. When the input voltage is above  $V_{LED} + V_{HR}$  the device operates in pass mode with the device not switching and the PFET on continuously. In pass mode the difference between (V\_IN - I\_LED  $\times R_{ON\ P}$ ) and V\_LED is dropped across the current source. If the device is operating in pass mode and  $V_{\mbox{\scriptsize IN}}$  drops to a point that forces the device into switching, the LM3561 will make a one-time decision to jump into switching mode. The LM3561 remains in switching mode until the device is shutdown and re-enabled. This is true even if  $V_{IN}$  were to rise back above  $V_{LED}$  + 250mV during the active Flash or Torch cycle. This prevents the LED current from oscillating back and forth between pass and boost mode when  $V_{IN}$  is close to  $V_{OUT}$ .

The main features of the LM3561 include: dual TX inputs (TX1 and TX2) for forcing the device into a lower current state during high battery current conditions, a hardware flash enable input (STROBE), an active low shutdown input (HWEN), an input voltage monitor for detecting low battery voltage conditions, and a dual function pin that can be configured as a low power indicator LED current source or as a comparator input for LED thermal sensing via an external NTC thermistor.

Control of the LM3561 is done via an I<sup>2</sup>C-compatible interface. This includes: adjustment of the LED current in TORCH and FLASH mode, adjustment of the indicator LED current, programming the flash LED current limeout duration, and programming of the switch current limit. Additionally, there are 7 flag bits that can be read back indicating that the programmed flash current timeout has expired, a device over temperature condition has happened, an LED failure (open or short), an LED thermal failure (tripping of the internal NTC comparator), an input under voltage fault (VIN Monitor), and a separate flag for each TX input.

### STARTUP

Turn on of the LM3561 via the I<sup>2</sup>C-compatible interface is done through bits [1:0] of the Enable Register. The device can be enabled in either Indicate mode, Torch mode, or Flash mode (see *Table 2*). On startup in Flash or Torch mode, when  $V_{OUT}$  is less than  $V_{IN}$ , the internal synchronous PFET turns on as a current source and delivers typically 200mA to the output capacitor. During this time the flash LED current source (LED) is off. When the voltage across the output capacitor reaches 2.3V the current source can turn on. At turn-on, the current source steps through each FLASH and TORCH level until the target LED current is reached (32 µs/step). This gives the device a controlled turn-on and limits inrush current from the  $V_{IN}$  supply.

### PASS MODE

On turn on, when the output voltage charges up to ( $V_{\rm IN}-150$  mV), the LM3561 will decide if the part operates in Pass Mode or Boost mode. If the voltage difference between  $V_{OUT}$  and  $V_{LED}$  is less than 250mV, the device will transition into Boost

Mode. If the difference between V<sub>OUT</sub> and V<sub>LED</sub> is greater than 250mV, the device will operate in Pass Mode. In Pass Mode the boost converter stops switching and the synchronous PFET turns fully on, bringing V<sub>OUT</sub> up to (V<sub>IN</sub> – I<sub>IN</sub>×R<sub>PMOS</sub>) where (R<sub>PMOS</sub> = 240mΩ). In Pass Mode the inductor current is not limited by the peak current limit. In this situation the output current must be limited to 1.5A.

### **OVER-VOLTAGE PROTECTION**

The output voltage is limited to typically 5V (4.9V min). In situations such as the current source open, the LM3561 will raise the output voltage in order to try and keep the LED current at its target value. When V<sub>OUT</sub> reaches 5V, the overvoltage comparator will trip and turn off both the internal NFET and PFET switches. When V<sub>OUT</sub> falls below 4.8V (typical) the LM3561 will begin switching again.

### **CURRENT LIMIT**

The LM3561 features 2 selectable current limits — 1A and 1.5A. These are selectable through the  $l^2C$ -compatible interface via bit [5] of the Flash Duration Register. When the current limit is reached the LM3561 stops switching for the remainder of the switching cycle.

Since the current limit is sensed in the NMOS switch there is no mechanism to limit the current when the device operates in Pass Mode. In situations where there could potentially be large load currents at OUT, and the LM3561 is operating in Pass mode, the load current must be limited to 1.5A. In Boost mode or Pass mode if  $V_{OUT}$  falls below approximately 2.3V the part stops switching and the PFET operates as a current source limiting the current to typically 200mA. This prevents damage to the LM3561 and excessive current draw from the battery during output short circuit conditions.

### THERMAL SHUTDOWN

The LM3561 features a thermal shutdown threshold of typically +150°C. When the die temperature reaches +150°C, the active current source (LED) will shutdown, and the TSD flag in the Flags register is written high. The device cannot be started up again until the Flags register is read back. Once the Flags register is read back the current source can be reenabled into Torch, or Flash Mode. The thermal shutdown (TSD) circuitry has an internal 250µs de-glitch timer which helps prevent unwanted noise from falsely triggering a TSD event. However, when the LM3561 is in boost mode at higher flash currents, the de-glitch timer can get reset by the high currents in the LM3561's GND. As a result the thermal shutdown's internal de-glitch timer can get reset before the TSD event can get latched in. This causes a TSD event to not get triggered until the LM3561's flash pulse reaches the end of the flash duration, when the noisy currents have dropped to a lower level. However, once the noise is lower and a TSD event is triggered, the next flash pulse is not allowed until the flags register is read back. In pass mode the boost switcher is off and the lower noise environment allows the devices TSD circuitry to shutdown immediately when the die temperature reaches +150°C.

### **FLASH MODE**

In Flash mode the LED current source (LED) provides 16 different current levels from typically 36mA to 600mA. The Flash currents are set by writing to bits [3:0] of the Flash Brightness Resister. Flash mode is activated by either writing a (1, 1) to bits [1:0] of the Enable Register, or by pulling the STROBE pin high. Once the Flash sequence is activated the current source (LED) will ramp up to the programmed Flash current by stepping through all Torch and Flash levels (32µs/step) until the programmed current is reached.

### **FLASH TERMINATION**

Bit [2] of the Enable Register determines how the Flash pulse terminates. With this bit = '1' the Flash current pulse will only terminate by reaching the end of the Flash timeout period (see *Figure 6*). With STR = '0', Flash mode can be terminated by pulling STROBE low, programming bits [1:0] of the Enable Register with (0,0), or by allowing the Flash timeout period to elapse (see *Figure 5*). If STR = '0' and STROBE is toggled before the end of the Flash timeout period, the timeout period resets on the rising edge of STROBE. See *LM3561 Timing Diagrams* regarding the Flash pulse termination for the different STR bit settings.

After the Flash pulse terminates, either by a flash timeout, pulling STROBE low, or disabling it via the I<sup>2</sup>C-compatible interface, the current source (LED) turns completely off. This happens even when Torch is enabled via the I<sup>2</sup>C-compatible interface and the Flash pulse is turned on by toggling STROBE. After a Flash event ends (bits [1:0] of the Enable Register are automatically re-written with (0, 0).

### **FLASH TIMEOUT**

The Flash timeout period sets the maximum duration of the flash current pulse. Bits [4:0] of the Flash Duration Register programs the 32 different Flash timeout levels in steps of 32ms, giving a Flash timeout range of 32ms to 1024ms (see *Table 8*).

### **TORCH MODE**

In Torch mode the current source (LED) provides 8 different current levels (see *Table 6*). The Torch currents are adjusted by writing to bits [2:0] of the Torch Brightness Register. Torch mode is activated by setting Enable Register bits [1:0] to (1, 0). Once the Torch mode is enabled the current sources will ramp up to the programmed Torch current level by stepping through all of the Torch currents at (32µs/step) until the programmed Torch current level.

### FLASH PULSE INTERRUPT (TX1), HARDWARE TORCH INPUT (TORCH) AND GENERAL PURPOSE I/O (GPIO1)

The TX1/TORCH/GPIO1 input has a triple function; either as a flash pulse interrupt (TX1), a hardware torch mode enable (TORCH), or as a general purpose I/O (GPIO1).

### Flash Interrupt (TX1)

With Configuration Register 1 Bit [7] = '0' (default), TX1/ TORCH/GPIO1 is a flash pulse interrupt input. This is designed to force the flash pulse into a lower current state in order to reduce the current pulled from the battery during high battery current situations. For example, when the LM3561 is engaged in a Flash event and TX1 is pulled high (active high polarity) the current source (LED) is forced into Torch mode at the programmed Torch current setting. If TX1 is then pulled low before the Flash pulse terminates, the LED current will ramp back to the previous Flash current level. At the end of the Flash timeout, whether TX1 is high or low, the LED current will turn off.

### **TX1 Polarity**

In TX1 mode, TX1 can be programmed as an active low TX1 input where pulling TX1 to GND will cause a TX1 event. TX1 polarity inversion is done via Configuration Register 1 bit [5].

### Hardware Torch Mode

With Configuration Register 1 Bit [7] = '1', TX1/TORCH/ GPIO1 is configured as a hardware Torch mode enable. In this mode (TORCH mode), a high at TORCH turns on the LED current at the programmed Torch current setting. The STROBE input and I<sup>2</sup>C Enabled flash take precedence over TORCH mode. In hardware torch mode, both the LED current source will turn off after a flash event and Configuration Register 1 Bit [7] will be reset to '0'. In this situation, to re-enter torch mode via hardware torch, the hardware torch enable bit (Configuration Register 1 Bit [7] must be reset to '1'). , , and detail the functionality of the TX1/TORCH input.

### **GPIO1 Mode**

With GPIO Register bit[0] = '1', the TX1/TORCH/GPIO1 pin is configured as a general purpose I/O. In GPIO1 mode this pin can be either a logic input or a logic output depending on the bit settings in bits [2:1] of the GPIO Register (see *Table 4*).

## FLASH PULSE INTERRUPT (TX2), GENERAL PURPOSE I/O (GPIO2), AND INTERRUPT OUTPUT (INT)

The TX2/GPIO2/INT pin has a triple function: either a flash interrupt input (TX2), a general purpose I/O (GPIO2), or as an interrupt output (INT).

### Flash Interrupt (TX2 Mode)

In TX2 mode (default), TX2 is a flash pulse interrupt input. This is designed to force the flash pulse into a lower current state in order to reduce the current pulled from the battery during high battery current situations. For example, when the LM3561 is engaged in a Flash event, and TX2 is pulled high (active high polarity, the current source (LED) is forced into torch mode at the programmed Torch current setting. If TX2 is then pulled low before the flash pulse terminates, the LED current will step back to the previous flash current level. At the end of the flash timeout, whether the TX2 pin is high or low, the LED current will turn off. In addition to forcing torch mode with a TX2 event, the TX2 input can be set to force shutdown. Configuration Register 2 bit[0] sets this mode (see Table 11). In TX2 shutdown mode, a TX2 event will shut down the flash pulse. Once shut down, the flash pulse must be re-enabled via STROBE or the flash enable bits in the Enable Register.

### **TX2 Forcing Shutdown**

TX2 also has the capability to force shutdown (see Figure 7). When bit [0] of Configuration Register 2 is set to a '1', TX2 will force shutdown when active. For example, if TX2 is configured for TX2 mode with active high polarity, and bit [0] of Configuration Register 2 is set to '1' then when TX2 is driven high, (LED) will be forced into shutdown. Once the current source is forced into shutdown by activating TX2, the current source can only be re-enabled in flash mode if TX2 is pulled low, and the Flags register is read back. If only the Flags register is read back and TX2 is kept high, the device will be reenabled into torch mode and not shutdown. This occurs because the TX2 shutdown feature is an edge-triggered event. With active high polarity the TX2 shutdown requires a rising edge at TX2 in order to force the current source back into shutdown. Once shut down, it takes a read back of the flags Register and another rising edge at TX2 to force shut down again.

### **TX2 Polarity**

In TX2 mode (default), TX2 is a flash pulse interrupt input. This is designed to force the flash pulse into a lower current state in order to reduce the current pulled from the battery

during high battery current situations. For example, when the LM3561 is engaged in a Flash event and TX2 is pulled high (active high polarity) the current source (LED) is forced into torch mode at the programmed Torch current setting. If TX2 is then pulled low before the flash pulse terminates, the LED current will step back to the previous flash current level. At the end of the flash timeout, whether the TX2 pin is high or low, the LED current will turn-off. In addition to forcing torch mode with a TX2 event, the TX2 input can be set to force shutdown. Configuration Register 2 bit[0] sets this mode (see *Figure 8*). In TX2 shutdown mode, a TX2 event will shutdown the flash pulse. Once shut down, the flash pulse must be re-enabled via STROBE or the flash enable bits in the Enable Register.

### **GPIO2 Mode**

The TX2/GPIO2/INT pin is configured as a general purpose logic input/output by setting GPIO Register bit[3] = '1'. In GPIO2 mode this pin can be either a logic input or output depending on the bit settings for GPIO Register bit [4] (see *Table 4*).

#### Interrupt Output Mode

The TX2/GPIO2/INT pin is configured as an interrupt output by setting the TX2/GPIO2/INT as a GPIO output and setting bit [6] of the GPIO register to '1'. When in INT mode, the TX2/GPIO2/INT pin will pull low when either of the following occur: 1. The LM3561 is in NTC Mode, the LED current source is enabled, and  $V_{NTC}$  falls below  $V_{TRIP}$ .

2. The LM3561's Input Voltage Monitor is enabled and  $V_{\rm IN}$  falls below  $V_{\rm IN\ TH}.$ 

### **INDICATOR LED/THERMISTOR (LEDI/NTC)**

The LEDI/NTC pin serves a dual function, either as an LED indicator driver or as a threshold detector for a negative temperature coefficient (NTC) thermistor circuit.

### Led Indicator Mode (LEDI)

LEDI/NTC is configured as an LED indicator driver by setting Configuration Register 1 bit [4] = '0' (default). The indicator current source is enabled by setting Enable Register bits [1:0] = '01'. In Indicator mode there are 8 different current levels available (2.25mA - 18mA) which are programmed through the Indicator Register (see *Table 3*).

### Led Thermal Comparator (NTC Mode)

Writing a '1' to Configuration Register 1 bit [4] disables the indicator current source and configures LEDI/NTC as a comparator input for monitoring an NTC thermistor circuit. In this mode LEDI/NTC becomes the negative input of an internal comparator, with the positive input internally connected to an internal reference ( $V_{TRIP} = 1V$ ). Additionally, Configuration Register 2 bit [1] determines the action NTC Mode takes if the voltage at LEDI/NTC falls below  $V_{TRIP}$ . With Configuration register 2 bit [1] = '0', the LED current source will be forced into Torch mode when the voltage at LEDI/NTC falls below

 $V_{TRIP}$ . With Configuration Register 2 bit [1] = '1' the device will shut down the current source (LED) when  $V_{LEDI/NTC}$  falls below  $V_{TRIP}$ . When the LM3561 is forced from Flash to Torch, normal LED operation (during the same Flash pulse) can only be re-started by reading from the Flags Register and ensuring the voltage at  $V_{LEDI/NTC}$  is above  $V_{TRIP}$ . When  $V_{LEDI/NTC}$  falls below  $V_{TRIP}$  and the Flags register is cleared, the LM3561 will go through a 250µs deglitch time before the flash current falls to either torch mode or goes into shutdown. This deglitch time prevents noise from inadvertently tripping the NTC comparator. For a more detailed description of this mode and designing the NTC circuit (see *NTC THERMISTOR SELECTION* section in the *Applications Information* section of this datasheet).

In NTC mode the NTC flag (see *Flags Register and Fault Indicators* section) can be output on the TX2/GPIO2/INT pin. This is accomplished by making the TX2/GPIO2/INT an interrupt output (see *Interrupt Output Mode* section).

### ALTERNATE EXTERNAL TORCH (AET MODE)

With Configuration Register 2 bit [2] set to '1' the operation of TX1/TORCH becomes dependent on its occurrence relative to STROBE. In this mode if TX1/TORCH goes high first, followed by STROBE going high, the LEDs are forced into torch mode with no timeout. In this mode if TX1/TORCH goes high *after* STROBE has gone high, then the TX1/TORCH goes high *after* STROBE has gone high, then the TX1/TORCH pin operates as a normal flash interrupt, and the LEDs will turn off at the end of the timeout duration. (See LM3561 Timing Diagrams: *Figure 9* and *Figure 10*). AET mode is can only be used with STROBE for edge sensitive operation (STR bit = 1), will force TX1 to act as a simple flash interrupt.

### INPUT VOLTAGE MONITOR

The LM3561 has an internal comparator that monitors the voltage at IN and can force the LED current into torch mode or into shutdown if  $V_{IN}$  falls below the programmable VIN Monitor Threshold ( $V_{IN\_TH}$ ). Bit [0] in the VIN Monitor register enables or disables this feature. When enabled, Bits [2:1] program the 4 adjustable thresholds of 2.9V, 3V, 3.1V, and 3.2V. Bit [3] in Configuration Register 2 selects whether an under-voltage event forces Torch mode or forces the LED current source off. (See *Table 5* and *Table 11*.)

When the VIN Monitor is active and V<sub>IN</sub> falls below the programmed threshold (V<sub>IN\_TH</sub>) the LEDs will either turn off or their current will be reduced to the programmed Torch current setting. To reset the LED current to its previous level, two things must occur. First, V<sub>IN</sub> must go above V<sub>IN\_TH</sub>, and the Flags register must be read back.

In VIN Monitor mode the VIN Monitor Flag (see *Flags Register and Fault Indicators* section) can be output on the TX2/ GPIO2/INT pin. This is accomplished by making the TX2/ GPIO2/INT an interrupt output (see *Interrupt Output Mode* section).















### Flags Register and Fault Indicators

The Flags Register contains the Interrupt and Fault indicators. Seven flags are available in the Flags Register. These include a Flash Timeout flag (TO), a Thermal Shutdown flag (TSD), an LED Failure flag (LEDF), an LED Thermal flag (NTC), and a VIN Monitor flag. Additionally, two interrupt flag bits TX1 interrupt and TX2 interrupt indicate a change of state of the TX1/TORCH pin (TX1 mode) and TX2/GPIO2/INT pin (TX2 mode). Reading back a '1' indicates the TX lines have changed state since the last read of the Flags Register. A read of the Flags Register resets the flag bits.

### **FLASH TIMEOUT**

The Flash Timeout Flag (TO), (bit [0] of the Flags Register) reads back a '1' if the LM3561 is active in Flash Mode and the timeout period expires before the flash pulse is terminated. The flash pulse can be terminated before the timeout period expires by pulling the STROBE pin low (with STR bit '0'), or by writing a '0' to bits [1:0] of the Enable Register. The TO flag is reset to (0) by pulling HWEN low, removing power to the LM3561, reading the Flags Register, or when the next Flash pulse is triggered.

### **THERMAL SHUTDOWN**

When the LM3561's die temperature reaches  $+150^{\circ}$ C the boost converter shuts down and the NFET and PFET turn off. Additionally, both current sources (LED and LEDI/NTC) turn off. When the thermal shutdown threshold is tripped a '1' gets written to bit [1] of the Flag Register (Thermal Shutdown bit). The LM3561 will start up again when the die temperature falls to below  $+135^{\circ}$ C, the Flags Register is read back, and the device is re-enabled.

### **LED FAULT**

The LED Fault flag (bit 2 of the Flags Register) reads back a '1' if the part is active in Flash or Torch mode and the current source (LED) experiences an open or short condition. An LED open condition is signaled if the OVP threshold is crossed at OUT. An LED short condition is signaled if the voltage at LED goes below 500mV.

There is a delay of 250 $\mu s$  before the LEDF flag is valid on a LED short. This is the time from when V\_{LED} falls below the

LED short threshold of 500mV (typical) to when the fault flag is valid. There is a  $2\mu$ s delay from when the LEDF flag is valid on an LED open. This delay is the time between when the OVP threshold is triggered and when the fault flag is valid. The LEDF flag can only be reset to (0) by pulling HWEN low, removing power to the LM3561, or reading the Flags Register.

### LED THERMAL FAULT

The NTC flag (bit [5] of the Flags Register) reads back a '1' if the LM3561 is active in Flash or Torch mode, the device is in NTC mode, and the voltage at LEDI/NTC has fallen below  $V_{TRIP}$  (1V typical). When this has happened and the LM3561 has been forced into Torch or LED shutdown, depending on the state of Configuration Register 2 bit [1], the voltage at LE-DI/NTC must rise above the  $V_{TRIP}$  threshold and the Flags Register must be read in order to place the device back in normal operation. (see Led Thermal Comparator (NTC Mode) section for more details).

### **INPUT VOLTAGE MONITOR FAULT**

The V<sub>IN</sub> Monitor Flag (bit [7] of the Flags Register) reads back a '1' when the Input Voltage Monitor is enabled and V<sub>IN</sub> falls below the programmed (V<sub>IN\_TH</sub>). The input voltage must rise above V<sub>IN\_TH</sub> and the Flags register must be read back in order to resume normal operation after the LED current has been forced to Torch mode or turned off due to a VIN Monitor event.

### **TX1 AND TX2 INTERRUPT FLAGS**

The TX1 and TX2 interrupt flags (bits [3] and [4] of the Flags register) indicate a TX event on the TX1 or TX2 pins. Bit 3 will read back a '1' if TX1/TORCH is in TX1 mode and the pin has changed from low to high since the last read of the Flags Register. Bit [4] will read back a '1' if TX2 is in TX2 mode and the pin has had a TX event since the last read of the Flags Register. A read of the Flags Register automatically resets these bits.

A TX event can be either a high to low transition or a low to high transition depending on the setting of the TX1 or TX2 polarity bits (see *Table 10*).

## I<sup>2</sup>C-Compatible Interface

### START AND STOP CONDITIONS

The LM3561 is controlled via an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates the START and STOP conditions.



### FIGURE 12. Start and Stop Sequences

The I<sup>2</sup>C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I<sup>2</sup>C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH

period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. *Figure 1* and *Figure 13* show the SDA and SCL signal timing for the I<sup>2</sup>C-compatible Bus. See the Electrical Characteristics Table for timing values.



### **TRANSFERRING DATA**

Every byte on the SDA line must be eight bits long with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the

master. The master releases SDA (HIGH) during the 9th clock pulse (write mode). The LM3561 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

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## **Register Descriptions**

### TABLE 1. LM3561 Internal Registers

Register Name	Internal Hex Address	Power On or Reset Value
Enable Register	0x10	0xF8
Indicator Brightness Register	0x12	0xF8
GPIO Register	0x20	0x80
VIN Monitor Register	0x80	0xF8
Torch Brightness Register	0xA0	0xFA
Flash Brightness Register	0xB0	0xFD
Flash Duration Register	0xC0	0xEF
Flags Register	0xD0	0x00
Configuration Register 1	0xE0	0x6A
Configuration Register 2	0xF0	0xF0

### ENABLE REGISTER (ADDRESS 0x10)

The Enable Register contains the enable bits that turn on the device in Indicate Mode, Torch Mode, or Flash Mode (bits[1:0]). These bits are always reset at the end of a flash pulse. Bit [2] sets the STROBE level or edge control.

### **TABLE 2. Enable Register Bit Settings**

Bits[7:3]	Bit 2	Bits [1:0]
Not Used	(Strobe Level or Edge, STR bit)	Enable Bits
N/A	0 = STROBE Input set for Level. Flash current	Enable Bits
	turns on when STROBE input is high and turns	00 = Shutdown ( <b>default</b> )
	off when STROBE either goes low or the	01 = Indicator Mode
	Timeout Duration expires (default)	10 = Torch Mode
	1 = STROBE Input set for edge triggered. Flash	11 = Flash Mode (bits reset at timeout)
	current turns on when STROBE sees a rising	
	edge. Flash pulse turns off when timeout	
	duration expires	

### **INDICATOR BRIGHTNESS REGISTER (ADDRESS 0x12)**

The Indicator Register contains the bits to set the indicator current level in indicate mode.

### TABLE 3. Indicator Brightness Register Bit Settings

Bits [7:3]	Bits [2:0]
Not Used	Indicate Current Settings
N/A	000 = 2.25mA (default)
	001 = 4.5mA
	010 = 6.75mA
	011 = 9mA
	100 = 11.25mA
	101 = 13.5mA
	110 = 15.75mA
	111 = 18mA

### **GPIO REGISTER (ADDRESS 0x20)**

The GPIO register contains the control bits which change the state of the TX1/TORCH/GPIO1 pin and the TX2/GPIO2 pin to general purpose I/O's (GPIO's).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	TX2/GPIO2/	TX2/GPIO2	TX2/GPIO2	TX2/GPIO2	TX1/GPIO1	TX1/GPIO1	TX1/GPIO1
	INT Interrupt	data	data direction	Control	data	data direction	Control
	Output						
N/A	0 = INT mode	This bit is the	0 = TX2/	0 = TX2/	This bit is the	0 = TX1/	0 = TX1/
	is disabled	read or write	GPIO2 is a	GPIO2 is a	read or write	GPIO1 is a	GPIO1 is
	(default)	data for TX2/	GPIO Input	flash interrupt	data for TX1/	GPIO input	configured as
	1 = When TX2/	GPIO2 in	(default)	input ( <b>default</b> )	GPIO1 in	(default)	flash interrupt
	GPIO2 is	GPIO mode	1 = TX2/	1 = TX2/	GPIO mode	1 = TX1/	input(default)
	configured as	(default is 0)	GPIO2 is a	GPIO2 is	(default is 0)	GPIO1 is a	1 = TX1/
	a GPIO output		GPIO Output	configured as		GPIO output	GPIO1 is
	TX2/GPIO2/			a GPIO			configured as
	INT is set for						a GPIO
	INT mode and						
	will pull low						
	when either						
	the LED						
	Thermal Fault						
	Flag is set or						
	the VIN						
	Monitor Flag is						
	set						

### **TABLE 4. GPIO Register Bit Settings**

### VIN MONITOR REGISTER (ADDRESS 0X80)

The VIN Monitor Register controls the on/off state of the VIN Monitor comparator as well as selects the 4 programmable thresholds.

### **TABLE 5. VIN Monitor Register Bit Settings**

Bits [7:3]	Bits [2:1]	Bit 0
Not Used	VIN Monitor Threshold Settings	VIN Monitor Enable
N/A	00 = 2.9V threshold (V <sub>IN</sub> falling)	0 = VIN Monitor Comparator is
	Default	disabled (default)
	01=3.0V threshold (V <sub>IN</sub> falling)	1 = VIN Monitor Comparator is
	10 = 3.1V threshold (V <sub>IN</sub> falling)	enabled.
	11 = 3.2V threshold (V <sub>IN</sub> falling)	

### **TORCH BRIGHTNESS REGISTER (0XA0)**

The Torch Brightness Register contains the bits to program the LED current in Torch Mode.

### **TABLE 6. Torch Brightness Register Bit Settings**

Bits [7:3]	Bits [2:0]
Not Used	Torch Current Settings
N/A	000 = 18mA
	001 = 36.8mA
	010 = 55.6mA (default)
	011 = 74.4mA
	100 = 93.2mA
	101 = 112mA
	110 = 130.8mA
	111 = 149.6mA
	<u>1</u>

### FLASH BRIGHTNESS REGISTER (ADDRESS 0XB0)

The Flash Brightness Register contains the bits to program the LED current in flash mode.

### TABLE 7. Flash Brightness Register Bit Settings

Bits [7:4]	Bits [3:0]
Not Used	Flash Current Settings
N/A	0000 = 36mA
	0001 = 73.6mA
	0010 = 111.2mA
	0011 = 148.8mA
	0100 = 186.4mA
	0101 = 224mA
	0110 = 261.6mA
	0111 = 299.2mA
	1000 = 336.8mA
	1001 = 374.4mA
	1010 = 412mA
	1011 = 449.6mA
	1100 = 487.2mA
	1101 = 524.8mA Default
	1110 = 562.4mA
	1111 = 600mA

### FLASH DURATION REGISTER (ADDRESS 0XC0)

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Bits [4:0] of the Flash Duration Register set the Flash timeout duration. Bit [5] sets the switch current limit.

Bit [7:6]	Bit 5	Bits [4:0]
Not Used	Current Limit	Flash Timeout Duration Settings
	Select	
N/A	0 = 1A Peak	00000 = 32ms timeout
	Current Limit	00001 = 64ms timeout
	1 = 1.5A Peak	00010 = 96ms timeout
	Current Limit	00011 = 128ms timeout
	(default)	00100 = 160ms timeout
		00101 = 192ms timeout
		00110 = 224ms timeout
		00111 = 256ms timeout
		01000 = 288ms timeout
		01001 = 320ms timeout
		01010 = 352ms timeout
		01011 = 384ms timeout
		01100 = 416ms timeout
		01101 = 448ms timeout
		01110 = 480ms timeout
		01111 = 512ms timeout (default)
		10000 = 544ms timeout
		10001 = 576ms timeout
		10010 = 608ms timeout
		10011 = 640ms timeout
		10100 = 672ms timeout
		10101 = 704ms timeout
		10110 = 736ms timeout
		10111 = 768ms timeout
		11000 = 800ms timeout
		11001 = 832ms timeout
		11010 = 864ms timeout
		11011 = 896ms timeout
		11100 = 928ms timeout
		11101 = 960ms timeout
		11110 = 992ms timeout
		11111 = 1024ms timeout

### TABLE 8. Flash Timeout Duration Register Bit Settings

### FLAGS REGISTER (ADDRESS 0XD0)

The Flags Register holds the status of the flag bits indicating LED Failure, Over-Temperature, the Flash Timeout expiring, VIN Monitor Fault, LED over temperature (NTC), and a TX1 or TX2 interrupt.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VIN Monitor	Not Used	LED Thermal	TX2 Interrupt	TX1 Interrupt	Led Fault	Thermal	Flash Timeout
Flag		Fault			(LEDF)	Shutdown	(TO)
		(NTC)				(TSD)	
0 = No Fault at	N/A	0 =LEDI/NTC	0=TX2 has not	0=TX1/	0 = Proper	0 = Die	0 = Flash
VIN (default)		pin is above	changed state	TORCH has	LED Operation	Temperature	timeout did not
1 = Input		V <sub>TRIP</sub> (default)	(default)	not changed	(default)	below Thermal	expire
Voltage		1=LEDI/NTC	1=TX2 has	state (default)	1 = LED Failed	Shutdown	(default)
Monitor is		has fallen	changed state	1=TX1/	(Open or	Limit ( <b>default</b> )	1 = Flash
enabled and		below V <sub>TRIP</sub>	(TX2 mode	TORCH pin	Short)	1 = Die	timeout
VIN has fallen		(NTC mode	only)	has changed		Temperature	Expired
below (V <sub>IN TH</sub> )		only)		state (TX1		has crossed	
_				mode only)		the Thermal	
						Shutdown	
						Threshold of	
						+150°C	

### **TABLE 9. Flags Register Bit Settings**

### **CONFIGURATION REGISTER 1 (ADDRESS 0XE0)**

Bit 7

Hardware

Configuration Register 1 contains the STROBE enable/disable bit, the STROBE polarity bit, the NTC enable bit, the polarity selection for TX1 and TX2 flash interrupts, and the hardware torch mode enable for TX1/TORCH.

1	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
	TX2 Polarity	TX1 Polarity	NTC Mode	STROBE	STROBE Input	Not Used
			Enable	Polarity	Enable	
	0 = TX2 is set	0 = TX1 is set	0 = LEDI/NTC	0 = STROBE	0 = STROBE	N/A

### **TABLE 10. Configuration Register 1 Bit Settings**

Torch Mode			Enable	Polarity	Enable		
Enable							
0 = TX1/	0 = TX2 is set	0 = TX1 is set	0 = LEDI/NTC	0 = STROBE	0 = STROBE	N/A	N/A
TORCH is a	for active low	for active low	is a Indicator	set for active	Input Disabled		
TX1 flash	polarity	polarity	Current	low polarity	(default)		
interrupt input	1 = TX2 is set	1 = TX1 is set	Source Output	1 = STROBE	1 = STROBE		
(default)	for active high	for active high	(default)	set for active	Input Enabled		
1 = TX1/	polarity	polarity	1 = LEDI/NTC	high polarity			
TORCH pin is	(default)	(default)	is a	(default)			
a hardware			Comparator				
TORCH			Input for LED				
enable. This			Temperature				
bit is reset to 0			Sensing				
after a flash							
event.							

Bit 0

Not Used

### CONFIGURATION REGISTER 2 (ADDRESS 0XF0)

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Configuration Register 2 contains the TX2 shutdown bit, the NTC shutdown bit, the Alternate External Torch Enable bit, and the VIN Monitor Shutdown bit.

Bits [7:4] Not Used	<b>Bit 3</b> V <sub>IN</sub> Monitor Shutdown	<b>Bit 2</b> AET mode	<b>Bit 1</b> NTC Shutdown	<b>Bit 0</b> TX2 Shutdown
N/A	0 = If IN drops	0 = Normal	0 = LEDI/NTC	0 = TX2
	below V <sub>IN TH</sub>	operation for	pin going	interrupt event
	and the VIN	TX1/TORCH	below V <sub>TRIP</sub>	forces the
	Monitor	high before	forces the	flash LED into
	feature is	STROBE (TX1	LEDs into	Torch mode
	enabled, the	mode only)	Torch mode	(TX2 mode
	LEDs are	default	(NTC mode	only) <b>default</b>
	forced into	1 = Alternate	only) <b>default</b>	1 = TX2
	Torch mode	External Torch	1 = LEDI/NTC	interrupt event
	(default)	Mode. TX1/	pin going	forces the
	1 = If IN drops	TORCH high	below V <sub>TRIP</sub>	flash LED into
	below V <sub>IN TH</sub>	before	forces the	shutdown
	and the VIN	STROBE	LEDs into	(TX2 mode
	Monitor	forces Torch	shutdown	only)
	feature is	mode with no	(NTC mode	
	enabled, the	timeout (TX1	only)	
	LEDs turn off	mode only)		

### TABLE 11. Configuration Register 2 Bit Settings

## \_M3561

## **Applications Information**

### **OUTPUT CAPACITOR SELECTION**

The LM3561 is designed to operate with a at least a 10µF ceramic output capacitor. When the boost converter is running the output capacitor supplies the load current during the boost converters on-time. When the NMOS switch turns off the inductor energy is discharged through the internal PMOS switch supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

For proper LED operation the output capacitor must be at least a 10µF ceramic. Larger capacitors such as 22µF can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge ( $\Delta V_Q$ ) and the ripple due to the capacitors ESR ( $\Delta V_{ESR}$ ) use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_{Q} = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}}$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left( \frac{I_{LED} \times V_{OUT}}{V_{IN}} \right) + \Delta I_{L}$$
  
where  
$$\Delta I_{L} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{EW} \times L \times V_{OUT}}$$

In ceramic capacitors the ESR is very low so assume that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. *Table 12* lists different manufacturers for various output capacitors and their case sizes suitable for use with the LM3561.

### **INPUT CAPACITOR SELECTION**

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM3561's boost converter and reduces noise on the devices input terminal that can feed through and disrupt internal analog signals. In the Typical Application Circuit a 10µF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the LM3561's input (IN) terminals. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. *Table 12* lists various input capacitors recommended for use with the LM3561.

### TABLE 12. Recommended Input/Output Capacitors (X5R Dielectric)

Manufacturer	Part Number	Value	Case Size	Voltage Rating
TDK Corporation	C1608JB0J106M	10µF	0603(1.6mm×0.8mm×0.8mm)	6.3V
TDK Corporation	C2012JB1A106M	10µF	0805(2mm×1.25mm×1.25mm)	10V
TDK Corporation	C2012JB0J226M	22µF	0805(2mm×1.25mm×1.25mm)	6.3V
Murata	GRM21BR61A106KE19	10µF	0805(2mm×1.25mm×1.25mm)	10V
Murata	GRM21BR60J226ME39L	22µF	0805(2mm×1.25mm×1.25mm)	6.3V

### **INDUCTOR SELECTION**

The LM3561 is designed to use a 1µH to 2.2µH inductor. *Table 13* lists various inductors that can work well with the LM3561. When the device is boosting  $(V_{OUT} > V_{IN})$  the inductor will typically be the biggest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the LM3561. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance.

mance ensure that the inductor saturation and the peak current limit setting of the LM3561 is greater than  $\rm I_{PEAK}.$  This can be calculated by:

$$I_{\text{PEAK}} = \frac{I_{\text{LOAD}}}{\eta} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} + \Delta I_{\text{L}} \text{ where } \Delta I_{\text{L}} = \frac{V_{\text{IN}} \times (V_{\text{OUT}} - V_{\text{IN}})}{2 \times f_{\text{SW}} \times L \times V_{\text{OUT}}}$$

 $f_{SW}$  = 2MHz, and  $\eta$  can be found in the Typical Performance Characteristics plots.

Manufacturer	L	Part Number	Dimensions (L×W×H)	R <sub>DC</sub>	I <sub>SAT</sub>
Coilcraft	1µH	XPL2010-102ML	2mm×1.9mm×1mm	<b>81</b> mΩ	1.6A
TDK	1µH	VLS252012T-1R0N	2mm×2.5mm×1.2mm	<b>73</b> mΩ	2.7A
TDK	1µH	VLS2010-1R0N	2mm x 2mm x 1mm	90mΩ	1.65A
TDK	1µH	VLS2012ET-1R0N	2mm x 2mm x 1.2mm	<b>71</b> mΩ	1.65A
TDK	1µH	VLS20160ET-1R0N	2mm x 1.6mm x 0.95mm	100mΩ	1.5A
TDK	1µH	VLS252010ET-1R0N	2.5mm x 2mm x 1mm	<b>70m</b> Ω	1.9A

#### **TABLE 13. Recommended Inductors**

### **NTC THERMISTOR SELECTION**

Programming bit [4] of Configuration Register 1 with a (1) selects Thermal Comparator mode, making the LEDI/NTC pin a comparator input for flash LED thermal sensing. The thermal sensing circuit consists of a negative temperature coefficient (NTC) thermistor and a series resistor which forms a resistive divider (see *Figure 15*).





The NTC thermistor senses the LEDs temperature via conducting the LEDs heat into the NTC thermistor. Heat conduction is improved with a galvanic connection at GND (LED cathode and NTC thermistor GND terminal) and by placing the thermistor in very close proximity to the flash LED.

NTC thermistors have a temperature to resistance relationship of:

$$R(T) = R_{25^{\circ}C} \times e^{\left[\beta\left(\frac{1}{T^{\circ}C + 273} - \frac{1}{298}\right)\right]}$$

where  $\beta$  is given in the thermistor datasheet and  $R_{25C}$  is the thermistor's value at +25°C.  $R_{BIAS}$  is chosen so that it is equal to:

$$R_{BIAS} = \frac{R_{T(TRIP)}(V_{BIAS} - V_{TRIP})}{V_{TRIP}}$$

.

where R(T)<sub>TRIP</sub> is the thermistor's value at the temperature trip point, V<sub>BIAS</sub> is the bias voltage for the thermistor circuit, and V<sub>TRIP</sub> = 1V (typical). Choosing R<sub>BIAS</sub> here gives a more linear response around the temperature trip voltage. For example with V<sub>BIAS</sub> = 1.8V and a thermistor whose nominal value at +25°C is 10kΩ and a  $\beta$  = 3380K, the trip point is chosen to be +93°C. The value of R(T) at 93°C is:

$$R(T) = 10 \text{ k}\Omega \text{ x } e^{\left[\beta \left(\frac{1}{93+273} - \frac{1}{298}\right)\right]} = 1.215 \text{ k}\Omega$$

$$R_{\text{BIAS}} \text{ is then: } \frac{1.215 \text{ k}\Omega \text{ x } (1.8\text{V} - 1\text{V})}{1\text{V}} = 972\Omega$$

*Figure 16* shows the linearity of the thermistor resistive divider of the previous example.





FIGURE 16. Thermistor Resistive Divider Response vs Temperature

Another useful equation for the thermistor resistive divider is developed by combining the equations for  $\rm R_{BIAS},$  and R(T) and solving for temperature. This gives the following relationship.

$$T(^{\circ}C) = \frac{\beta \times 298^{\circ}C}{298^{\circ}C \times LN \left[\frac{V_{TRIP} \times RBIAS}{(V_{BIAS} - V_{TRIP}) \times R_{25^{\circ}C}}\right] + \beta} -273^{\circ}C$$

### NTC THERMISTOR PLACEMENT

The termination of the thermistor must be done directly to the cathode of the Flash LED in order to adequately couple the heat from the LED into the thermistor. Consequentially, the noisy environment generated from the switching of the LM3561's boost converter can introduce noise from GND into

Using a spreadsheet such as Excel, different curves for the temperature trip point T(°C) can be created vs R<sub>BIAS</sub>, Beta, or V<sub>BIAS</sub> in order to help better choose the thermal components for practical values of thermistors, series resistors (R3), or reference voltages V<sub>BIAS</sub>.

the thermistor sensing input. To filter out this noise it is necessary to place a  $0.1\mu F$  or larger ceramic capacitor close to the LEDI/NTC pin. The filter capacitor's return must also connect with a low-impedance trace, as close as possible to the GND pin of the LM3561.

## Layout Recommendations

The high frequency and relatively large switching currents of the LM3561 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

- 1. Place  $C_{IN}$  on the top layer (same layer as the LM3561) and as close to the device as possible. The input capacitor conducts the driver currents during the lowside MOSFET turn-on and turn-off and can see current spikes over 500mA in amplitude. Connecting the input capacitor through short wide traces on both the IN and GND terminals will reduce the inductive voltage spikes that occur during switching and which can corrupt the  $V_{IN}$  line.
- 2. Place  $C_{OUT}$  on the top layer (same layer as the LM3561) and as close as possible to the OUT and GND terminal. The returns for both  $C_{IN}$  and  $C_{OUT}$  should come together at one point, and as close to the GND pin as possible. Connecting  $C_{OUT}$  through short wide traces will reduce the series inductance on the OUT and GND terminals that can corrupt the V<sub>OUT</sub> and GND line and cause excessive noise in the device and surrounding circuitry.
- 3. Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the fast dV/dt present at SW that can couple into nearby traces.

- 4. Avoid routing logic traces near the SW node so as to avoid any capacitively coupled voltages from SW onto any high impedance logic lines such as TX1/TORCH/ GPIO1, TX2/GPIO2/INT, HWEN, LEDI/NTC (NTC mode), SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
- 5. Terminate the Flash LED cathode directly to the GND pin of the LM3561. If possible, route the LED return with a dedicated path so as to keep the high amplitude LED current out of the GND plane. For a Flash LED that is routed relatively far away from the LM3561, a good approach is to sandwich the forward and return current paths over the top of each other on two adjacent layers. This will help in reducing the inductance of the LED current paths.
- 6. The NTC Thermistor is intended to have its return path connected to the LED's cathode. This allows the thermistor resistive divider voltage ( $V_{NTC}$ ) to trip the comparators threshold as  $V_{NTC}$  is falling. Additionally, the thermistor to LED cathode junction can have low thermal resistivity since both the LED and the thermistor are electrically connected at GND. The draw back is that the thermistor's return will see the switching currents from the LM3561's boost converter. Because of this, it is necessary to have a filter capacitor at the NTC pin which terminates close to the GND of the LM3561 and which can conduct the switched currents to GND.



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