National Semiconductor

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LM3464

LED Driver with Dynamic Headroom Control and Thermal Control Interfaces

General Description

The LM3464 is a 4-channel high voltage current regulator that provides a simple solution for LED lighting applications. The LM3464 provides four individual current regulator channels and works in conjunction with external N-channel MOSFETs and sense resistors to give accurate driving current for every LED string. Additionally, the Dynamic Headroom Control (DHC) output can be interfaced to the external power supply to adjust the LED supply voltage to the lowest level that is adequate to maintain all the string currents in regulation, yielding the optimal overall efficiency.

Digital PWM or analog voltage signals can be used to control the duty cycle of the all the channels. When analog control is used, the dimming frequency can be programmed via an external capacitor. A minimum duty cycle control is provided in the conditions that the analog dimming is configured as thermal feedback.

Protection features include VIN under-voltage lock-out, LED open/short circuit and over-temperature fault signaling to the system controller.

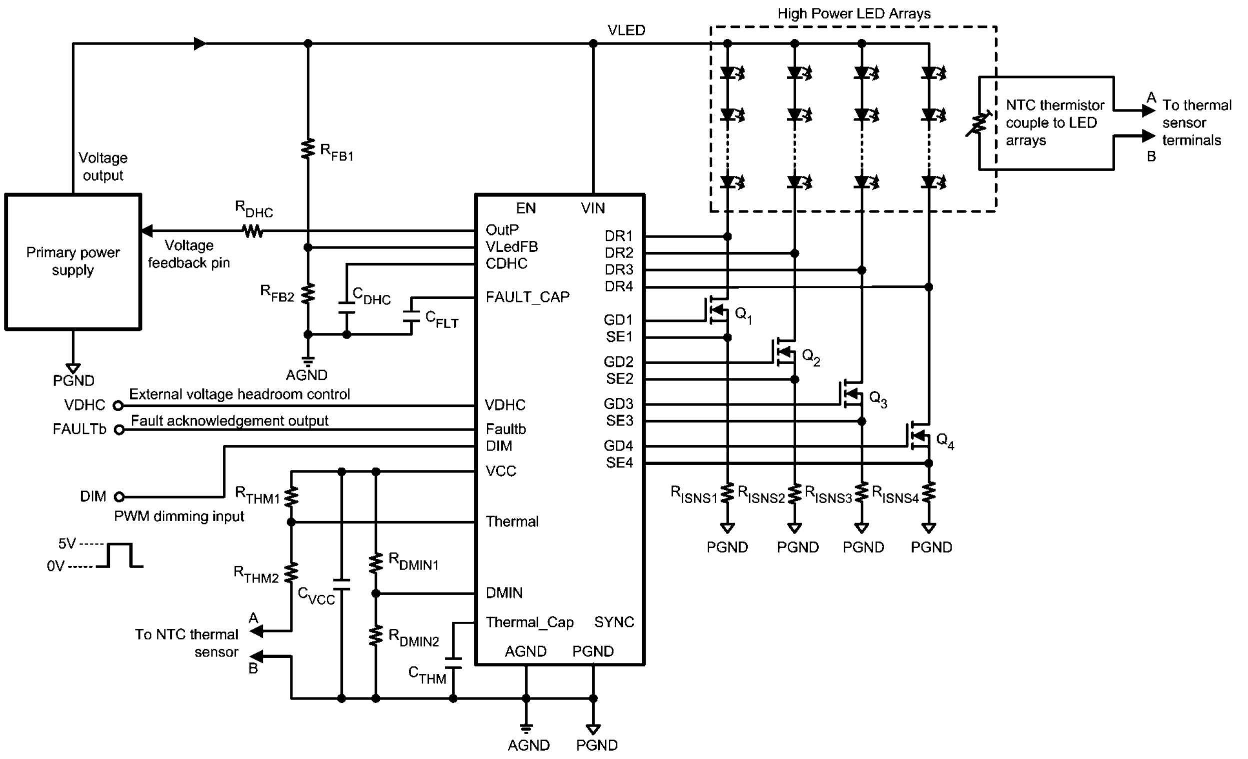
Features

- Wide input voltage range (12V-80V)
- Dynamic Headroom Control ensures maximum efficiency
- 4 output channels with individual current regulation
- High channel to channel accuracy
- Digital PWM/Analog dimming control interface
- Resistor programmable dimming frequency & minimum duty cycle (analog dimming mode)
- Direct interface to thermal sensor
- Fault detection
- Over temperature protection
- Thermal shutdown
- Under voltage lockout
- Thermal enhanced eTSSOP-28 package

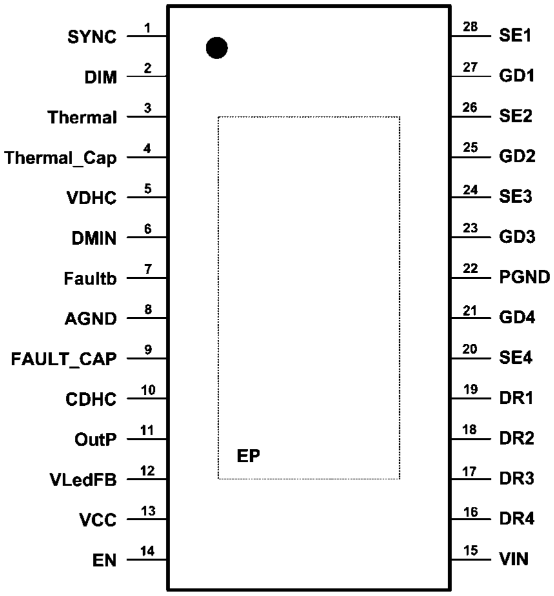
Applications

- Streetlights
- Solid State Lighting Solutions

Typical Application



Connection Diagram



Top View
28 Lead Plastic eTSSOP-28
NS Package Number MXA28A

30115002

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM3464MH	Exposed Pad TSSOP-28	MXA28A	73 Units per Anti-Static Tube
LM3464MHX			2500 Units on Tape and Reel

Pin Descriptions

Pin	Name	Description	Application Information
1	SYNC	Synchronization signal output for cascade operation (Master-Slave configuration)	Connect this pin to the DIM pin of other LM3464 to enable cascade operation (multiple device). This pin should leave open for single device operation.
2	DIM	PWM dimming control	Apply logic level PWM signal to this pin controls the average brightness of the LED string. (<1.25V disable output).
3	Thermal	Thermal sensor input	Connect thermal sensor to this pin with bias accordingly to facilitate thermal foldback and control the brightness of the LED array.
4	Thermal_Cap	Thermal dimming ramp capacitor	Connect a capacitor across this pin and GND to define the thermal dimming frequency.
5	VDHC	Head room control	Apply external voltage across this pin and ground to define the minimum drain voltage. This pin is internal biased at 0.9V.
6	DMIN	Minimum thermal dimming duty control	The voltage across this pin and GND defines the minimum thermal dimming duty cycle.
7	Faultb	Fault signal output	Open Drain output, pull-down when FAULT condition occurred.
8	AGND	Signal ground	Analog ground connection for internal circuitry. Must be connected to PGND external to the package.
9	FAULT_CAP	Fault delay capacitor	Connect to an external capacitor to program the fault response time.
10	CDHC	DHC time constant capacitor	An external capacitor to ground programs the Dynamic Headroom Control loop response time
11	OutP	DHC Output	Connect this pin to the voltage feedback input of primary power supply to facilitate dynamic headroom control.
12	VLedFB	Output voltage sense input	This pin senses the output voltage of the primary power supply.
13	VCC	Internal regulator output	This pin is the output terminal of the internal voltage regulator and should be bypassed by a high quality 1uF ceramic capacitor.
14	EN	Enable input	This pin serves as device enable input when logic level signal is applied. (Active high with internal pull-up)
15	VIN	Supply voltage	The input voltage should be in the range of 12V to 80V.
16	DR4	Channel 4 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 4 to facilitate DHC operation and fault detection.
17	DR3	Channel 3 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 3 to facilitate DHC operation and fault detection.
18	DR2	Channel 2 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 2 to facilitate DHC operation and fault detection.
19	DR1	Channel 1 drain sense input	This pin senses the drain voltage of the external MOSFET of channel 1 to facilitate DHC operation and fault detection.

Pin	Name	Description	Application Information
20	SE4	Channel 4 sense input	Connect to an external sense resistor to define the Channel 4 LED current.
21	GD4	Channel 4 gate driver output	Connect to the gate of external NMOS to control the channel 4 LED current.
22	PGND	Power Ground	Ground for power circuitry. Reference point for all stated voltages. Must be externally connected to EP and AGND
23	GD3	Channel 3 gate driver output	Connect to the gate of external NMOS to control the channel 3 LED current.
24	SE3	Channel 3 sense input	Connect to an external sense resistor to define the Channel 3 LED current.
25	GD2	Channel 2 gate driver output	Connect to the gate of external NMOS to control the channel 2 LED current.
26	SE2	Channel 2 sense input	Connect to an external sense resistor to define the Channel 2 LED current.
27	GD1	Channel 1 gate driver output	Connect to the gate of external NMOS to control the channel 1 LED current.
28	SE1	Channel 1 sense input	Connect to an external sense resistor to define the Channel 1 LED current.
EP	EP	Thermal Pad (Power Ground)	Used to dissipate heat from the package during operation. Must be electrically connected to PGND external to the package.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} to GND	-0.3V to 100V
DR1, DR2, DR3, DR4 to GND	-0.3V to 100V
EN to GND	-0.3V to 5.5V
All other inputs to GND	-0.3V to 7V
ESD Rating (*Note 2*)	
Human Body Model	±2 kV
Storage Temperature Range	−65°C to + 150°C
Junction Temperature (T_J)	+ 150°C

Operating Ratings

Supply Voltage Range (VIN)	12V to 80V
Junction Temperature Range (T_J)	−40°C to + 125°C
Thermal Resistance (θ_{JC}) (*Note 3*)	29°C/W

Electrical Characteristics

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 48V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcc Regulator						
$V_{IN-UVLO}$	Vin under voltage lockout	V_{IN} increasing		8.5		V
$V_{IN-UVLO-HYS}$	Vin UVLO hysteresis	V_{IN} decreasing		95		mV
V_{CC}	VCC output voltage	$C_{VCC} = 0.68\ \mu F$ No load	**6.15**	6.3	**6.51**	V
$V_{CC-UVLO}$	VCC under-voltage lockout threshold (UVLO)	V_{CC} increasing	**4.98**		**5.28**	V
$V_{CC-UVLO-HYS}$	VCC UVLO hysteresis	V_{CC} decreasing		250		mV
I_{IN}	Quiescent Current from VIN	$C_{VCC} = 0.68\ \mu F$ No load	**1.65**	**2.3**	**3**	mA
I_{VCC}	VCC Current limit	$V_{CC} = 0V$	**18**			mA
Device Enable						
$V_{EN-DISABLE}$	Device disable voltage threshold	V_{EN} Decreasing	**2.1**	**2.55**	**3**	V
I_{EN-MAX}	EN pin internal pull current	$V_{EN} = 0V$	**7.2**	**11**	**14.7**	uA
Analog Dimming Control Interface						
$V_{CTHM-MAX}$	Sawtooth max. voltage threshold at Thermal_Cap pin 100% output duty cycle		**2.95**	**3.25**	**3.3**	V
$V_{CTHM-MIN}$	Sawtooth min. voltage threshold at Thermal_Cap pin 0% output duty cycle		**0.325**	**0.4**	**0.493**	V
I_{CTHM}	Thermal_Cap pin output current		**38.9**	**50**	**61**	uA
PWM Dimming Control Interface						
$V_{DIM-LED-ON}$	DIM pin voltage threshold at LED ON	$V_{DMIN} = 0V$ $V_{THERMAL} = V_{CC}$	**1.19**			V
$V_{DIM-LED-OFF}$	DIM pin voltage threshold at LED OFF	$V_{DMIN} = 0V$ $V_{THERMAL} = V_{CC}$			**1.3**	V
Dynamic Headroom Control Output						
$V_{OutP-MAX}$	OutP pin max. output voltage			V_{CC}-0.5		V
$V_{OutP-MIN}$	OutP pin min. output voltage	IoutP = 1 mA current sink		0.3		V
$V_{LEDFB-LED-ON}$	VLedFB pin voltage threshold at LED ON		**2.4**	**2.5**	**2.58**	V
$V_{LEDFB-SYS-RST}$	VLedFB pin voltage threshold at system reset			**1.2**		V
LED Current Regulator						
$V_{GDx-MAX}$	GDx gate driver max. output voltage		4.73	V_{CC}−1		V
$V_{GDx-MIN}$	GDx gate driver min. output voltage			0.115	0.127	V
$I_{GDx-MAX}$	GDx gate driver short circuit current	GDx short to GND			8	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Fault Detection						
$V_{SHORTFAULT}$	DRx short fault threshold	Any $V_{DRx} < 2.5V$	**8.35**	**8.4**	**9.75**	V
$V_{OPENFAULT}$	SEx open fault threshold	Measure at SEx pin	30			mV
$I_{FAULT-CAP}$	FAULT_CAP pin output current			25		uA
$V_{FAULT-CAP}$	FAULT-CAP pin voltage threshold at fault timer expire	$V_{FAULT-CAP}$ rising		3.6		V
R_{Faultb}	Faultb pin to GND resistance	LED fault = TRUE		110		Ω
Thermal Protection						
T_{OTM-TH}	Over Temperature Monitor Threshold			125		°C
$T_{OTM-HYS}$	Over Temperature Monitor Hysteresis			20		°C
T_{SD}	Thermal shutdown temperature	T_J rising		165		°C
T_{SD-HYS}	Thermal shutdown temperature hysteresis	T_J falling		20		°C

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

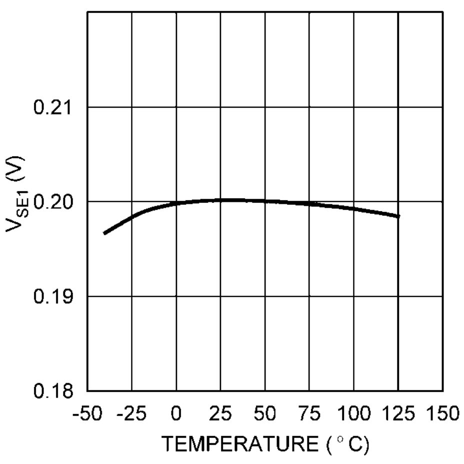
Note 3: θ_{JC} measurements are performed in general accordance with Mil-Std 883B, Method 1012.1 and utilizes the copper heat sink technique. Copper Heat Sink @ 60°C.

Note 4: V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Typical Performance Characteristics

All curves taken at VIN = 48V with configuration in typical application for driving twelve power LEDs with four output channels active and output current per channel = 350 mA. T_A = 25°C, unless otherwise specified.

Channel 1 Current Sense Voltage (V_{SE1})



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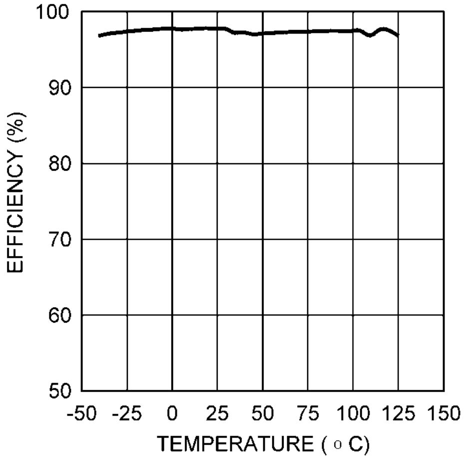
Effifciency (%)



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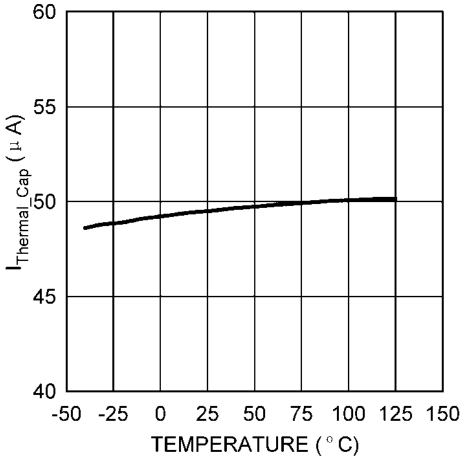
Thermal_Cap Pin Output Current



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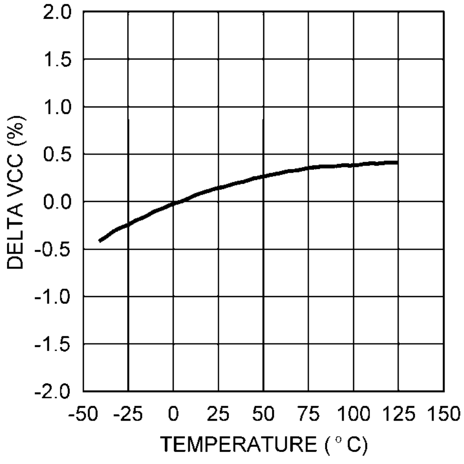
VCC Variation (%)



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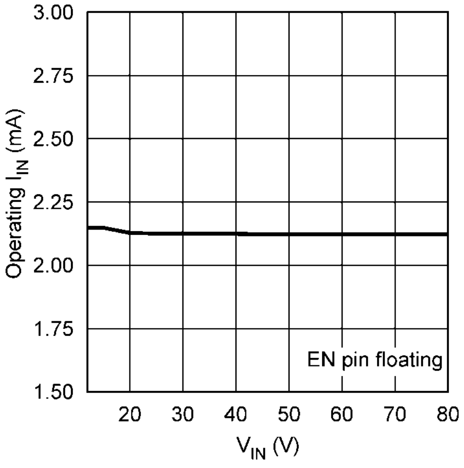
Operating Current (EN pin floating)



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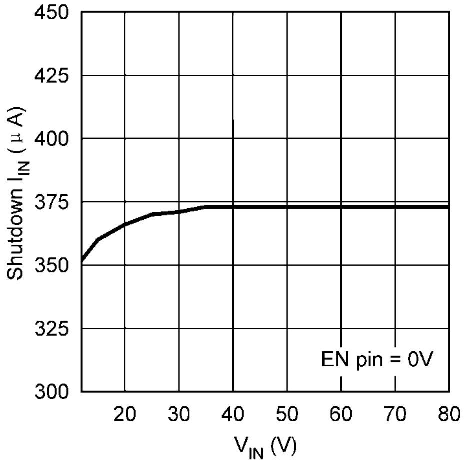
Shutdown Current (EN pin = 0V)



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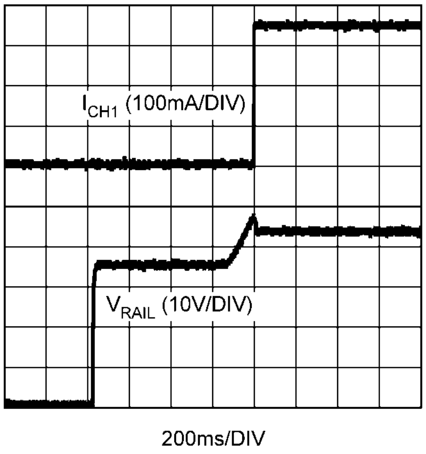
Startup Waveforms



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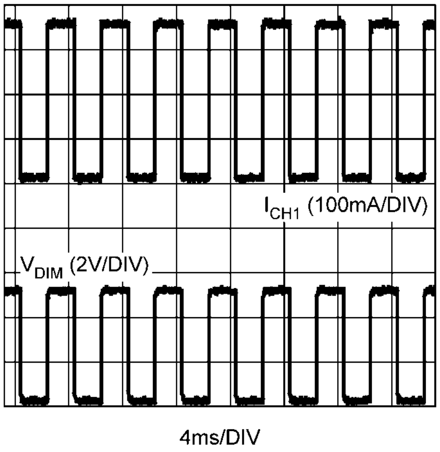
PWM Dimming (DIM pin)



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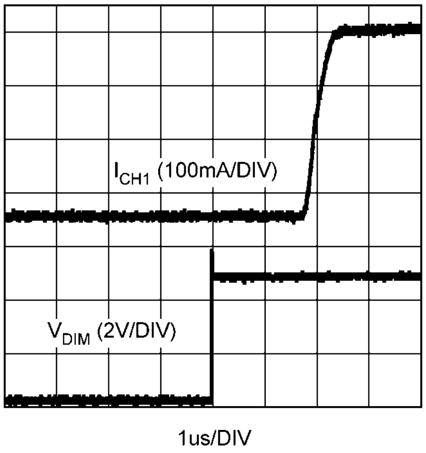
PWM Dimming Delay Time (V_{DIM}) rising



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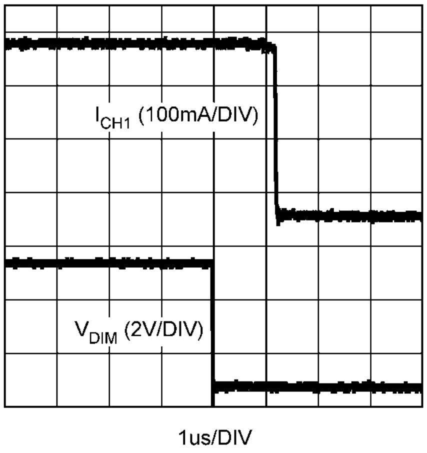
PWM Dimming Delay Time (V_{DIM}) falling



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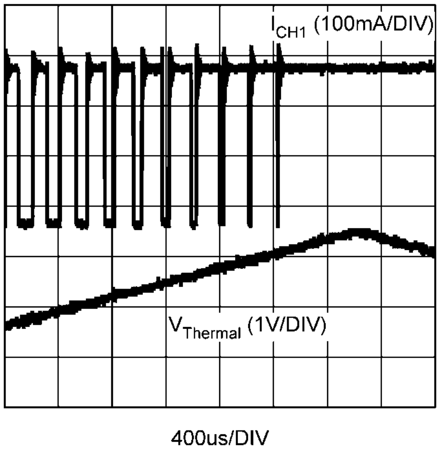
Thermal Foldback Dimming ($V_{THERMAL}$) rising



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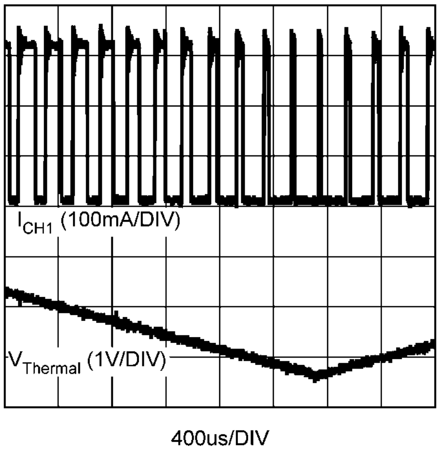
Thermal Foldback Dimming ($V_{THERMAL}$) falling



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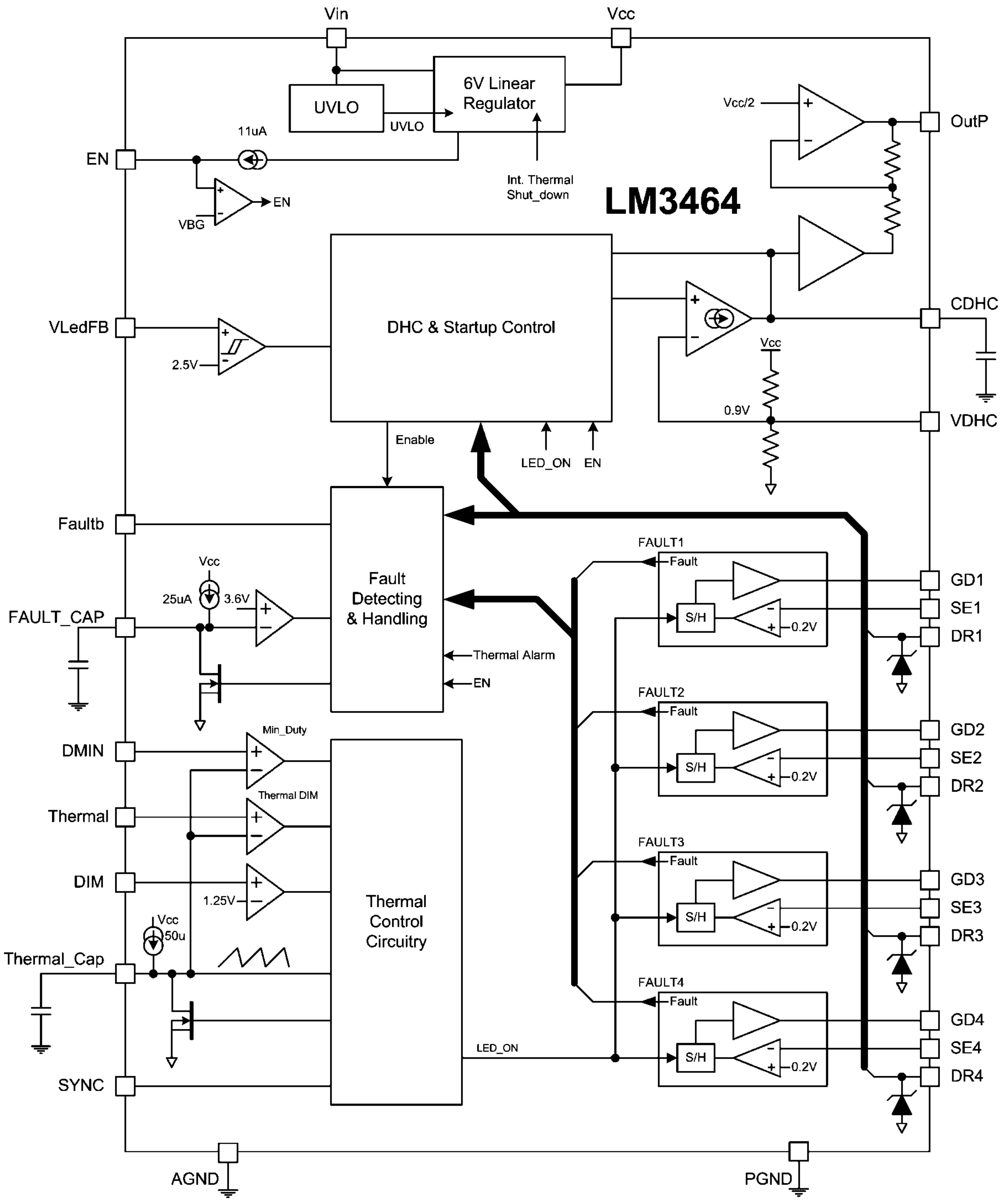
Block Diagram



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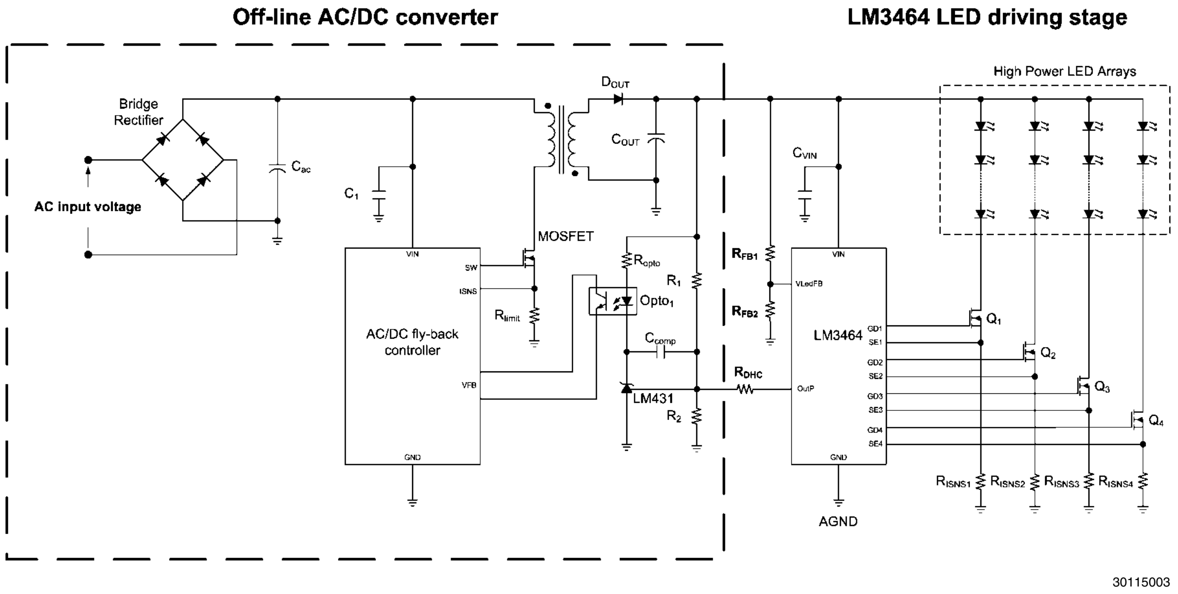


FIGURE 1. Typical Application Circuit with Fly-Back AC/DC Converter

Overview

The LM3464 is a linear current regulator with four output channels designed for LED lighting systems with wide input voltage range, high speed PWM and thermal foldback dimming control interface. The incorporation of the Dynamic Headroom Control (DHC) technology controls the output voltage of the primary power source and keeps the overall efficiency of the system always maximum. Linear current regulation secures high accuracy output current, LED and system reliability. High speed PWM dimming provides the flexibility of brightness control while maintaining color temperature of the light. The thermal foldback feature enables the LM3464 to manage the temperature of the LED heat sink or system chassis with a simple NTC/PTC temperature sensor. The thermal foldback input can also be used as an analog dimming control input to adapt to other sensors easily, such as ambient light sensor.

Dynamic Headroom Control (DHC)

Operation Principles of DHC

Dynamic Headroom Control is a technology that aims at maximizing the overall system efficiency by altering the supply voltage to the LED(s) dynamically in respect to the characteristics of the LED(s). In the LM3464, DHC is facilitated by connecting a resistor in between the OutP pin of the LM3464 and the voltage feedback node of the primary power supply (AC/DC) as shown in Figure 2.

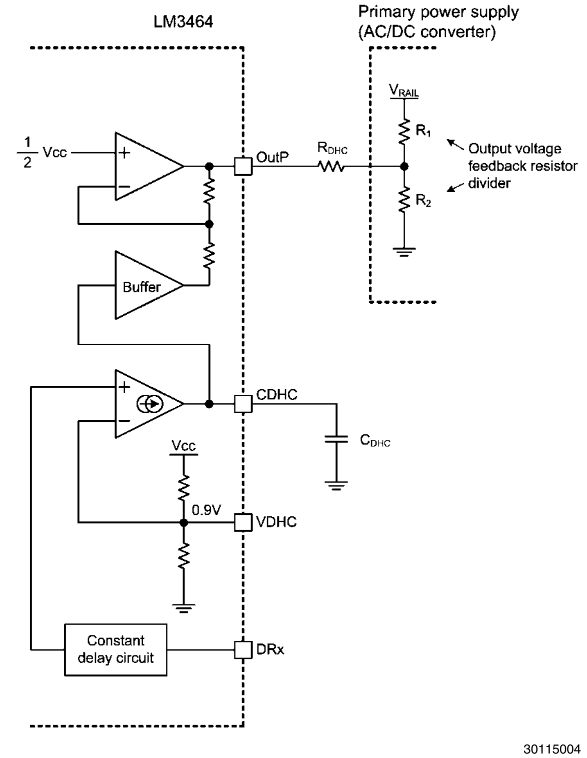


FIGURE 2. Circuitry of the DHC Mechanism

For example, in steady state, when all the output channels are in regulation and the forward voltage of any LED string decreases due to temperature raise, the drain voltage of the corresponding channel (DRx) increases to exceed the default 0.9V typical headroom voltage in order to maintain constant output current. As the drain voltage increases, the voltage of CDHC increases and the current sink into the OutP pin decreases. This will finally result in decrease of rail voltage (V_{RAIL}) until the corresponding DRx voltage returns to minimum level.

System Operation

In order to provide failure protection to the LEDs, the rail voltage is pulled up by the LM3464 from a relatively low voltage level until reaching certain preset level. Figure 3 shows the change of the rail voltage of the LM3464 LED lighting system upon the primary power source is powered.

Figure 1 shows the typical application circuit of powering the LM3464 LED driver circuitry with an off-the-shelf fly-back AC/DC converter. In this application, output voltage feedback of the AC/DC converter is mainly governed by a voltage reference IC, LM431 and a voltage divider consists of R_1 and R_2. The LM3464 influences the output voltage of the AC/DC converter by sinking current from the junction of the voltage divider (R_1 and R_2) to realize dynamic headroom control.

The operation of the LM3464 upon startup can be divided into several phases according to the change of the rail voltage as shown in Figure 3. When the AC/DC converter is powered up, the rail voltage increases and stays steady when its native nominal output voltage, $V_{RAIL(nom)}$ is reached. This voltage is defined by the output voltage feedback resistor divider of the AC/DC converter. At this voltage level, the LM3464 is powered already. After certain delay defined by C_{DHC}, the LM3464 starts to push up the rail voltage by sinking current into the OutP pin from the voltage feedback node of the AC/DC converter until V_{DHC_READY} is reached. This is the possible highest rail voltage in normal operation and the voltage level that the LED strings turns on and DHC begins. As the LEDs turn on, the output capacitor of the primary power supply discharges and the rail voltage decreases to certain level that system efficiency is maximized (V_{LED}).

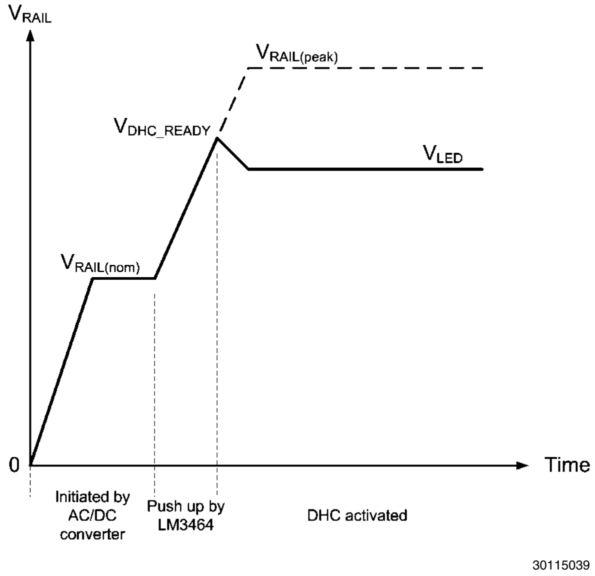


FIGURE 3. Changes of Rail Voltage Upon Power Up

Application Information

SETTING ($V_{RAIL(nom)}$)

The nominal rail voltage $V_{RAIL(nom)}$ is the nominal output voltage of the primary power supply (AC/DC) prior to DHC begins. The selection of $V_{RAIL(nom)}$ is primarily dependent on the forward voltages of the LED arrays and should follow the equation shows below:

$$V_{RAIL(nom)} \leq V_{f(all\_temp)} + V_{VDHC}$$

In the equation, $V_{f(all\_temp)}$ is the lowest forward voltage among all the LED arrays under all possible temperature. And V_{VDHC} is the voltage headroom that defines by the voltage at the VDHC pin. Normally, the forward voltage of an LED drops as the ambient temperature increases. This could create large variation of total forward voltage of a LED sting under different temperature. In order to ensure proper system startup, the variation of LED forward voltage against temperature and forward current must be considered in calculations.

SETTING V_{DHC_READY} AND $V_{RAIL(peak)}$

DHC begins when the voltage at VLedFB pin reaches 2.5V, which is defined by the values of R_{FB1} and R_{FB2}:

$$2.5V = V_{DHC\_READY} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

Where

$$V_{DHC\_READY} < V_{RAIL(peak)}$$

At this stage, the current of the LED strings are regulated and the rail voltage decreases to reduce the voltage drop and power dissipation on the MOSFETs.

In case the OutP pin is accidentally shorten to ground, the rail voltage will increase and end up exceeding V_{DHC_READY}. The possible peak output voltage, $V_{RAIL(peak)}$ of the AC/DC converter can be roughly defined by the forward voltage of the LED strings and must set below the rated voltage of the components at the output of the AC/DC converter. It is suggested to limit $V_{RAIL(peak)}$ to no more than 10VDC higher than the forward voltage of the LED string. The following equations define the maximum output voltage of the AC/DC converter that can be pushed up by the LM3464:

$$V_{RAIL(peak)} = V_{R1} + V_{REF(AC/DC)} = (R_1 \times I_{R1}) + V_{REF(AC/DC)}$$

for $V_{REF(AC/DC)} = 2.5V$

$$I_{R1} = \frac{V_{RAIL(peak)} - 2.5V}{R_1}$$

also since

$$I_{R1} = \frac{V_{REF(AC/DC)}}{R_{D2}} + \frac{V_{REF(AC/DC)} - V_{D1} - V_{outP(min)}}{R_{DHC}}$$

$$= \frac{2.5V}{R_{D2}} + \frac{2.5V - 0.5V - 0.3V}{R_{DHC}}$$

$$R_{DHC} = \frac{1.7V}{\left(I_{R1} - \frac{2.5V}{R_2}\right)}$$

As the system enters steady state, the rail voltage V_{RAIL} decreases and finally settles to an optimal level that maintains the maximum power efficiency of the entire system. The voltage level of V_{RAIL} under steady state can be calculated following this equation:

$$V_{RAIL} = V_{f(highest)} + V_{VDHC}$$

In the equation, V_{RAIL} is the rail voltage in steady state and $V_{f(highest)}$ is the total forward voltage of the LED string which carry the highest forward voltage among the four LED stings.

V_{VDHC} is the voltage at the VDHC pin. This voltage decides the headroom voltage for the LM3464 driver stage and equals to the minimum V_{DRx} among the drain voltage of the MOSFETs under steady state. The VDHC pin is internally biased to 0.9V which also set the default voltage headroom to 0.9V. In applications that the output of the AC/DC converter contains more than 0.9V peak-to-peak ripple voltage, the voltage headroom can be increased by applying external bias to the VDHC pin.

DEFINING VOLTAGE HEADROOM

The voltage headroom is the rail voltage margin that reserve for precision linear current regulation under steady state. Under steady state, the voltage headroom is always minimized by the LM3464 to reduce power losses on the MOSFETs till one of the drain voltage (V_{DRx}) of the MOSFETs equals the voltage on VDHC pin (0.9V typical).

With external bias, the voltage of the VDHC pin can be adjusted up or down to adapt to different types of primary power supply. Figure 4 shows a simple resistor based biasing circuit that derives biasing voltage from the output of the internal voltage regulator, the VCC pin.

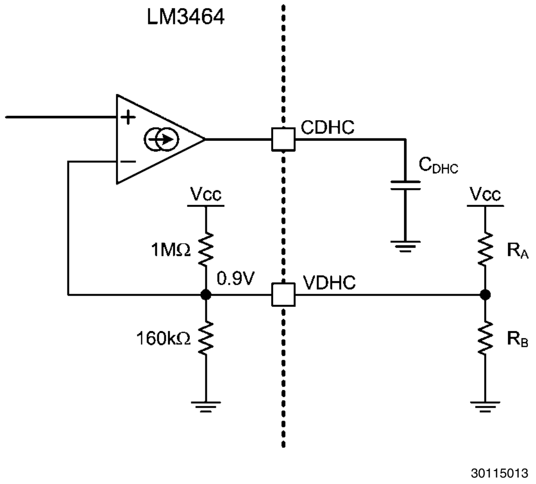


FIGURE 4. Adjusting Voltage Headroom with Resistors

With the additional resistors, the VDHC pin voltage is adjustable in between 0.8V and 2V. The values of R_A and R_B should be at least 10 times lower than the values of the internal resistor divider of the VDHC pin. However, it is recommended not to set the voltage headroom too low because the ripple voltage of the primary power supply output may and cause visible flicker due to insufficient voltage headroom. Thus the voltage headroom follows this equation:

$$V_{DHC} = \frac{160\ k\Omega\ //\ R_B}{160\ k\Omega\ //\ R_B + 1\ M\Omega\ //R_A} \times V_{CC}$$

where $0.8V < V_{VDHC} < 2V$

SETTING LED CURRENT

The LED current regulating mechanism of the LM3464 driver stage contains four individual LED current regulators. Every LED current regulator is composed of an external MOSFET (Q_1-Q_4), a current sensing resistor (R_{ISNS1}-R_{ISNS4}) and an amplifier inside the LM3464 that monitors the feedback voltage from the current sensing resistor. The integrated amplifier compares the voltage across current sensing resistors (R_{ISNS1}-R_{ISNS4}) to a 200mV typical reference voltage and controls the gate voltage of the MOSFETs (Q_1-Q_4) to realize linear current regulations. Figure 5 shows the simplified circuit of the linear LED current regulators.

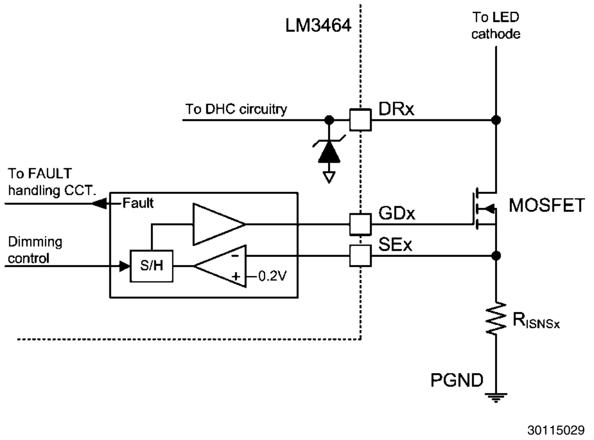


FIGURE 5. Linear LED Current Regulator

The driving currents of the LED strings are defined by the values of R_{ISNS1} to R_{ISNS4} individually. The LED current and the value of R_{ISNSx} is related by the following equation:

$$I_{LED} = \frac{200}{R_{ISNSx}}\ mA$$

Since R_{ISNS1} to R_{ISNS4} define and carry LED currents, these resistors should be resistors with no more than 1% tolerance and adequate rated power to the desired LED current.

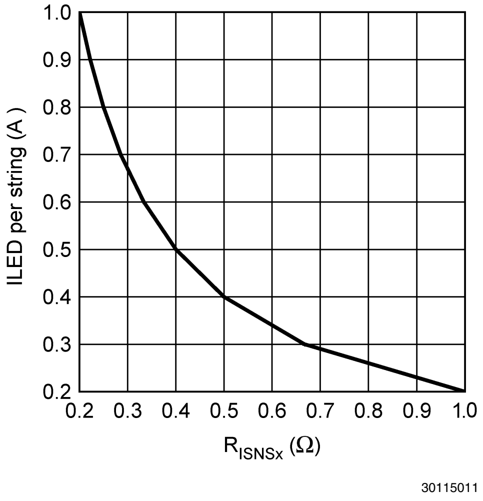


FIGURE 6. LED Current vs R_{ISNSx}

RESPONSE OF THE LM3464 DRIVER STAGE

In order to ensure good operation stability of the entire system, the response of the LM3464 circuitry must be set slower than the primary power supply. The response of the LM3464 is decided by the value of the capacitor C_{DHC}. In general, a higher capacitance C_{DHC} will result in slower response of the LM3464 driver stage.

Generally, a first order integrator that consists of C_{DHC} and a transconductance amplifier with g_m = 76umho and +/– 15uA current limit as shown in Figure 7 defines the frequency response of the LM3464 driver stage.

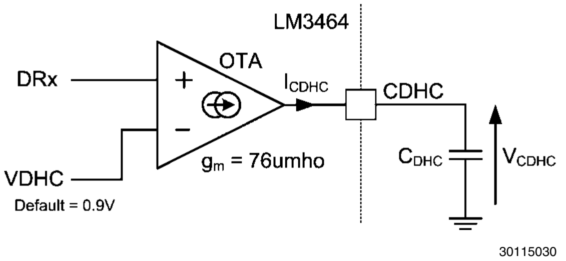


FIGURE 7. Simplified Circuit of the Frequency Response Setting Mechanism

The transconductance amplifier serves as a voltage to current converter that charges C_{DHC} with current proportional to the voltage difference between V_{DRx} and V_{VDHC}.

As the voltage of the OutP pin is equal to $V_{CC} - V_{CDHC}$, the speed of voltage change of the OutP pin is limited by C_{DHC}. The higher capacitance the C_{DHC} has, the longer time the OutP pins takes for certain voltage change. Thus the value of C_{DHC} decides the response of the LM3464 driver stage.

If the response of the LM3464 driver stage is set faster than that of the primary power supply, the entire system will suffer from unstable operation. However, setting the response of the LM3464 driver stage unnecessarily slow will worsen transient performance of the system and false trigger the fault detection mechanism of the LM3464. Practically, the minimum value of the C_{DHC} can be found out by means of 'try and error'. In most cases, a 1uF 16V ceramic capacitor is a good starting point that sets the response of the LM3464 driver stage slow enough for initial trial.

The value of the C_{DHC} capacitor can be reduced to speed up the response of the LM3464 driver stage. Otherwise, in case the system is unstable with 1uF C_{DHC}, the capacitance of the C_{DHC} capacitor should be increased until the entire system get into stable operation.

This approach is effectively setting the cut-off frequency of the LM3464 driver stage lower than that of the primary power supply. Usually, setting the cut-off frequencies of the two stages apart can help avoiding unstable operation. The cut-off frequency of the LM3464 driver stage is governed by the follow equation:

$$f_{LM3464(-3\ dB)} = \frac{1}{2\pi(1.2 \times 10^6) \times C_{DHC}}$$

THERMAL FOLDBACK INTERFACE

The thermal foldback function of the LM3464 helps in reducing the average LED currents and prolonging the LED lifetime under high temperature. The Thermal pin of the LM3464 is an analog input for thermal foldback control that accepts DC voltage from 0V to V_{CC}. The thermal foldback control circuitry reduces the average LED currents by means of PWM dimming as shown in Figure 8:

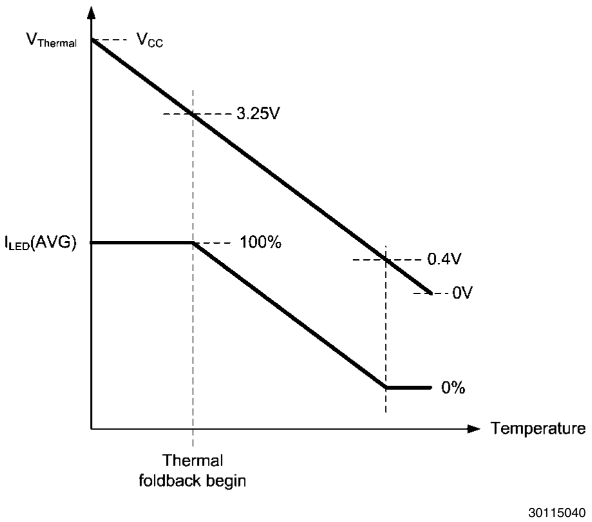


FIGURE 8. Average LED Current Reduces According to $V_{Thermal}$

The dimming frequency is defined by a sawtooth waveform that generated by charging and discharging the capacitor C_{THM} connected across the Thermal_Cap pin and GND. The LM3464 charges the C_{THM} up to 3.25V with 50uA constant current and discharge the C_{THM} by pulling the Thermal_Cap pin to ground until the pin voltage equals 0.4V. By comparing the voltage at the Thermal pin to the sawtooth wave, a PWM dimming signal for thermal foldback is obtained as shown in Figure 9:

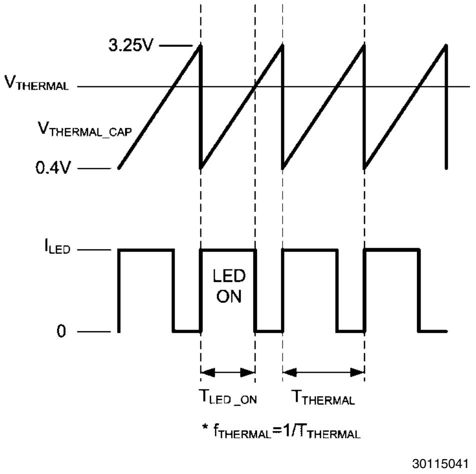


FIGURE 9. Signals Facilitating Thermal Foldback Control

If the voltage at the Thermal pin is driven to exceed 3.25V, all output channels will be enabled with 100% thermal dimming duty cycle. If the Thermal pin voltage is set below 0.4V, all output channels will be disabled with 0% thermal dimming duty cycle. The dimming frequency and duty cycle with thermal foldback control are governed by the following equations:

$$f_{Thermal\text{-}foldback} = \frac{50\ \mu A}{(3.25 - 0.4) \times C_{THM}}$$

$$D_{Thermal\text{-}foldback} = (T_{LED\_ON} \times f_{Thermal\text{-}foldback}) \times 100\%$$

$$= [(V_{THERMAL} - 0.4) \text{ X } 35]\%$$

$$\text{for } 0.4 \leq V_{THERMAL} \leq 3.25V$$

SETTING MINIMUM THERMAL DIMMING DUTY CYCLE

In applications that need to guarantee minimum illumines under high temperature environments, the minimum dimming duty cycle for thermal foldback may need to be limited. Such limit is defined by the voltage at the DMIN pin. When the Thermal pin voltage falls below the voltage at the DMIN pin, the thermal foldback dimming duty cycle will maintain at the level that defined by DMIN, as shown in Figure 10.

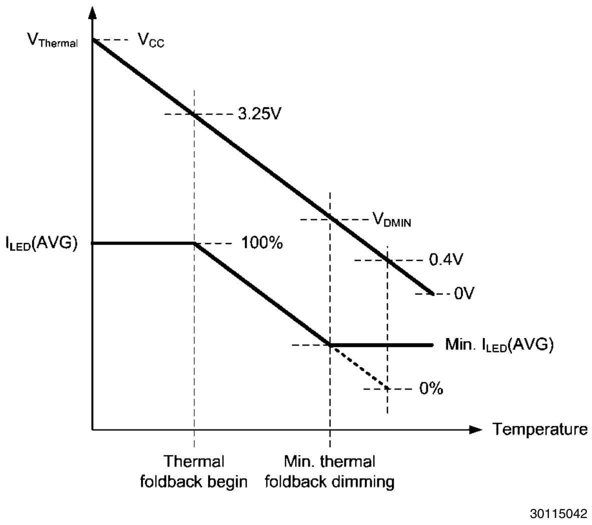


FIGURE 10. Thermal Foldback Control with Minimum Dimming Duty Cycle Limit

To define the minimum thermal dimming duty cycle, a voltage in between 0.4V to 3.25V should be applied to the DMIN pin. The minimum duty cycle is governed by the following equation:

$$D_{MINIMUM} = [(V_{DMIN} - 0.4) \text{ X } 35]\%$$

$$\text{for } 0.4 \leq V_{DMIN} \leq 3.25V$$

When the voltage at the DMIN pin is below 0.4V (e.g. connect to GND), the minimum thermal dimming feature is disabled. In applications that thermal foldback control is not required, the DMIN pin can be tied to GND to reduce power consumption.

PWM DIMMING

The LM3464 provides a DIM pin that accepts TTL logic level signal for PWM dimming. When the DIM pin is pulled low, all LED current regulators will turn off while maintaining V_{CC} regulator and part of the internal circuitries operating. External pull up resistor is required if the DIM pin is driven by open collector / drain driver. PWM dimming guarantees uniform color temperature of the light throughout the entire dimming range. The average current of every output channel is decided by the dimming duty cycle and follows the equation below:

$$I_{LED(AVG)} = D_{PWM} \times I_{LED}$$

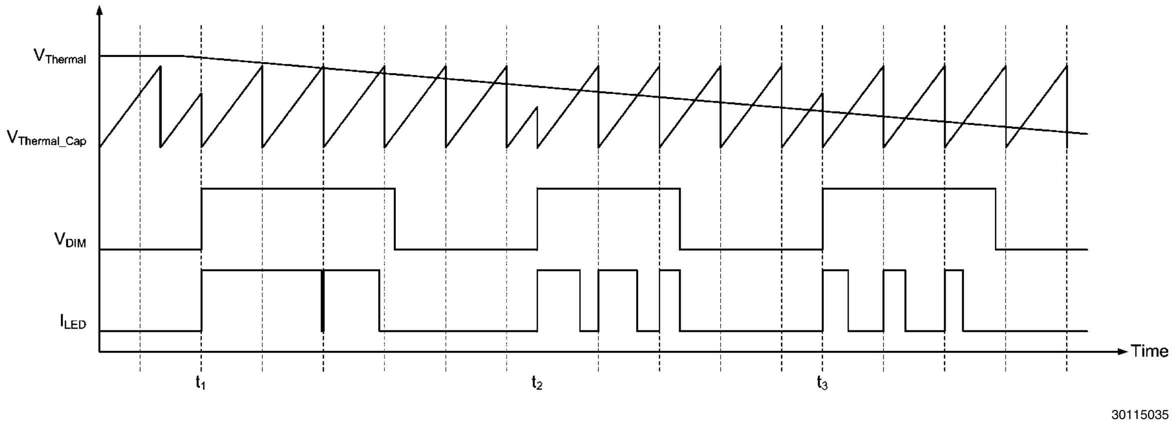


FIGURE 11. Thermal Foldback + PWM Dimming Control

PWM DIMMING CONTROL WITH THERMAL FOLDBACK

The PWM dimming control can coexist with thermal foldback by applying PWM dimming control signal and thermal control signal to the DIM and Thermal pins concurrently. Normally, the dimming frequency for the thermal foldback should be much higher than that of the PWM dimming control signal. Figure 10 presents the relationship among $V_{Thermal}$, $V_{Thermal\_Cap}$, V_{DIM} and I_{LED}. As shown in the Figure, when thermal foldback is in functional, the average output current can be further decreased linearly according to the duty cycle of the PWM dimming signal being applied to the DIM pin. In order to synchronize the dimming signals, the C_{THM} is discharged on every rising edge of the PWM dimming signal on DIM pin, notice as t_1, t_2 and t_3 in Figure 11.

LOW POWER STANDBY

The LM3464 will enter low power standby mode when the EN pin is pulled to GND. The EN pin is internally biased thus no external pull-up resistor or bias is required. Under standby mode, all the output channels are cut-off and part of the internal circuitries are disabled to maintain low power consumption. The OutP pin will stop sinking current from the feedback node of the primary power stage and causes the rail voltage fall back to $V_{RAIL(nom)}$ slowly. The V_{CC} regulator will maintain operation to supply power and bias for external circuities. When the EN pin is released (floating), the LM3464 exits low power standby mode and the startup sequence begins as described in Figure 3.

FAULT HANDLING and INDICATION

The LM3464 features a complete mechanism for fault handling and indication. The LM3464 detects LED failures like open and short circuits of LED strings, insufficient supply voltage etc. In order to avoid false triggering the fault detection circuitry, the LM3464 features a timer for fault recognition. When a fault condition fulfils and sustains longer than certain preset delay time, a fault is confirmed and the Faultb pin will be pulled low as an indication. The delay time for fault detection is defined by the value of the capacitor connects across the FAULT_CAP pin and GND, C_{FLT}. Normally, a 2.2 nF C_{FLT} that set a 264 us delay time is suitable for most application. For those applications with slow response primary power supply, the value of C_{FLT} may need to increase accordingly. The time delay for fault detection is governed by the following equation:

$$T_{FAULT} = \frac{C_{FLT} \times 3.0V}{25\ \mu A}$$

OPEN CIRCUIT OF LED STRINGS

Detection of LED open circuit is facilitated by detecting both the V_{SEx} and the internal gate signal before feeding to the internal MOSFET gate driver. When a LED string is open circuit, the V_{SEx} pin will be pulled down to below 30mV by the current sensing resistor. As V_{SEx} falls below its regulated level, LM3464 will then push up the gate voltage of the corresponding MOSFET (V_{GDx}) and try to maintain current regulation. Thus, a fault of open circuit will be detected when V_{SEx} falls below 30mV and internal gate voltage reaches its maximum (V_{GDx} is about 5V).

When fault happens and the fault recognition time defined by C_{FLT} expires, the failed channel(s) will be cut-off. To reactivate those cut-off channel(s), the EN pin should be pulled to GND for soft reset or repowering the whole system for system reset, then the startup sequence shows in Figure 3 starts-over.

SHORT CIRCUIT OF LED STRINGS

In the situations that the system has been normally started up and the LEDs in a LED string are shortened, the corresponding drain voltage (DRx) will increase so as to maintain correct current regulation. When drain voltage of that particular channel rises up to 8.4V higher than those of other channels, the channel with LEDs shortened will be latched off and isolated from the system to avoid further damages. Once a situation is recognized as fault, no matter it is due to inappropriate operation, failure of source power or shortening / disconnecting of LED strings, the Faultb pin will be pulled low. The Faultb pin is an active low output (normal high) that can be use as an acknowledgement pin of the LM3464 to report failure to the supporting control circuitries such as hosting micro-controller.

DRIVING LESS THAN FOUR LED STRINGS

The LM3464 allows users to disable the unused output channels. Any output channel without a LED string connected or with DRX and SEx pins floating will be disabled at system startup. A disabled channel will be taken out from the DHC loop and will not contribute headroom control signal to the LM3464. This function is applicable to both single LM3464 and cascade operation modes.

EXPANDING NUMBER OF OUTPUT CHANNEL

The LM3464 can be cascaded to expand the number of output channel. Bases on the master-slave architecture, one of the LM3464 in the system must be set to master mode and the rest must be set to slave mode. Figure 13 shows an example application circuit that features eight output channels.

To enable cascade operation, the SYNC pin of the master LM3464 should connect to the DIM pin of the first slave device and similarly the SYNC pin of such slave device should connect to its down stream slave device for startup synchronization. In addition, the OutP pins of all the LM3464 have to tie up though a diode and resistor R_{DHC} to the voltage feedback node of the primary power supply to accomplish dynamic headroom control.

The slave devices can only be commanded by the master LM3464. With the connections between master and slave devices, the information of startup synchronization, thermal foldback and PWM dimming are gathered by the master device and then distribute stage by stage through the SYNC pin.

To set a LM3464 in master mode, the voltage of the VLedFB pin must be below 3.25V. When the VLedFB pin is connected to VCC, the device is in slave mode. In slave mode, local thermal foldback and PWM control are overridden by the packaged synchronization signal delivered from the master.

CONNECTION TO LED ARRAYS

When LEDs are connected to the LM3464 driver stage through long cables, the parasitic components of the cable harness and MOSFETS may resonant and eventually lead to unstable system operation. In applications with over 1 meter cables between the LM3464 driver stage and LED light engine, a 4.7kΩ resistor should be added across the GDx pins to GND as shown in Figure 12.

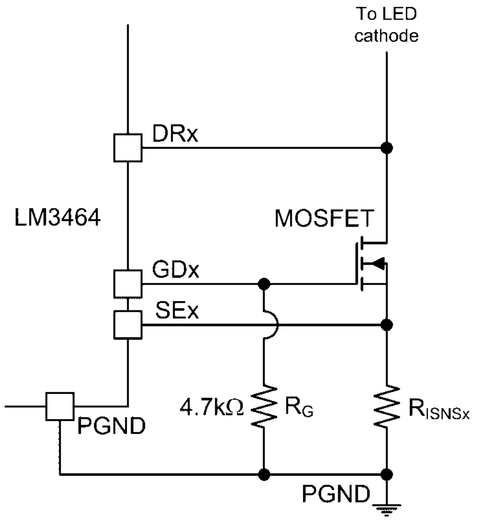


FIGURE 12. Additional Resistor Across GDx and SEx for Cable Harness Over 1m Long

Additional Application Circuit

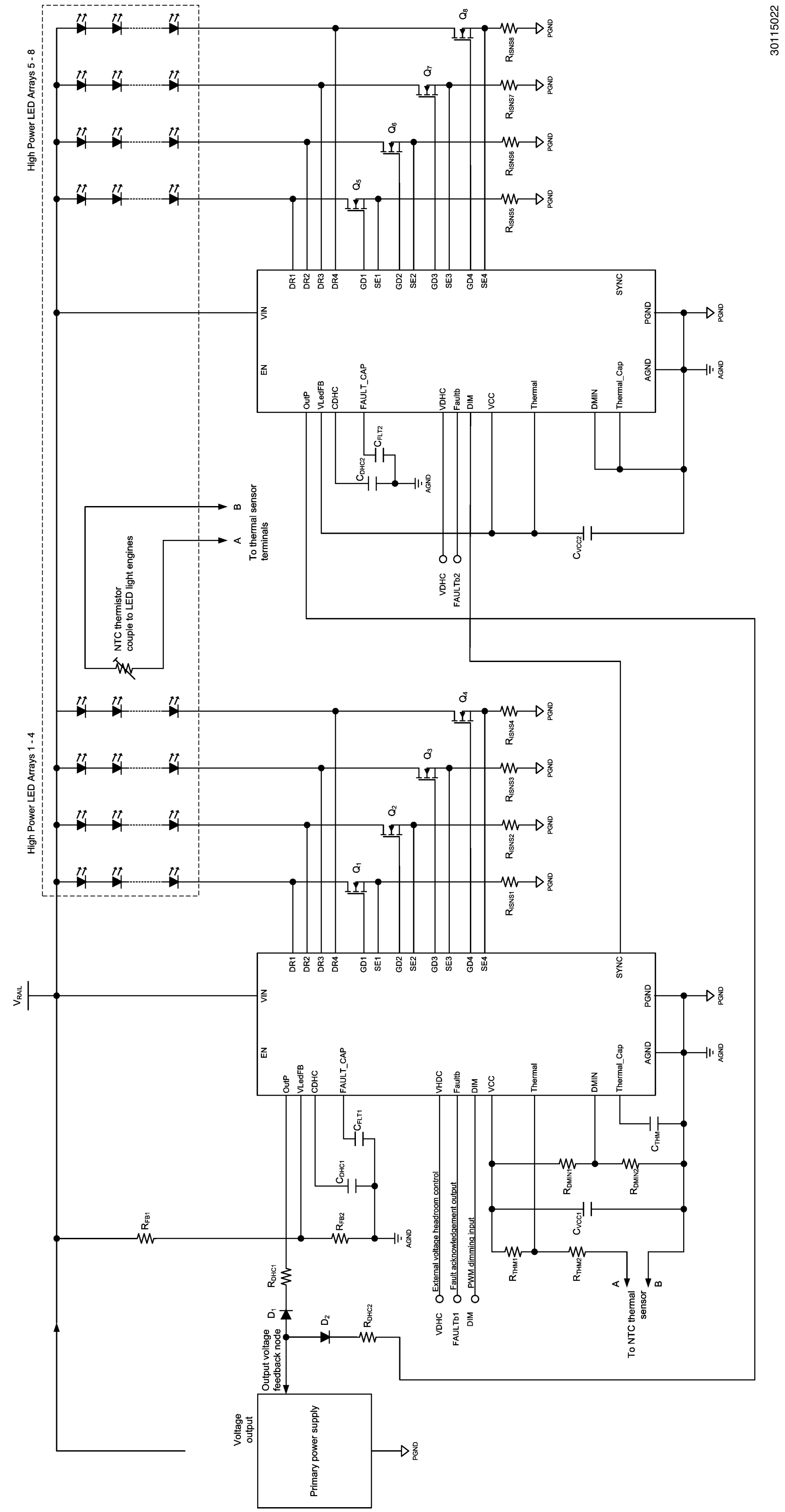
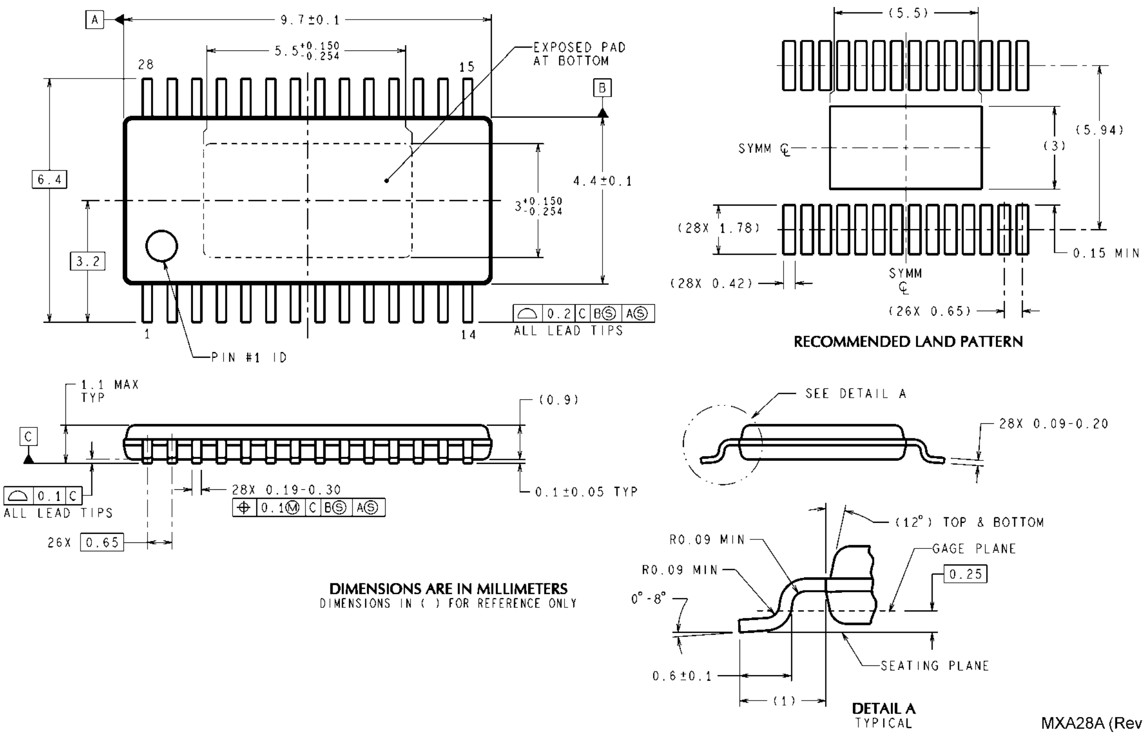


FIGURE 13. Cascade Operation with Thermal Foldback Control

Physical Dimensions inches (millimeters) unless otherwise noted



MXA28A (Rev D)

28-Lead eTSSOP Package
NS Package Number MXA28A

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