October 1998

SPC8110F0A LOCAL BUS LCD/CRT VGA CONTROLLER

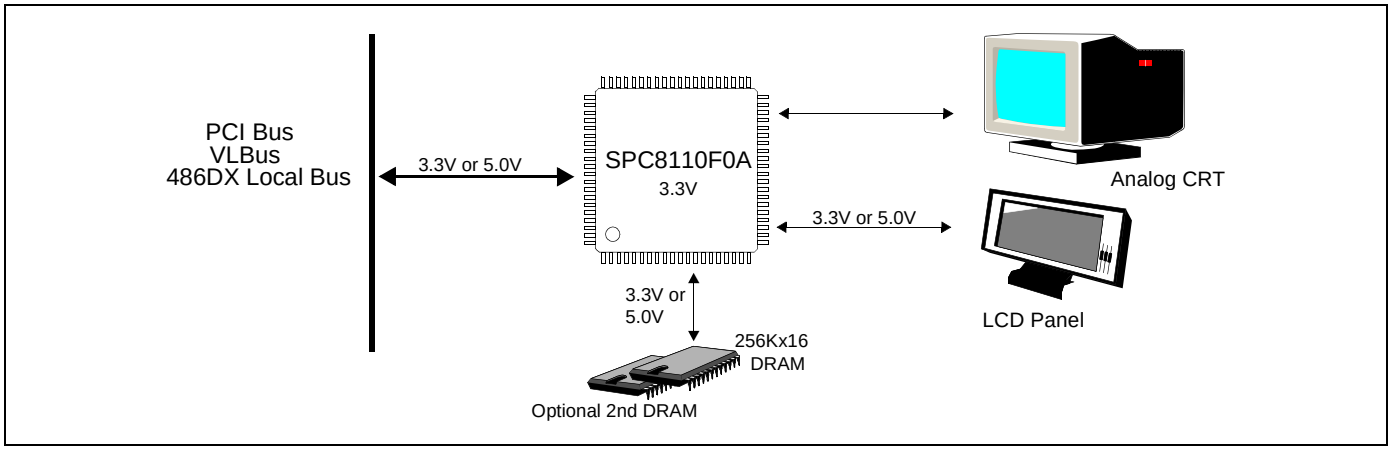
■ DESCRIPTION

The SPC8110 is a single chip, multi-function, mixed voltage LCD/CRT VGA controller. This controller features an integrated RAMDAC, PLL, Bit Block Transfer engine (BitBLT) and a CPU local bus interface. The SPC8110 accelerates the display of graphical user interface software on flat panel and analog CRT displays.

■ KEY FEATURES

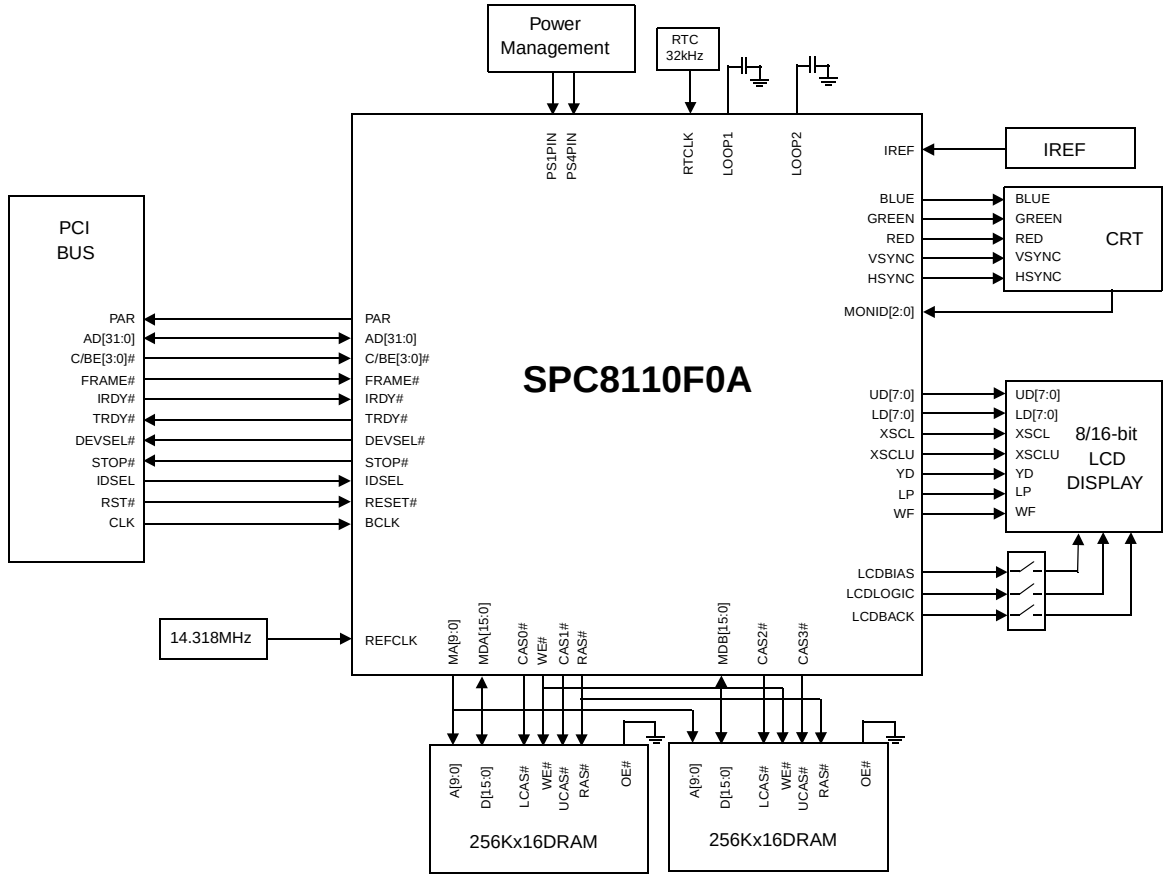
- Hardware VGA compatible
- 32-bit PCI, VL-Bus or 486DX local bus direct Interface
- 512KB or 1024KB display memory using one or two 256K x 16 self-refresh DRAM, respectively (CAS or WE controlled; symmetrical or asymmetrical addressing)
- Hardware Bit Block Transfer engine
- Hardware 64 x 64 pixel 2-bit cursor
- Hardware color expansion
- Linear mode addressing
- Internal PLL and clock generation
- Internal 256 x 18-bit RAMDAC
- Direct analog CRT drive
- 9/12/16/18-bit TFT LCD Panel support
- 4/8/16-bit passive LCD Panel support
- Multi-resolution LCD Panel interface: dual panel-dual drive, single panel-single drive
- 16, 32 & 64 LCD gray shades by Frame Rate Modulation (FRM) and dithering
- Maximum 256 simultaneous colors from a possible 256K colors on LCD or CRT
- Simultaneous LCD and analog CRT display
- Vertical centering and expansion
- LCD panel power sequencing
- Extensive hardware and software activated power save modes and status signals
- 3.3/5.0 mixed voltage operation
- 208 pin QFP8 S1 package

■ BLOCK DIAGRAM



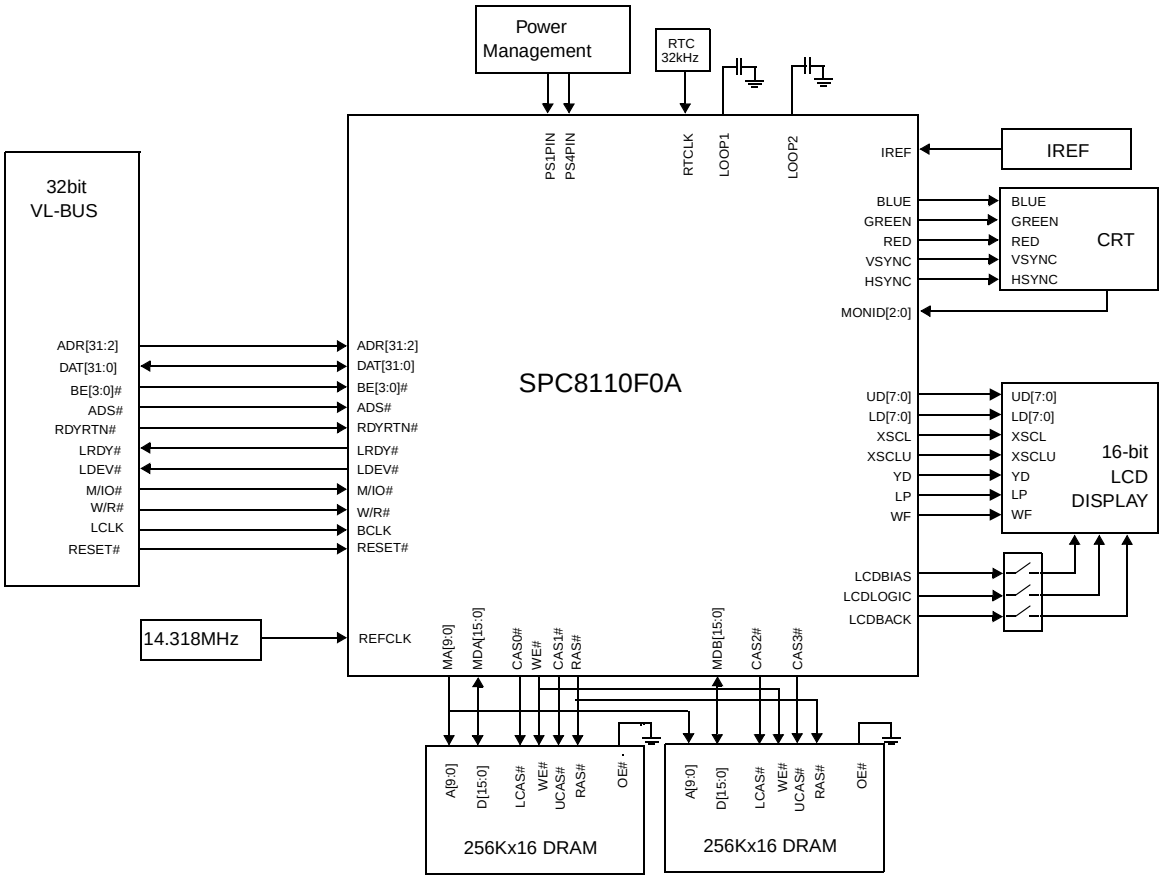
■ PCI BUS SYSTEM BLOCK DIAGRAM

Shown with 1024 KB memory option



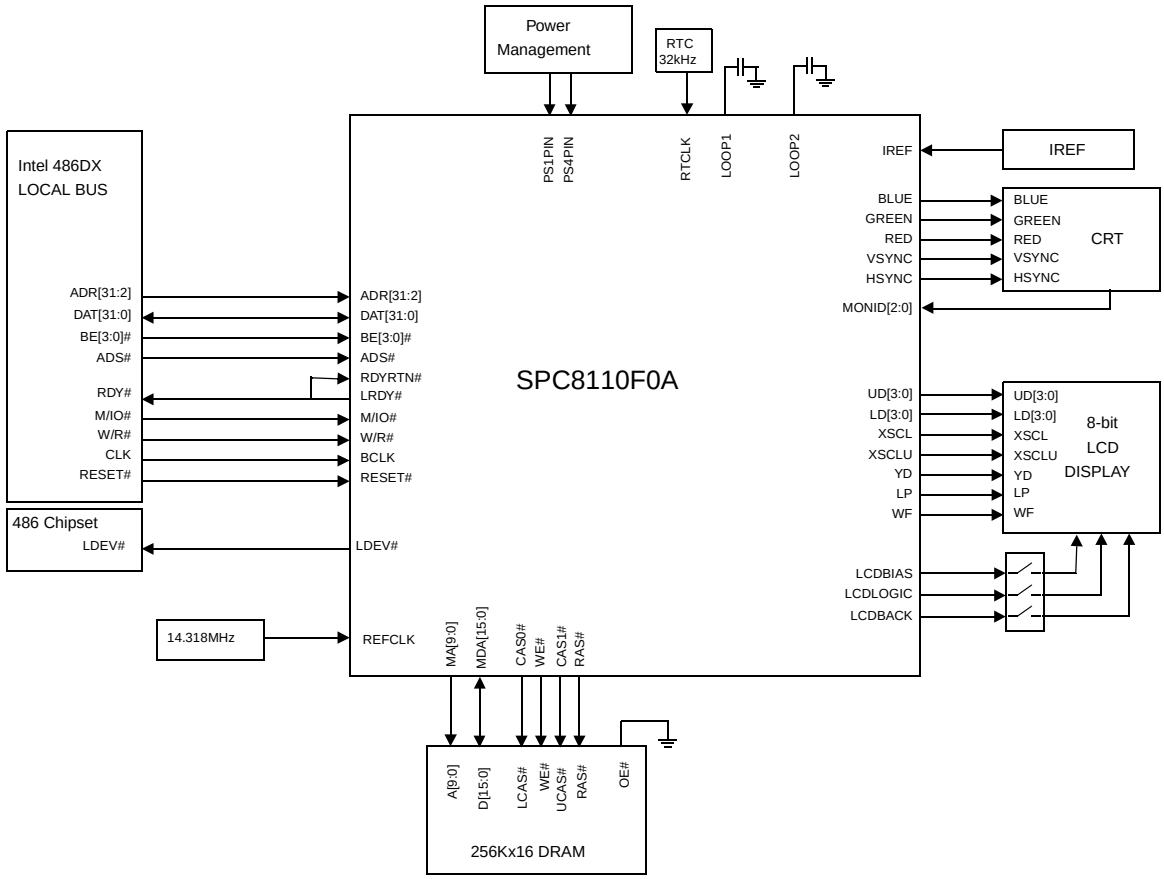
■ VL-BUS SYSTEM BLOCK DIAGRAM

Shown with 1024 KB memory option



■ 486DX-33 LOCAL BUS SYSTEM BLOCK DIAGRAM

Shown with 512 KB memory option

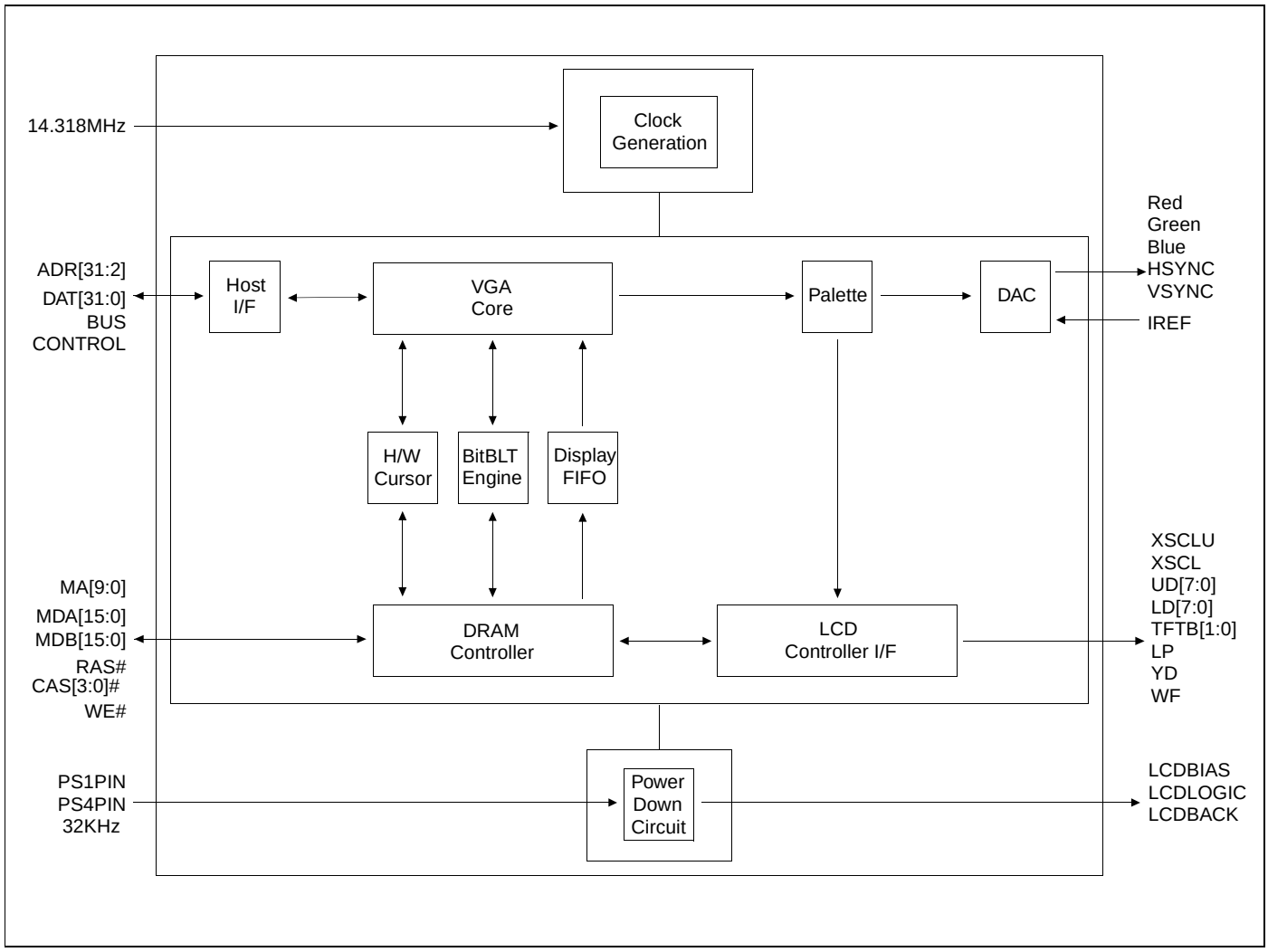


■ SPC8110 VIDEO MODES

Mode No. (Hex)	Pixels Addressable		Horizontal Pixels Displayed		Vertical Pixels Displayed	Font Size		Number of Shades			Nominal Frame Rate (Hz) for 1024KB RAM		
	Horizontal (characters)	Vertical (rows)	CRT	LCD		CRT	LCD	Mono LCD	Color LCD	CRT	CRT (typical)	Single Panel LCD	Dual Panel LCD
0	(40)	(25)	320	320	200	8x8	8x8	16	16	16	70	79	78
0+	(40)	(25)	320	320	350	8x14	8x14	16	16	16	70	79	78
0++	(40)	(25)	360	320	400	9x16	8x16	16	16	16	70	79	78
1	(40)	(25)	320	320	200	8x8	8x8	16	16	16	70	79	78
1+	(40)	(25)	320	320	350	8x14	8x14	16	16	16	70	79	78
1++	(40)	(25)	360	320	400	9x16	8x16	16	16	16	70	79	78
2	(80)	(25)	640	640	200	8x8	8x8	16	16	16	70	79	78
2+	(80)	(25)	640	640	350	8x14	8x14	16	16	16	70	79	78
2++	(80)	(25)	720	640	400	9x16	8x16	16	16	16	70	79	78
3	(80)	(25)	640	640	200	8x8	8x8	16	16	16	70	79	78
3+	(80)	(25)	640	640	350	8x14	8x14	16	16	16	70	79	78
3++	(80)	(25)	720	640	400	9x16	8x16	16	16	16	70	79	78
4	320	200	320	320	200	n/a	n/a	4	4	4	70	79	78
5	320	200	320	320	200	n/a	n/a	4	4	4	70	79	78
6	640	200	640	640	200	n/a	n/a	2	2	2	70	79	78
7	(80)	(25)	640	640	350	8x14	8x14	2	2	2	70	79	78
7+	(80)	(25)	720	640	400	9x16	8x16	2	2	2	70	79	78
0D	320	200	320	320	200	n/a	n/a	16	16	16	70	79	78
0E	640	200	640	640	200	n/a	n/a	16	16	16	70	79	78
0F	640	350	640	640	350	n/a	n/a	2	2	2	70	79	78
10	640	350	640	640	350	n/a	n/a	16	16	16	70	79	78
11	640	480	640	640	480	n/a	n/a	2	2	2	60	79	78
12	640	480	640	640	480	n/a	n/a	16	16	16	60	79	78
13	320	200	320	320	200	n/a	n/a	64	256	256	70	79	78
6A	800	600	800	800	600	n/a	n/a	16	16	16	72	60	72
100	640	400	640	640	400	n/a	n/a	64	256	256	70	79	78
101	640	480	640	640	480	n/a	n/a	64	256	256	60	79	78
102	800	600	800	800	600	n/a	n/a	16	16	16	72	60[2]	72
103	800	600	800	800	600	n/a	n/a	64	256	256	72	60[2]	72[1]
104	1024	768	1024	1024	768	n/a	n/a	16	16	16	60	n/a[2]	70
105	1024	768	1024	n/a	768	n/a	n/a	64	n/a	256	60[1]	n/a[2]	n/a
108	(80)	(60)	640	640	480	8x8	8x8	16	16	16	60	79	78
109	(132)	(25)	1056	n/a	350	8x14	n/a	n/a	n/a	16	70	n/a	n/a
10A	(132)	(43)	1056	n/a	350	8x8	n/a	n/a	n/a	16	70	n/a	n/a
10B	(132)	(50)	1056	n/a	400	8x8	n/a	n/a	n/a	16	70	n/a	n/a
10C	(132)	(60)	1056	n/a	480	8x8	n/a	n/a	n/a	16	60	n/a	n/a

1. Only available with 1024KB RAM.
2. Support for large TFT panels requires custom BIOS and drivers.

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

Host Interface

The Host Interface can be programmed to accommodate any of the following three standards: Intel486 DX local bus interface, VL-Bus interface and PCI interface. It has a one-stage buffer for zero wait-state write operation.

Clock Generator

The Clock Generator contains two PLLs that are separately programmed to produce the memory and pixel clocks from a single clock source. The reference clock is typically 14.318 MHz.

VGA Core

The VGA Core contains the Sequencer, CRTC Controller, Graphics Controller, Attribute Controller, and the rest of the standard VGA circuitry.

Hardware Cursor

The Hardware Cursor generates a 64 x 64 x 2-bit hardware cursor or sprite that can be overlaid on the displayed image.

BitBLT Engine

The Bit Block Transfer Engine performs read, write, and move blits, solid fills, destination inversions, and pattern fills. It performs all data alignment and masking at the blit boundary and also performs color expansion to accelerate the writing of text images. The Bit Block Transfer Engine operates in both 4-bit planar mode and 8-bit linear (packed-pixel) mode.

Display FIFO

The Display FIFO is an 8 stage FIFO that is used to buffer the video data from display memory.

VGA Palette

The VGA Palette implements the standard 256-word x 18-bit VGA lookup table, plus 4-word x 18-bit entries for Hardware Sprites.

DAC

The DAC functions as a triple 6-bit 65 MHz DAC to drive the RGB outputs connected to the analog display.

LCD Interface

The LCD Interface contains frame rate modulation and dithering circuitry displaying a maximum of 64 shades of gray in monochrome LCD mode. In color LCD mode, it uses frame rate modulation (FRM) to display 256 out of a possible 4096 colors, and additional dithering techniques for a full 256K possible colors.

Power Save Logic

Power Save Logic implements all the power down features of the chip.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS} - 0.3 to 7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	°C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
HV_{DD}	Supply Voltage	V_{SS} = 0 V	4.5	5.0	5.5	V
LV_{DD}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
V_{IN}	Input Voltage	V_{SS}	V_{SS}	--	V_{DD}	V
T_{OPR}	Operating Temperature		0	25	70	°C
I_{OPR}	Average Power Consumption			381.7		mW

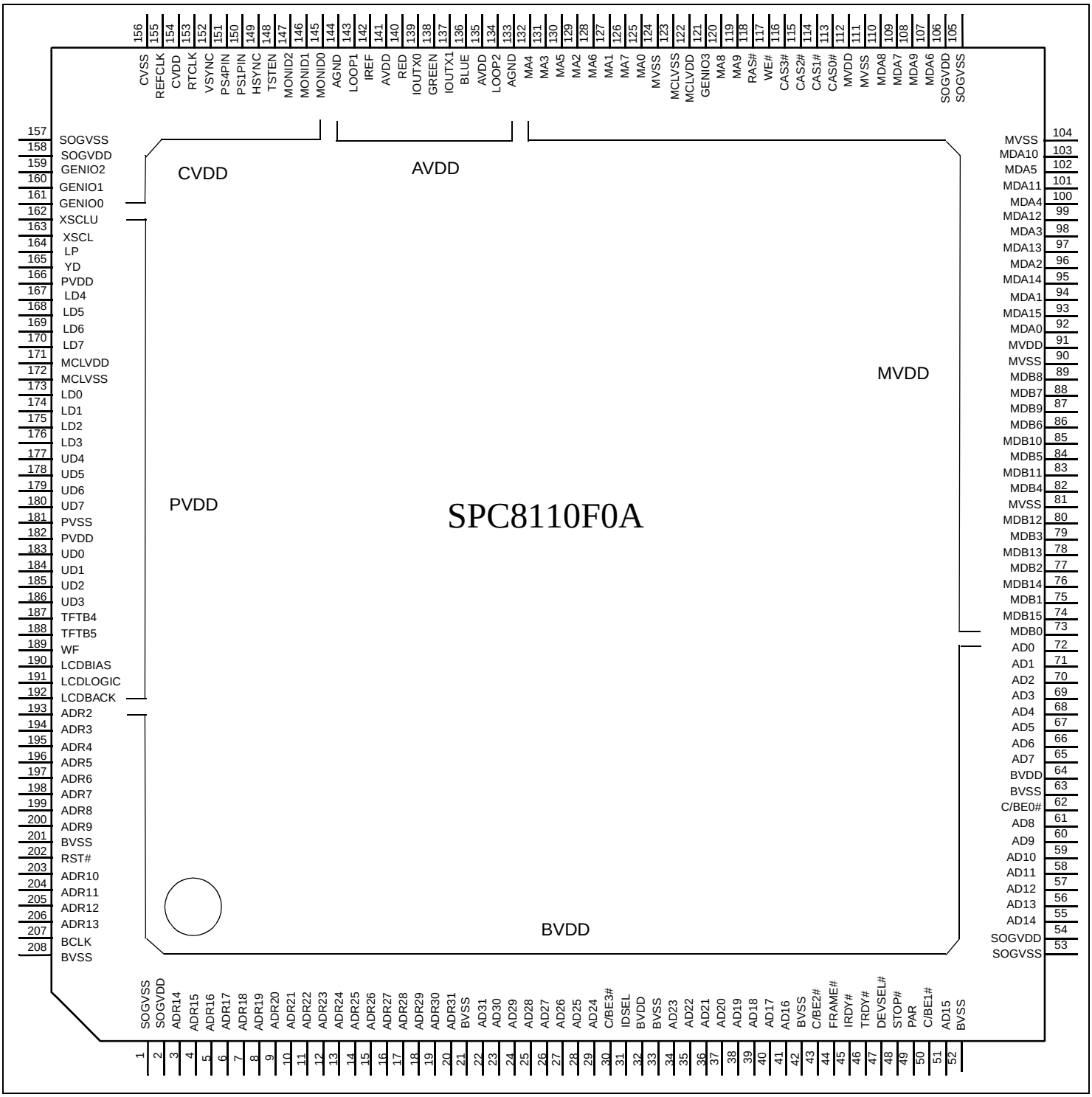
Input Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage	V_{DD} = 4.5V/3.0V	--	--	0.8	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.5V/3.6V	2.0	--	--	V
HR_{PD}	Pull Down Resistance	V_{DD} = 5V	25	50	100	KΩ
LR_{PD}	Pull Down Resistance	V_{DD} = 3.3V	45	90	180	KΩ
V_{T+}	Positive-going Threshold CMOS Schmitt Trigger	V_{DD} = 5/3.3V			2.4	V
V_{T-}	Negative-going Threshold CMOS Schmitt Trigger	V_{DD} = 5/3.3V	0.6			V
HV_H	Hysteresis Voltage CMOS Schmitt Trigger	V_{DD} = 5/3.3V	0.1			V
C_{IN}	Clock Pin Capacitance	BCLK, RESET#, REFCLK, MONID[2:0], TSTEN, PS1PIN,PS4PIN, RTCLK		4		pF
C_{BID}	Input Pin Capacitance	all pins not listed in C_{IN}		10		pF
I_L	Input Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	-1		1	µA

Output Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage Type 2 Type 3 Type 4	V_{DD} = 5/3.3V I_{OL} = 6mA I_{OL} = 12mA I_{OL} = 24mA			V_{SS} + 0.3	V
V_{OH}	High Level Output Voltage Type 2 Type 3 Type 4	V_{DD} = 5/3.3V I_{OH} = -2mA I_{OH} = -4mA I_{OH} = -8mA	V_{DD}- 0.3			V
I_{OZ}	Off-state Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	-1		1	µA

■ SPC8110 PIN OUT



Note: Pin names correspond to the PCI bus configuration.
Pin placement subject to change.

■ PIN DESCRIPTION

Key:						
	A	=	Analog	P	=	Power
	I	=	Input	SCH	=	Schmitt Trigger
	O	=	Output	PD	=	Pull Down
	I/O	=	Bidirectional			

■ CPU INTERFACE

PCI Bus

Pin Name	Type	Output Type	Pin No.	Description
AD[31:0]	I/O	4	22-29, 34-41, 51, 55-61, 65-72	PCI multiplexed Address and Data Bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times.
ADR[31:2]	I	--	20-3, 206-203, 200-193	Unused VL-Bus Address inputs. These pins should be tied high in PCI mode.
C/BE[3:0]#	I	--	30, 43, 50, 62	PCI Bus Command and Byte Enables.
IDSEL	I	--	31	PCI Bus Initialization Device Select.
STOP#	I/O	4	48	PCI Bus Stop.
FRAME#	I	--	44	PCI Bus Cycle Frame.
IRDY#	I	--	45	PCI Bus Initiator Ready.
PAR	O	4	49	Parity. This line is driven by the chip only during read cycles, and is in a hi-Z state at all other times. It is always hi-Z and should be tied high in VL Bus mode.
BCLK	I	--	207	PCI Bus Clock.
TRDY#	I/O	4	46	PCI Bus Target Ready.
DEVSEL#	O	4	47	PCI Bus Device Select.
RST#	I w/SCH	--	202	CPU Reset. The active low reset signal from the CPU clears all internal registers and forces all signals to their inactive state. On the rising edge of the RESET# the MDA[0...15] bus is latched in for configuration.

Intel486/VL-Bus

Pin Name	Type	Output Type	Pin No.	Description
ADR[31:2]	I	--	20-3, 206-203, 200-193	VL-Bus Address inputs. These inputs are unused and must be tied high in PCI Bus mode.
DAT[31:0]	I/O	4	22-29, 34-41, 51, 55-61, 65-72	VL-Bus Data inputs. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times.
BE[3:0]#	I	--	30, 43, 50, 62	VL-Bus byte enables.
W/R#	I	--	31	VL-Bus Write or Read Status.
M/IO#	I	4	48	VL-Bus Memory or I/O Status.
ADS#	I	--	44	VL-Bus Address Data Strobe.
RDYRTN#	I	--	45	VL-Bus Ready Return.
BCLK	I	--	207	VL-Bus Local CPU Clock.
LRDY#	O	4	46	VL-Bus Local Ready.
LDEV#	O	4	47	VL-Bus Local Device.
RESET#	I w/SCH	--	202	CPU Reset. The active low reset signal from the CPU clears all internal registers and forces all signals to their inactive state. On the rising edge of the RESET# the MDA[0...15] bus is latched in for configuration.
PAR	O	4	49	Unused (Parity). This line is used in PCI mode only. It is hi-Z at all times in VL-Bus mode and should be tied high.

■ VIDEO MEMORY INTERFACE

Pin Name	Type	Output Type	Pin No.	Description
MA[9:0]	O	2	119, 120, 126, 128, 130, 132, 131, 129, 127, 125	Multiplexed row/column address bits for video display memory.
MDA[15:0]	I/O w/ PD	2	93, 95, 97, 99, 101, 103, 108, 110, 109, 107, 102, 100, 98, 96, 94, 92	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET# is low, or when MClkOFF is active. These pins are also used as configuration inputs. They have internal pull down resistors that have typical values of 50KΩ/100KΩ at 5V/3.3V respectively.
MDB[15:0]	I/O w/ PD	2	74, 76, 78, 80, 83, 85, 87, 89, 88, 86, 84, 82, 79, 77, 75, 73	Data bits for video display memory when 1024KB of memory is present. The output drivers of these pins are placed into a high-impedance state when RESET# is low, or when MClkOFF is active. The inputs have internal pull down resistors that have typical values of 50K Ω/100K Ω at 5 V/3.3 V respectively. They should be left open-circuit when only 512KB of memory is attached.
RAS#	O	2	118	DRAM Row Address Strobe.
CAS[0]# (CAS#)	O	2	113	DRAM Column Address Strobe for MDA[7:0], or Column Address Strobe for all bytes, as configured by an auxiliary register.
CAS[3:1]# (WE[3:1]#)	O	2	116-114	DRAM Column Address Strobes or Write Enable Strobes for {MDB[15:0],MDA[15:8]}, as configured by an auxiliary register. CAS[3:2]# (WE[3:2]#) are unused and should be left open-circuit when only 512KB of memory is present.
WE# (WE[0]#)	O	2	117	DRAM Write Enable Strobe for all bytes or Write Enable Strobe for MDA[7:0], as configured by an auxiliary register.

■ CLOCK INPUTS

Pin Name	Type	Output Type	Pin No.	Description
REFCLK	I	--	155	This pin is the reference clock used by the internal PLLs to generate all the necessary clocks. This must be stable during full operation. REFCLK may shut down only after the chip is totally powered down. Input frequency is typically 14.318 MHz.
RTCLK	I	--	153	Real Time Clock. This input must be used to provide a low frequency clock for generating DRAM refresh. This clock must be approximately 32 kHz and 50% duty cycle.

■ CRT INTERFACE

Pin Name	Type	Output Type	Pin No.	Description
RED, GREEN, BLUE	AO	--	140, 138, 136	Analog outputs from the Video DAC. Internal comparator for monitor sense is available on all three pins. This pin should be connected to AGND if the DAC is not required.
HSYNC	O	3	149	Horizontal Sync. This output is driven to indicate the horizontal retrace period. In CRT only mode, the polarity of this signal is controlled by register 3C2h, bit 6. In TFT or double scan mode this bit is active low to indicate 640 x 480 resolution. This pin is held low in LCD modes. This pin follows the DPMS standard during power down modes.
VSYNC	O	3	152	Vertical Sync. This output is driven to indicate the vertical retrace period. In CRT only mode, the polarity of this signal is controlled by register 3C3h, bit 7. In TFT or double scan mode this bit is active low to indicate 640 x 480 resolution. This pin is held low in LCD modes. This pin follows the DPMS standard during power down modes.
IREF	AI	--	142	Current reference input for the Video DAC. This pin should be connected to AGND if the DAC is not required. See "External Reference Component Values" document, X07G-G-002-xx.
MONID[2:0]	I	--	147-145	Monitor ID bits. Connected to the CRT to identify the monitor type.

■ LCD PANEL INTERFACE

Pin Name	FPDI-1 PIN Name[1]	Type	Output Type	Pin No.	Description
YD	FPFRAME	O	4	165	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	FPLINE	O	4	164	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	FPSHIFT	O	4	163	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
XSCLU	FPSHIFT2	O	4	162	Second Shift Clock for some color LCD displays.
UD[7:0] LD[7:0]	UD[7:0] LD[7:0]	I/O	4	180-177, 186-183, 170-167, 176-173	Panel display data bus. The data format depends on the specific panel connected. These pins are driven low when the LCD interface is disabled (e.g. CRT only mode). For 8-bit panels, UD[7:4] and LD[7:4] are driven low.
TFTB[5:4]	-	O	4	188-187	TFT display data bus for the two lsb of the color blue. For non-TFT panels, these two pins are driven low.
LCDBIAS	-	O	2	190	LCD power control for the LCD bias circuitry. Active (On) polarity is defined by the state of MDA[3] on the rising edge of RESET#.
LCDBACK	-	O	2	192	LCD power control for the LCD back light. Active (On) polarity is defined by the state of MDA[1] on the rising edge of RESET#.
LCDLOGIC	-	O	2	191	LCD power control for the LCD logic circuitry. Active (On) polarity is defined by the state of MDA[2] on the rising edge of RESET#.
WF	MOD	O	4	189	LCD Backplane Bias signal. Output toggling frequency is programmable in an auxiliary register. For TFT panels, this pin outputs the display enable signals.

1. VESA Flat Panel Display Interface Standard (FPDI-1™)

■ MISCELLANEOUS

Pin Name	Type	Output Type	Pin No.	Description
TSTEN	I w/ PD	--	148	This pin, when high, sets the SPC8110F0A into either boundary pin SCAN or pin output drive test, depending on the state of PS1PIN. This input has an internal pull down resistor that has a typical value of 50K/100K Ω at 5 V/3.3 V respectively.
GENIO[3:0]	I/O w/ PD	2	121, 159, 160, 161	General purpose I/O pins. Output state of each pin is programmable to control external devices. See AUX[34h].
LOOP1	I	--	143	Connects to Loop Filter Resister and Capacitor for PLL1, where suggested values are R=70 Ω and C=0.1 uf. See "External Reference Component Values" document, X07G-G-002-xx.
LOOP2	I	--	134	Connects to Loop Filter Resister and Capacitor for PLL2, where suggested values are R=70 Ω and C=0.1 uf. See "External Reference Component Values" document, X07G-G-002-xx.
IOUTX[1:0]	A	--	137, 139	Balanced current output for the DAC. This pin should be connected to AGND if the DAC is not required. See "External Reference Component Values" document, X07G-G-002-xx.

■ POWER SAVE MODE CONTROLS

Pin Name	Type	Output Type	Pin No.	Description
PS1PIN	I w/ SCH, PD	--	150	Pin used to initiate a power save mode 1. The polarity of this pin is programmable and has a default polarity of active low. This input has an internal pull down resistor that has a typical value of 50K/100K Ω at 5 V/3.3 V respectively. When TSTEN is active, the polarity of PS1PIN selects the test to be either boundary pin SCAN (PS1PIN = 1) or pin output drive test (PS1PIN = 0).
PS4PIN	I w/ SCH, PD	--	151	Pin used to initiate a power save mode 4. The polarity of this pin is programmable and has a default polarity of active low. This input has an internal pull down resistor that has a typical value of 50K/100K Ω at 5 V/3.3 V respectively.

■ POWER SUPPLY

Pin Name	Type	Pin No.	Description
SOGVDD	P	158, 106, 54, 2	V_{DD} supply for core logic. (3.3V only.)
MVDD	P	112, 91	V_{DD} supply for memory pins. (Either 3.3V or 5.0V.)
BVDD	P	32, 64	V_{DD} supply for bus interface pins. (Either 3.3V or 5.0V.)
CVDD	P	154	V_{DD} supply for control interface pins. (Either 3.3V or 5.0V.)
PVDD	P	166, 182	V_{DD} supply for panel interface pins. (Either 3.3V or 5.0V.)
AVDD	P	135, 141	Analog power supply. (3.3V only.)
MCLVDD	P	122, 171	VDD supply for MCL logic. (3.3V only.)
SOGVSS	P	157, 105, 53, 1	VSS supply for core logic.
MVSS	P	111, 124, 104, 90, 81	VSS supply for memory pins.
BVSS	P	201, 208, 21, 42, 52, 33, 63	VSS supply for bus interface pins.
CVSS	P	156	VSS supply for CRT interface pins.
PVSS	P	181	VSS supply for panel interface pins.

Pin Name	Type	Pin No.	Description
AGND	P	133, 144	Analog Ground.
MCLVSS	P	123, 172	VSS supply for MCL logic.

■ INTEL486/VL-BUS TO PCI BUS PIN MAPPING

VL-Bus Name	PCI Name	Pin No.
RESET#	RST#	202
RDYRTN#	IRDY#	45
ADR[31:2]	--	20-3, 206-203, 200-193
W/R#	IDSEL	31
LDEV#	DEVSEL#	47
DAT[31:0]	AD[31:0]	22-29, 34-41, 51, 55-61, 65-72

VL-Bus Name	PCI Name	Pin No.
BCLK	BCLK	207
--	PAR	49
M/IO#	STOP#	48
ADS#	FRAME#	44
LRDY#	TRDY#	46
BE[3:0]#	C/BE[3:0]#	30, 43, 50, 62

■ MIXED VOLTAGE OPERATION

Mixed Voltage	SOGVDD, MCLVDD, AVDD	BVDD	CVDD	PVDD	MVDD
Configuration 1	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Configuration 2					5.0 V
Configuration 3				5.0 V	3.3 V
Configuration 4					5.0 V
Configuration 5			5.0 V	3.3 V	3.3 V
Configuration 6					5.0 V
Configuration 7				5.0 V	3.3 V
Configuration 8					5.0 V
Configuration 9		5.0 V	3.3 V	3.3 V	3.3 V
Configuration 10					5.0 V
Configuration 11				5.0 V	3.3 V
Configuration 12					5.0 V
Configuration 13			5.0 V	3.3 V	3.3 V
Configuration 14					5.0 V
Configuration 15				5.0 V	3.3 V
Configuration 16					5.0 V

■ DEFAULT PIN MAPPING FOR THE VARIOUS LCD AND TFT PANEL OPTIONS

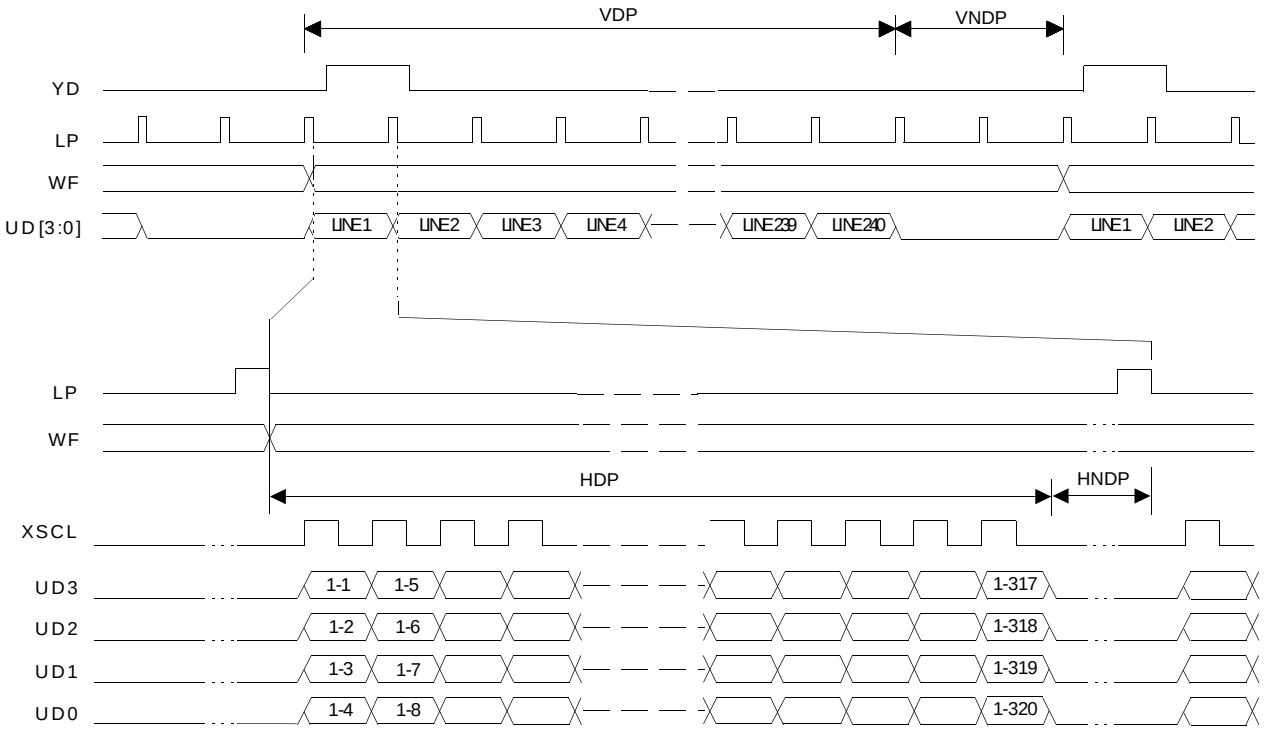
Pin Name	TFT				Color LCD				Mono LCD	
	18-Bit Color	9-Bit x 2 Color	12-Bit Color	9-Bit Color	16-Bit	8-Bit Half Panel	8-Bit	6-Bit	8-Bit	4-Bit
XSCLU	CLK	CLK	CLK	CLK			XSCLU			
XSCL					XSCL	XSCL	XSCL	XSCL	XSCL	XSCL
LP	HS	HS	HS	HS	LP	LP	LP	LP	LP	LP
YD	VS	VS	VS	VS	YD	YD	YD	YD	YD	YD
LD4	R0	R10			LD4				UD0	UD0
LD5	R1	R11			LD5				UD1	UD1
LD6	R2	R12	R0		LD6				UD2	UD2
LD7	R3	R00	R1	R0	LD7				UD3	UD3
LD0	R4	R01	R2	R1	LD0		LD0	LB	LD0	
LD1	R5	R02	R3	R2	LD1		LD1	LG	LD1	
LD2	G0	G10			LD2		LD2	LR	LD2	
LD3	G1	G11			LD3		LD3		LD3	
UD4	G2	G12	G0		UD4	UD4				
UD5	G3	G00	G1	G0	UD5	UD5				
UD6	G4	G01	G2	G1	UD6	UD6				
UD7	G5	G02	G3	G2	UD7	UD7				
UD0	B0	B10			UD0	UD0	UD0	UB		
UD1	B1	B11			UD1	UD1	UD1	UG		
UD2	B2	B12	B0		UD2	UD2	UD2	UR		
UD3	B3	B00	B1	B0	UD3	UD3	UD3			
TFTB4	B4	B01	B2	B1						
TFTB5	B5	B02	B3	B2						
WF	DE	DE	DE	DE	WF	WF	WF	WF/DE	WF	WF
LCDBIAS					(DISP)	(DISP)	(DISP)	(DISP)	(DISP)	(DISP)

■ ALTERNATE PIN MAPPING FOR THE VARIOUS LCD AND TFT PANEL OPTIONS

Pin Name	TFT				Color LCD			Mono LCD	
	18-Bit Color	9-Bit x 2 Color	12-Bit Color	9-Bit Color	16-Bit	8-Bit Half Panel	8-Bit	8-Bit Single	8-Bit Dual
XSCLU	CLK	CLK	CLK	CLK	XSCL	XSCL	XSCL	XSCL	XSCL
XSCL							XSCLU		
LP	HS	HS	HS	HS	LP	LP	LP	LP	LP
YD	VS	VS	VS	VS	YD	YD	YD	YD	YD
LD4	R0	R10							
LD5	R1	R11							
LD6	R2	R12	R0		UD0	UD0	UD0		
LD7	R3	R00	R1	R0	UD1	UD1	UD1	D6	UD2
LD0	R4	R01	R2	R1	UD2	UD2	UD2	D7	UD3
LD1	R5	R02	R3	R2	UD3	UD3	UD3		
LD2	G0	G10			UD4	UD4			
LD3	G1	G11			UD5	UD5			
UD4	G2	G12	G0		LD4				
UD5	G3	G00	G1	G0	LD5			D3	LD3
UD6	G4	G01	G2	G1	LD6			D4	UD0
UD7	G5	G02	G3	G2	LD7			D5	UD1
UD0	B0	B10			UD6	UD6			
UD1	B1	B11			UD7	UD7			
UD2	B2	B12	B0		LD0		LD0		
UD3	B3	B00	B1	B0	LD1		LD1	D0	LD0
TFTB4	B4	B01	B2	B1	LD2		LD2	D1	LD1
TFTB5	B5	B02	B3	B2	LD3		LD3	D2	LD2
WF	DE	DE	DE	DE	WF	WF	WF	WF	WF
LCDBIAS					(DISP)	(DISP)	(DISP)	(DISP)	(DISP)

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

4-Bit Single Panel

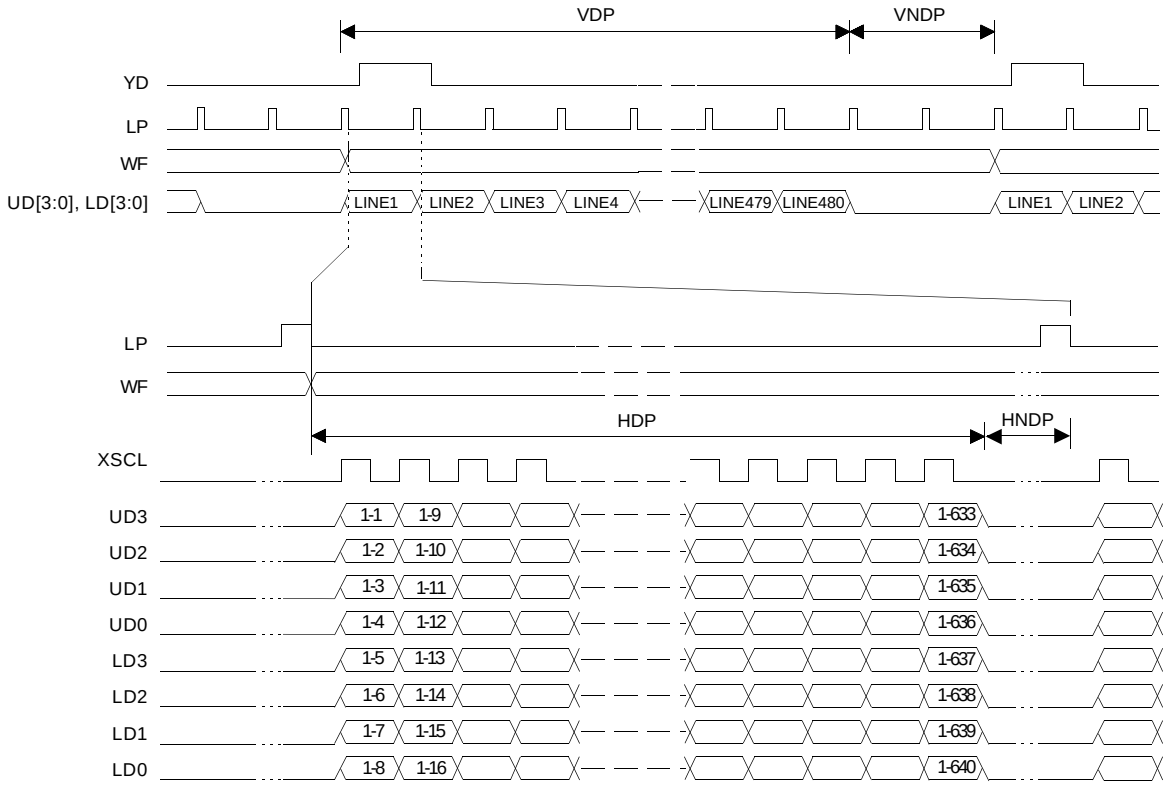


* diagram drawn with 2 LP vertical blank period
Example timing for a 320 x 240 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

8-Bit Single Panel

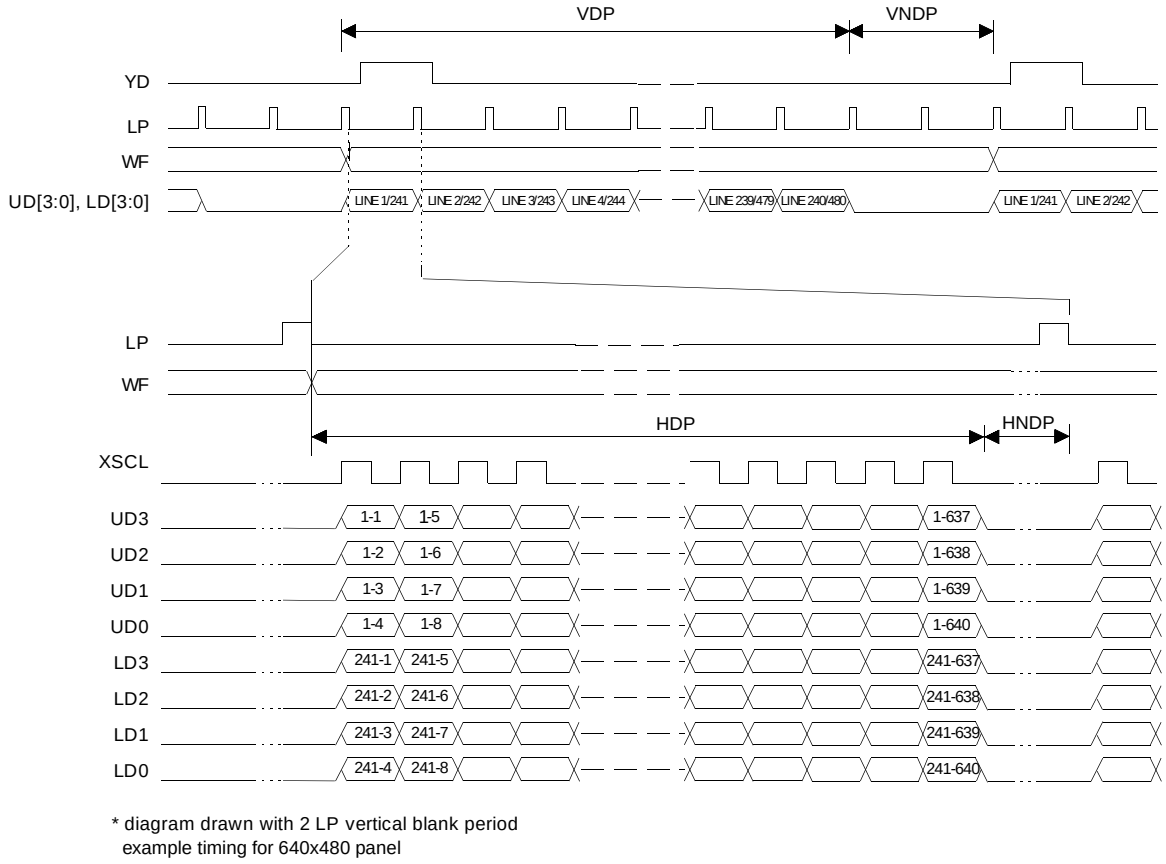


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

8-Bit Dual Panel

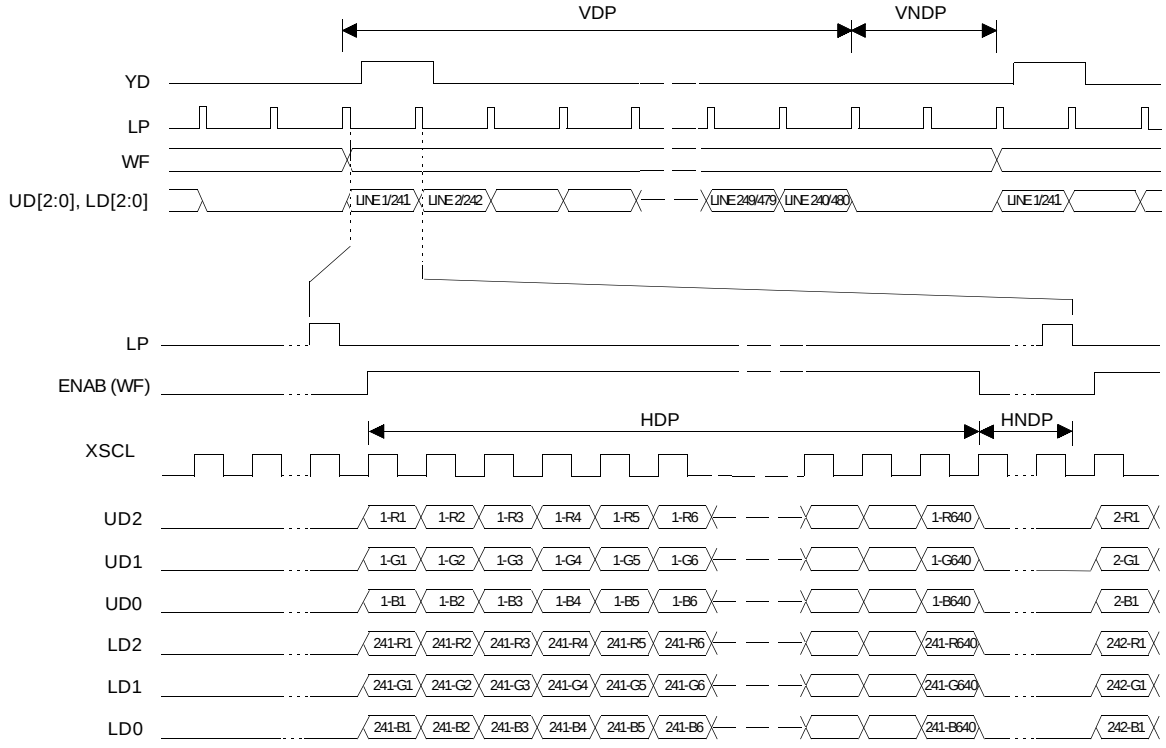


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

6-Bit Dual Color Panel

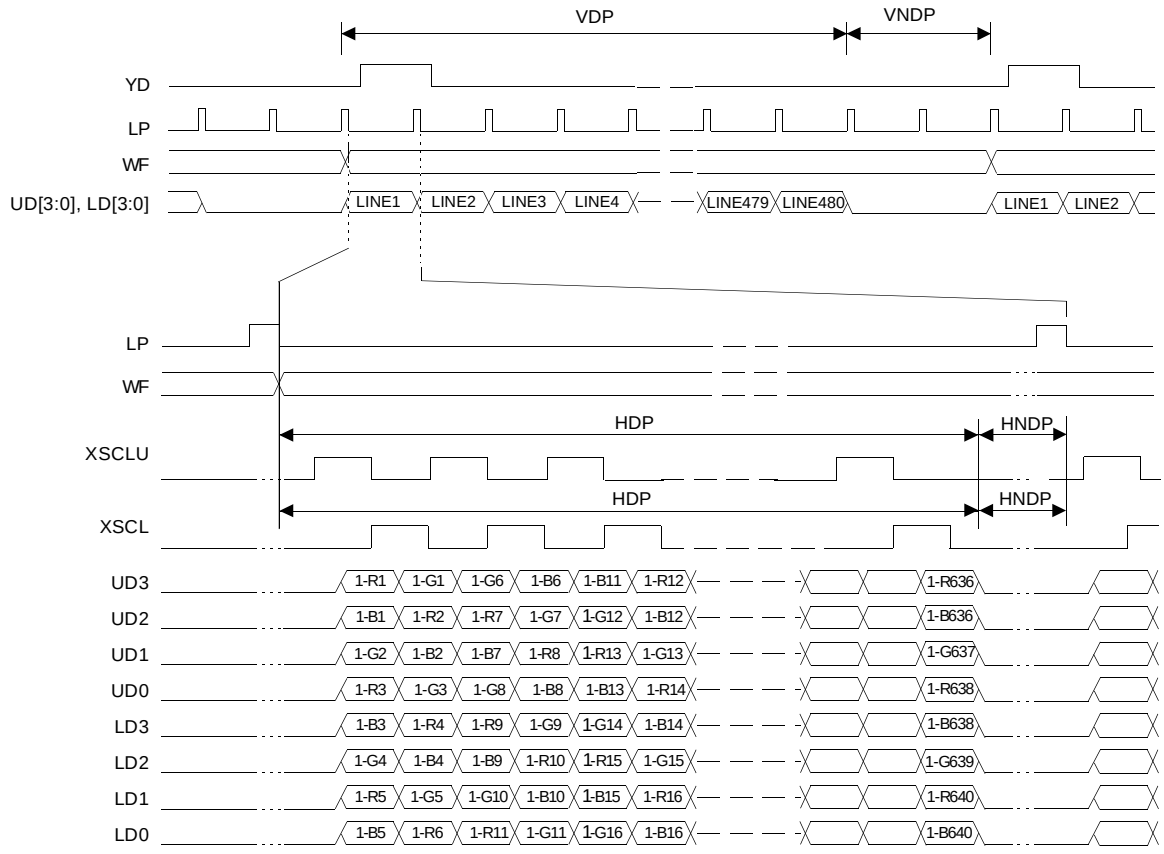


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

8-Bit Single Color Panel

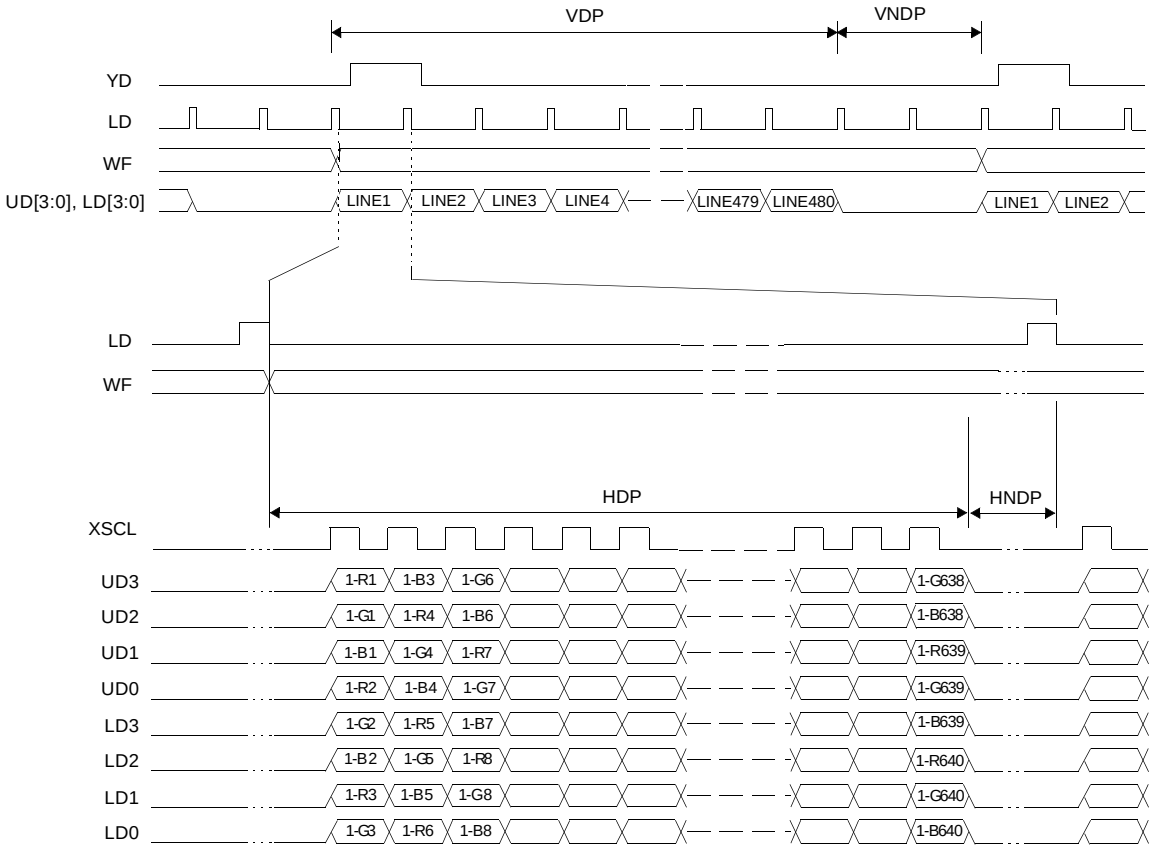


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

8-Bit Single Color Panel (Alternate Data Format)

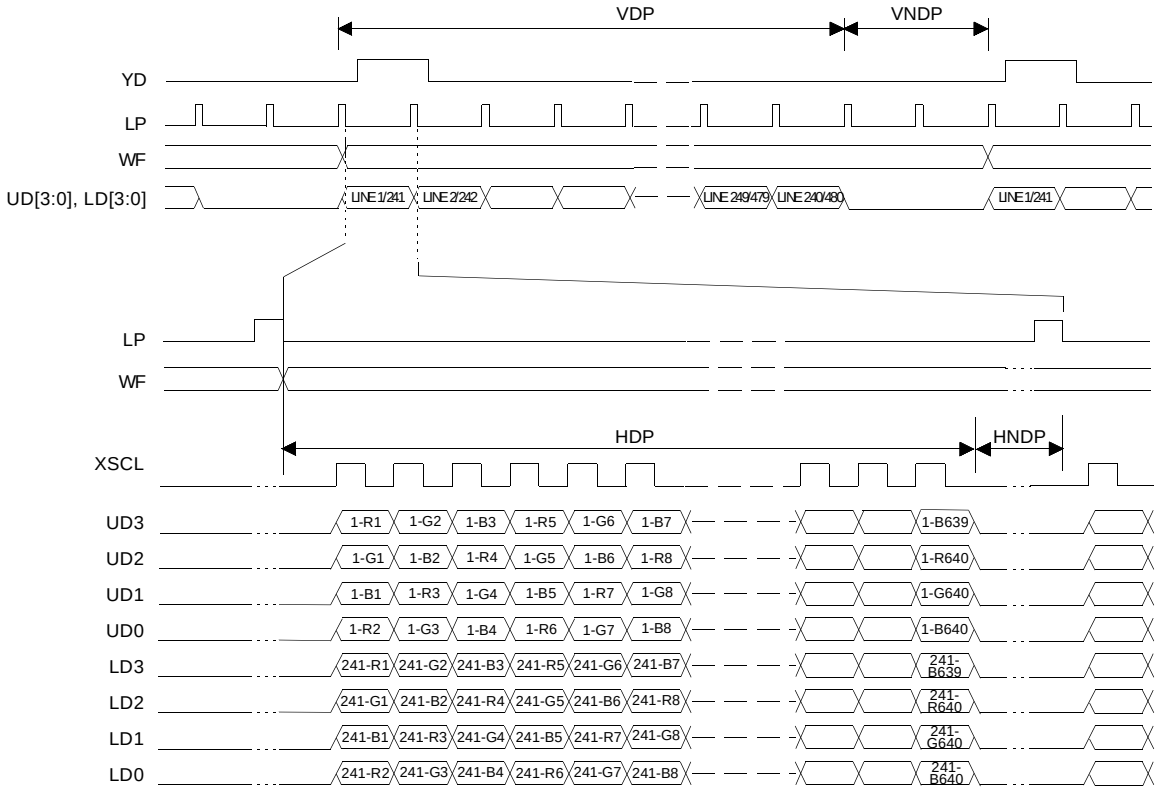


* diagram drawn with 2 LD vertical blank period
Example timing for a 640 x 480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

8-Bit Dual Color Panel (One Shift Clock)

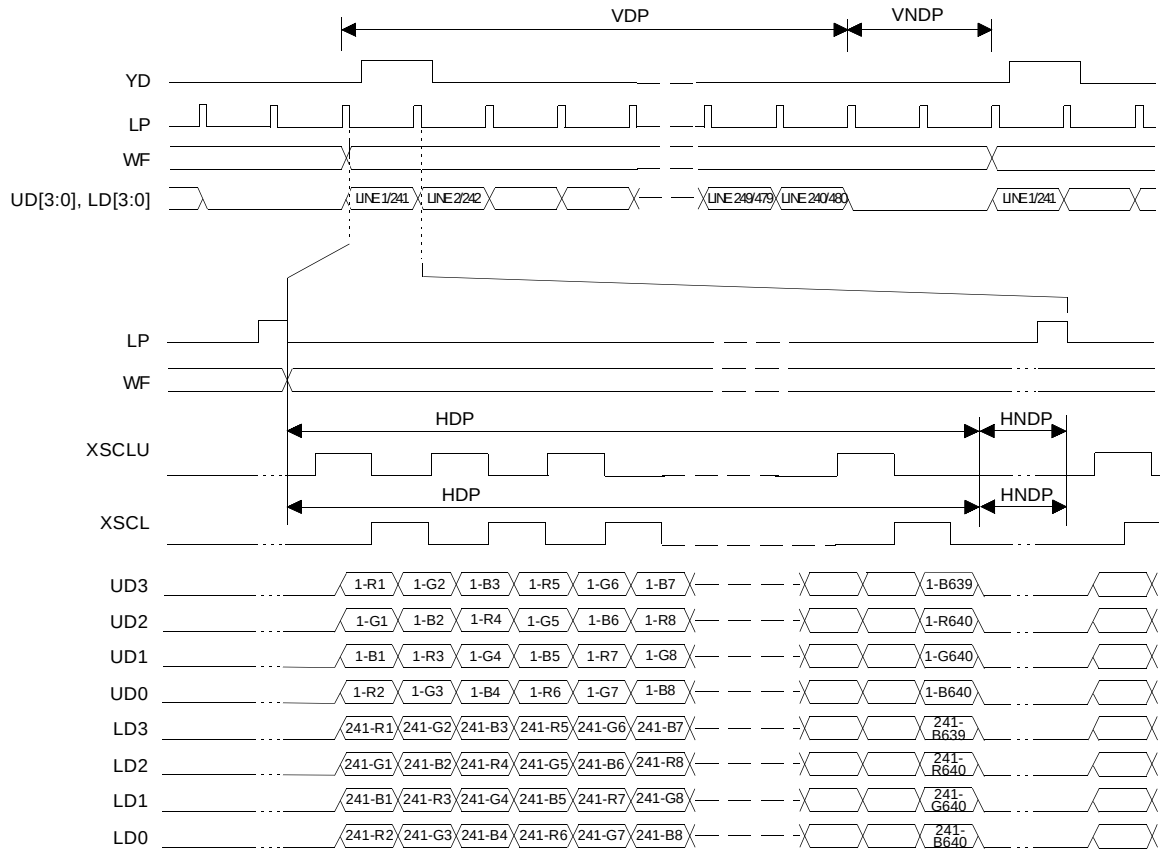


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HD = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

8-Bit Dual Color Panel (Two Shift Clocks)

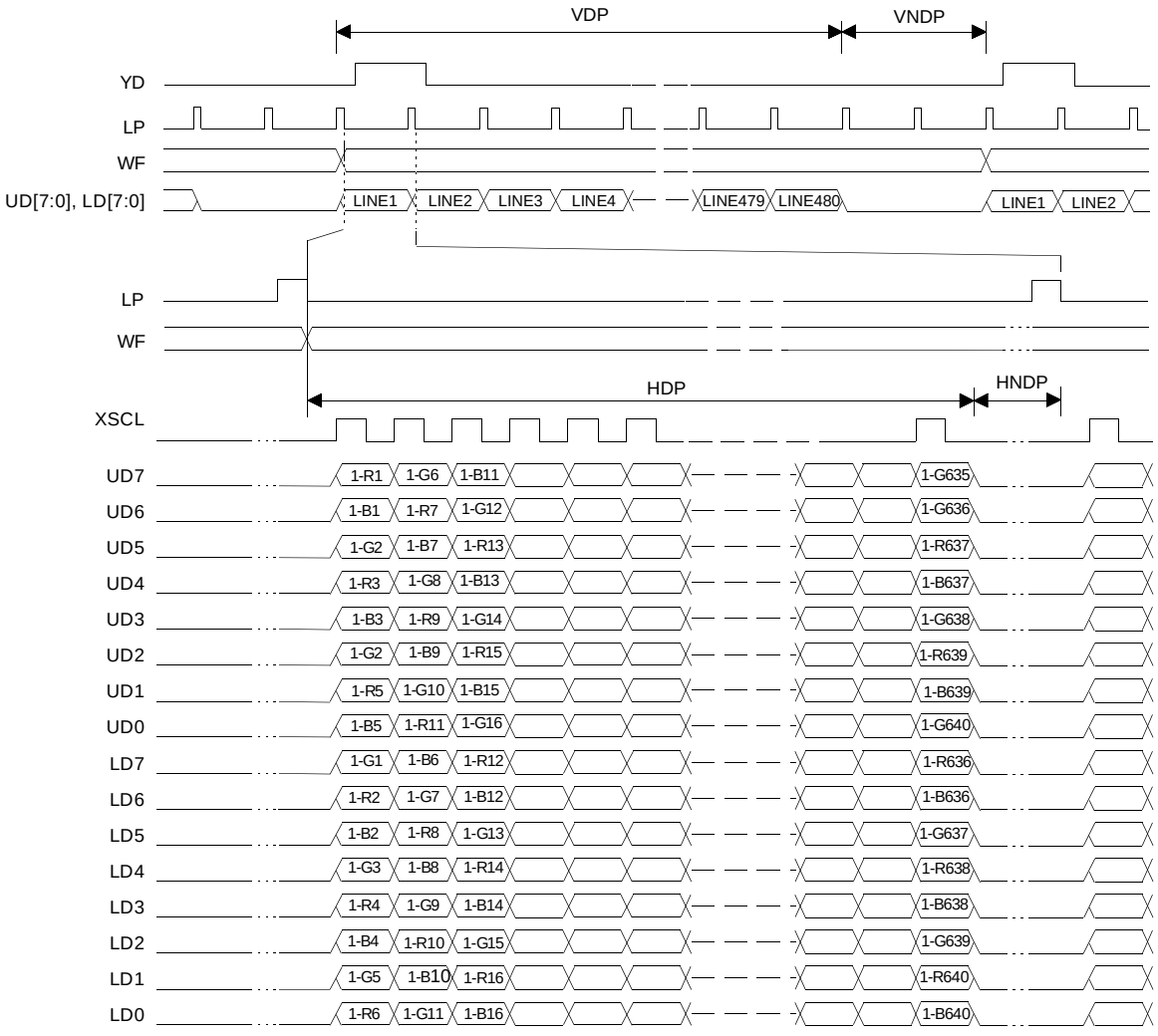


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VND = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

16-Bit Single Color Panel

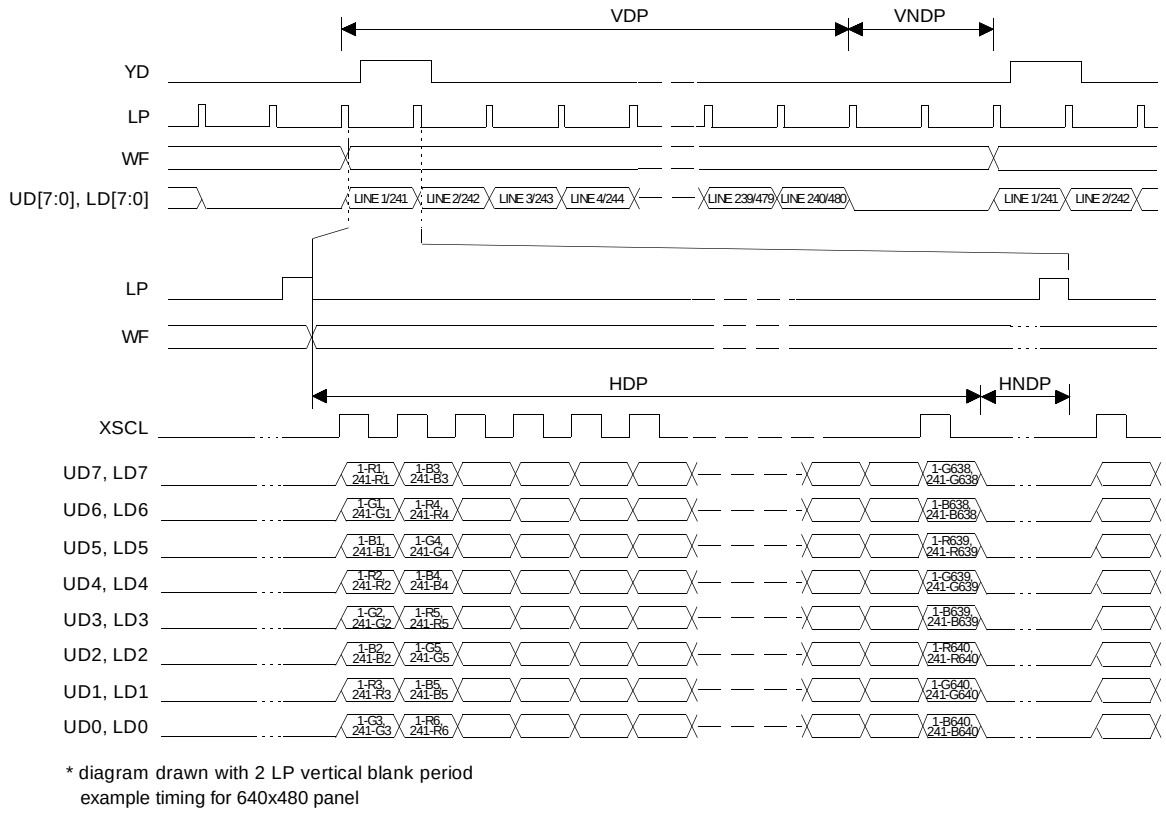


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ COLOR PASSIVE STN LCD PANEL INTERFACE

16-Bit Dual Color Panel

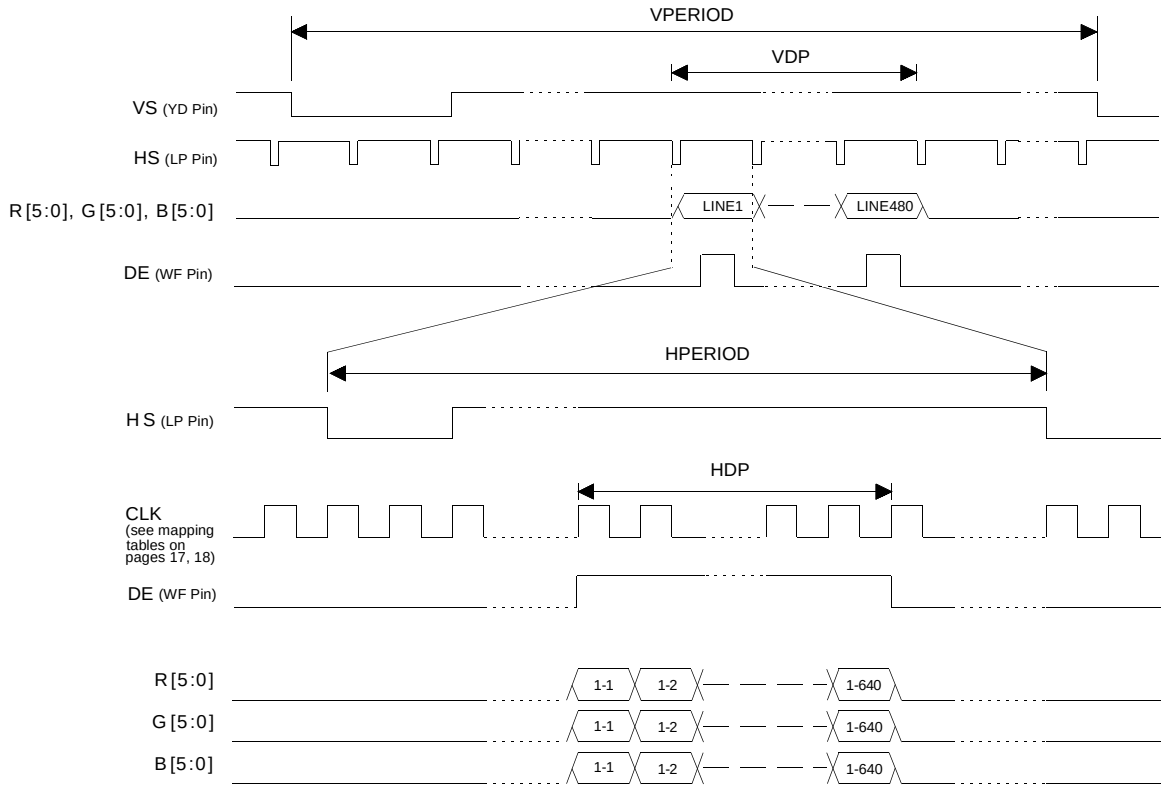


* diagram drawn with 2 LP vertical blank period
example timing for 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ ACTIVE MATRIX LCD PANEL INTERFACE

18-Bit Color TFT

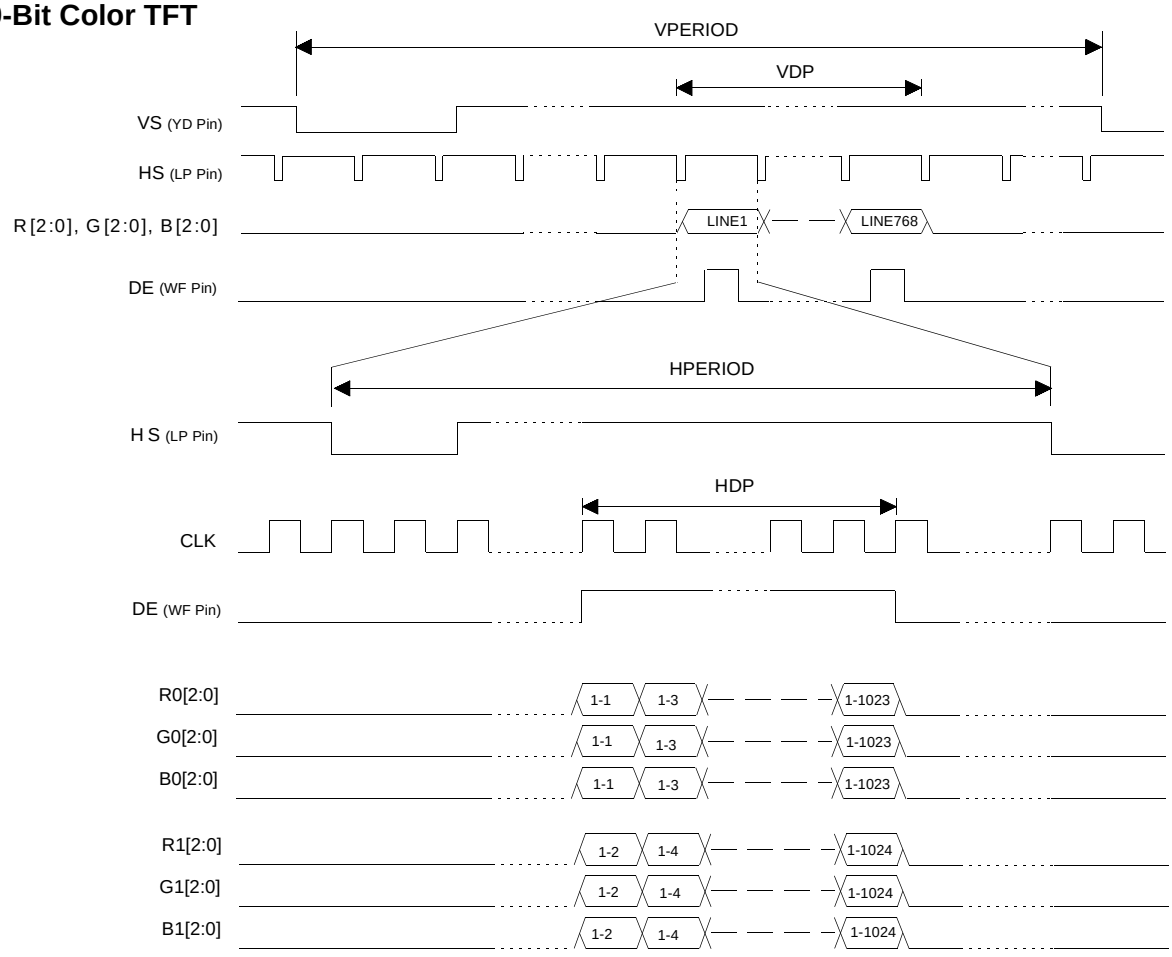


Note: DE (Data Enable) is used to indicate the first pixel
Example Timing for 640 x 480 panel

VPERIOD = Vertical Display Period
VDP = Vertical Display Period
HPERIOD = Horizontal Period
HDP = Horizontal Display Period

■ ACTIVE MATRIX LCD PANEL INTERFACE

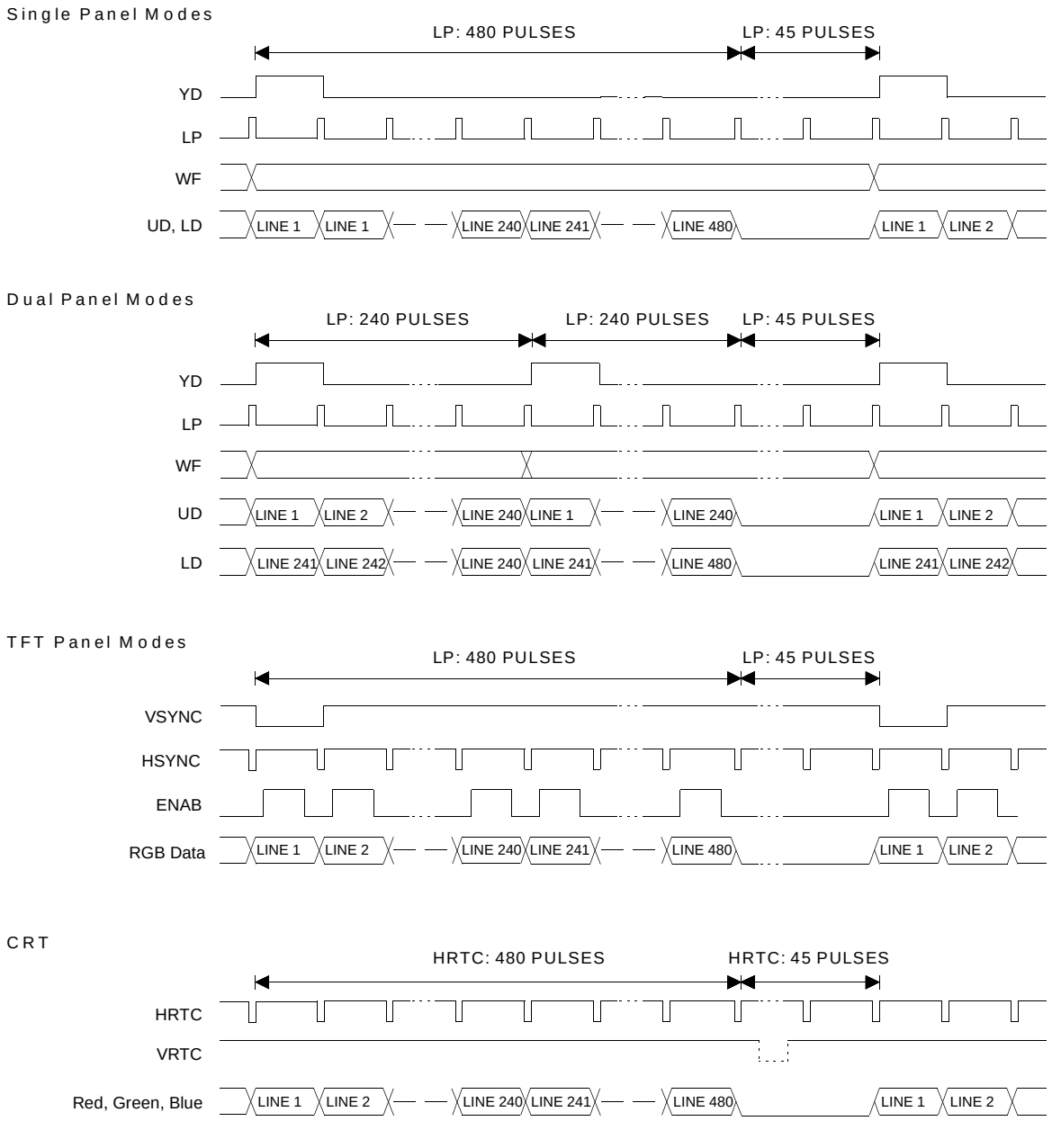
2 X 9-Bit Color TFT



Note: DE (Data Enable) is used to indicate the first pixel
example timing for 1024x768 panel

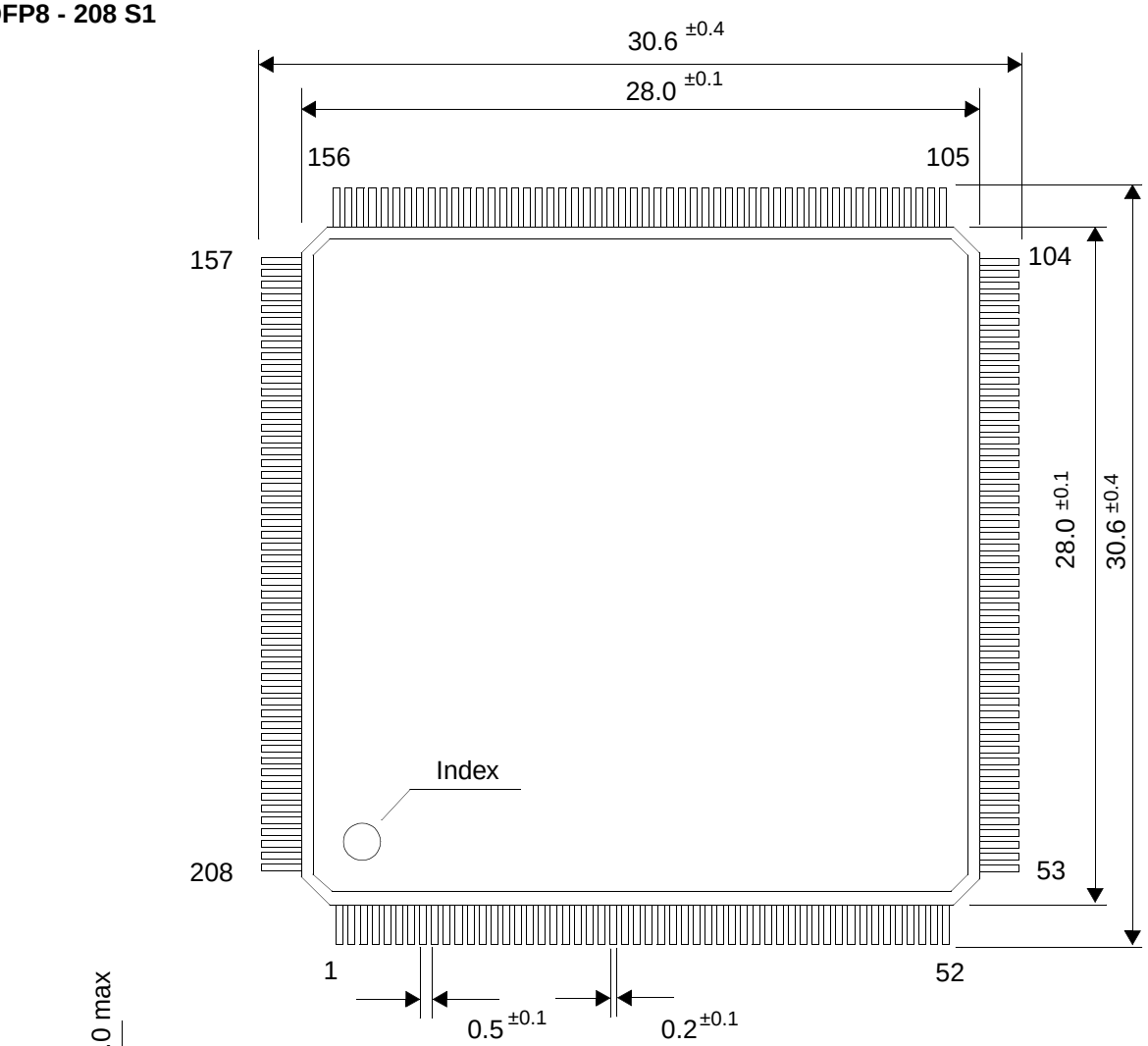
VPERIOD = Vertical Display Period
VDP = Vertical Display Period
HPERIOD = Horizontal Period
HDP = Horizontal Display Period

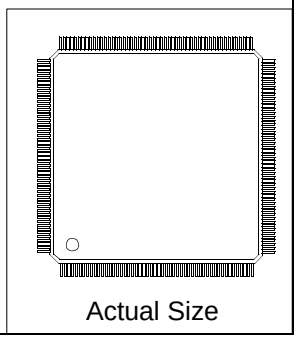
■ SIMULTANEOUS DISPLAY INTERFACE



■ PACKAGE DIMENSIONS

QFP8 - 208 S1 **Unit: mm**





■ COMPREHENSIVE SUPPORT TOOLS

Seiko Epson provides the designer and manufacturer a complete set of resources and tools for the development of LCD Graphics Systems.

Documentation

- Technical manuals
- Evaluation/Demonstration board manual

Evaluation/Demonstration Board

- Assembled and fully tested Graphics Evaluation/Demonstration board
- Schematic of Evaluation/Demonstration board
- Parts List
- Installation Guide
- CPU Independent Software Utilities
- Evaluation Software
- Windows CE Display Driver

■ Application Engineering Support

Seiko Epson offers the following services through their Sales and Marketing Network:

- Sales Technical Support
- Customer Training
- Design Assistance

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS:

- SPC8110 Technical Manual
- SDU8110 Evaluation Boards
- Windows® CE Display Driver
- CPU Independent Software Utilities

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