DATA SHEET

凌陽科技
SUNPLUS

SPC41B1

40KB Sound Controller

SEP. 04, 2001

Version 1.3

Table of Contents

PAGE

1. GENERAL DESCRIPTION 3

2. BLOCK DIAGRAM 3

3. FEATURES 3

4. APPLICATION FIELD 3

5. SIGNAL DESCRIPTIONS* 4

6. FUNCTIONAL DESCRIPTIONS 5

6.1. CPU 5

6.2. ROM AREA 5

6.3. RAM AREA 5

6.4. MAP OF MEMORY AND I/OS 5

6.5. I/O PORT CONFIGURATION* 5

6.6. POWER SAVINGS MODE 6

6.7. LOW VOLTAGE RESET 6

6.8. TIMER/COUNTER 7

6.9. SPEECH AND MELODY 7

7. ELECTRICAL SPECIFICATIONS 8

7.1. ABSOLUTE MAXIMUM RATINGS 8

7.2. AC CHARACTERISTICS (T_A = 25℃) 8

7.3. DC CHARACTERISTICS (VDD = 3.0V, T_A = 25℃) 8

7.4. DC CHARACTERISTICS (VDD = 5.0V, T_A = 25℃) 8

7.5. THE RELATIONSHIP BETWEEN THE R_{OSC} AND THE F_{CPU} 9

8. APPLICATION CIRCUITS 10

8.1. APPLICATION CIRCUIT 10

8.2. CURRENT MODE DAC SPEAKER DRIVER 11

9. PACKAGE/PAD LOCATIONS 12

9.1. PAD ASSIGNMENT 12

9.2. ORDERING INFORMATION 12

9.3. PAD LOCATIONS 13

10. DISCLAIMER 14

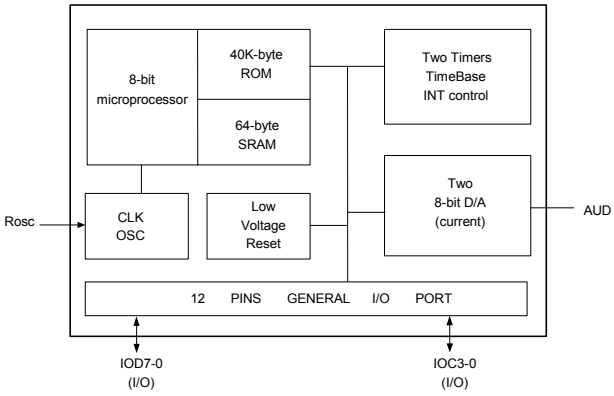
11. REVISION HISTORY 15

40KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC41B1 is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 40K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 13 sec speech duration @ 6KHz sampling rate) and 64-byte working SRAM. It includes two Timer/Counters, 12 Software Selectable I/Os, and one 8-bit current output (D/A). For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V and includes Low Voltage Reset function. The Low Voltage Reset automatically resets when the working voltage is less than 2.2V. In addition, SPC41B1 has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPC41B1 includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- **Provides 40K-byte ROM for program and audio data**
- **64-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- **Supports R_{osc} only**
- Max. CPU clock: 4.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 12 general I/Os**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- **Approx. 13 sec speech**
  @ 6KHz sampling rate with 4-bit ADPCM
- **One D/A output**
- **Low Voltage Reset**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	8	I	Supply voltage input
VSS	1, 7	I	Ground
ROSC	9	I	Oscillator input
RESET	2	I	RESET
TEST	11	I	TEST MODE
AUD	10	O	AUDIO OUTPUT
IOC0 IOC1 IOC2 IOC3	6 5 4 3	I/O I/O I/O I/O	Port C is a 4-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer or Open-drain NMOS type (sink current). IOC1: EXT INT IN IOC2: EXT COUNT IN **See note 1 and 2 below.
IOD0 IOD1 IOD2 IOD3 IOD4 IOD5 IOD6 IOD7	19 18 17 16 15 14 13 12	I/O I/O I/O I/O I/O I/O I/O I/O	Port D is an 8-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS type (send current). (Key change, Wake up I/O) **See note 1 and 2 below.

* Refer to SPC Programming Guide for complete information.

Note: 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), Open Drain NMOS output (sink).

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit microprocessor of SPC41B1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC41B1 is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. ROM AREA

The SPC41B1 provides a 40K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.3. RAM AREA

The SPC41B1 total RAM consists of 64 bytes (including Stack) at locations from $C0 through $FF.

6.4. Map of Memory and I/Os

*I/O PORT:

– PORT IOC $0004
IOD $0005
– I/O CONFIG $0000
$0001

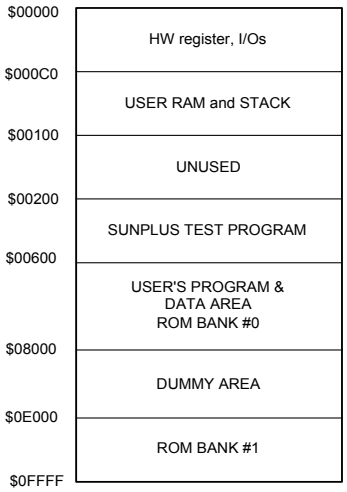
*NMI SOURCE:

– INTA (from TIMER A)

*INT SOURCE:

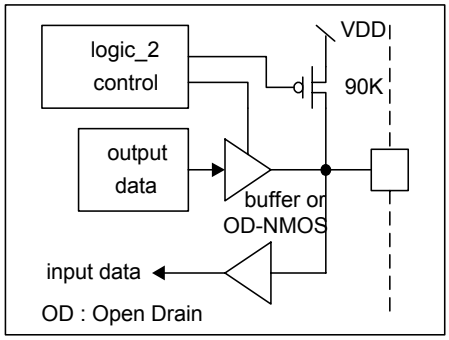
– INTA (from TIMER A)
– INTB (from TIMER B)
– CPU CLK / 1024
– CPU CLK / 8192
– CPU CLK / 65536
– EXT INT

*MEMORY MAP (From ROM view)

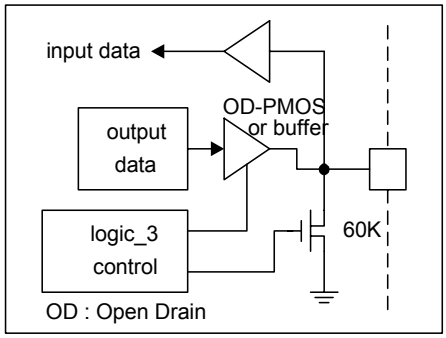


6.5. I/O Port Configuration*

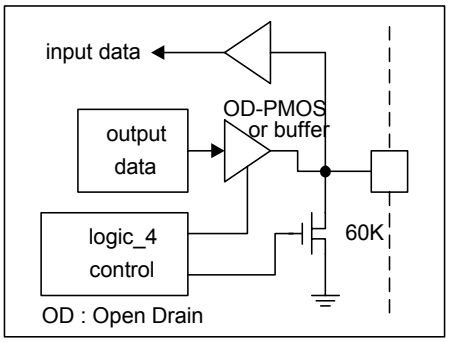
Input/Output IOC port : IOC3 - 0



Input/Output IOD port : IOD3 - 0



Input/Output IOD port : IOD7 - 4



* Values shown are for VDD = 5.0V test conditions only.

6.6. Power Savings Mode

The SPC41B1 provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the SPC41B1. After the SPC41B1 is awakened, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (See FIG.1).

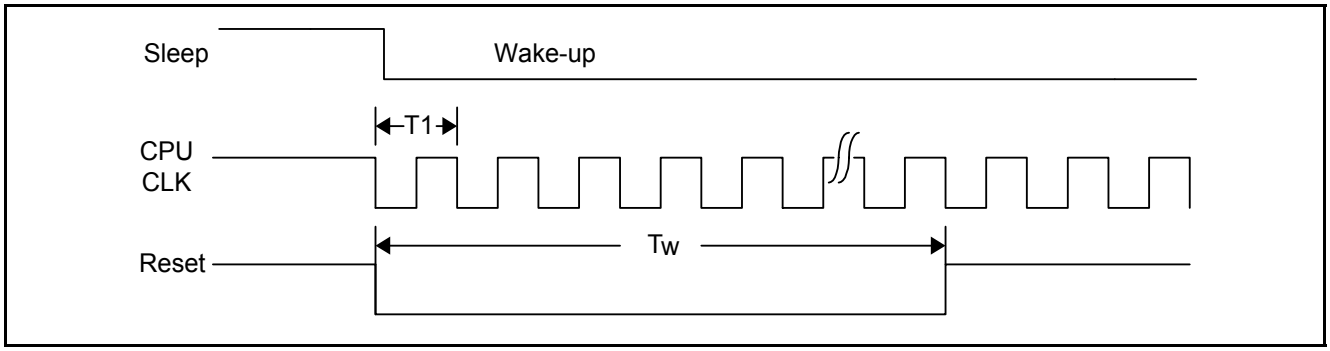
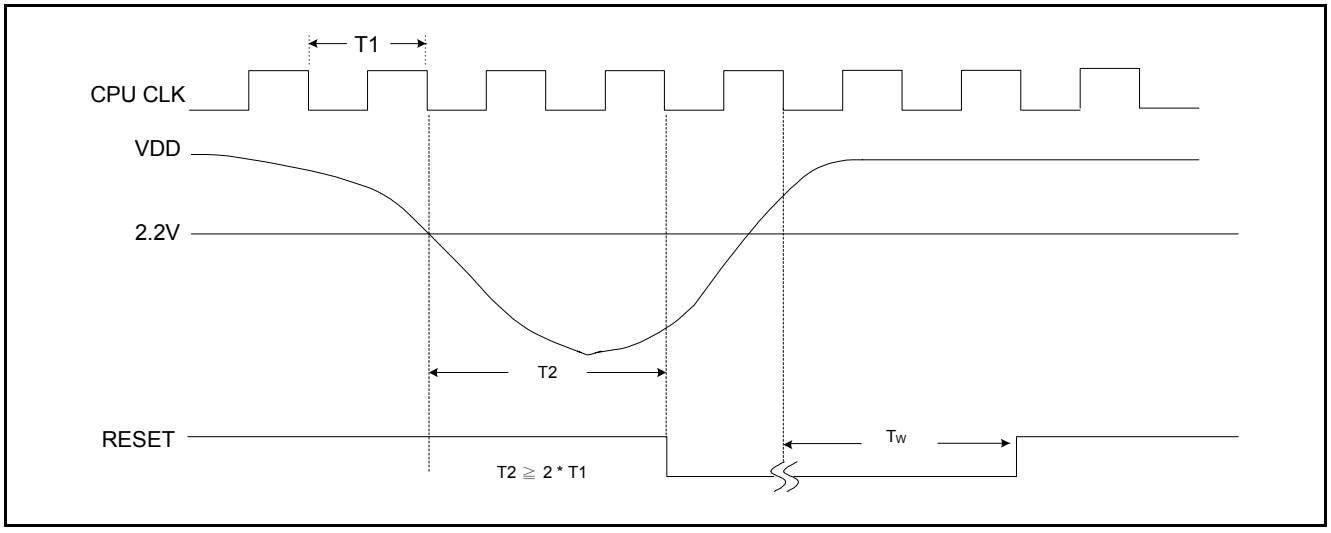


FIG. 1

$T1 = 1 / (F_{CPU})$, Tw ≧ 65536 x T1

6.7. Low Voltage Reset

The SPC41B1 includes a Low Voltage Reset (LVR) function. Below the minimum power-supply voltage of 2.2V, the CPU system will become unstable and malfunction. Low Voltage Reset will reset all functions into the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V (FIG.2).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

6.8. Timer/Counter

The SPC41B1 contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time. The read instruction will not affect the value of the counter or reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.9. Speech and Melody

Since the SPC41B1 provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the SPC41B1 can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPC41B1 provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

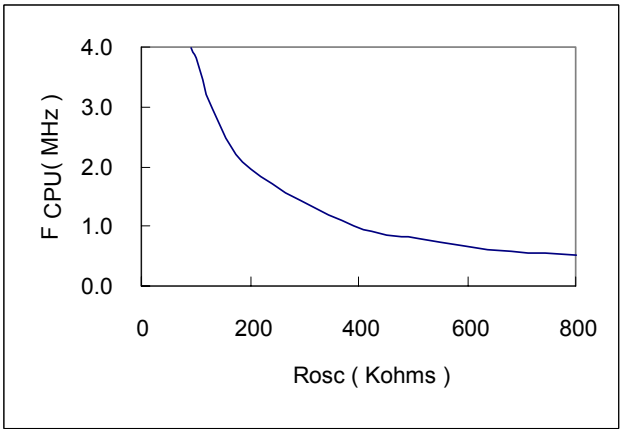
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (IOC, IOD)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (IOC, IOD)	I_{OL}	2.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Input Resistor (IOD)	R_{IN}	-	120	-	Kohm	Pull Low, VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

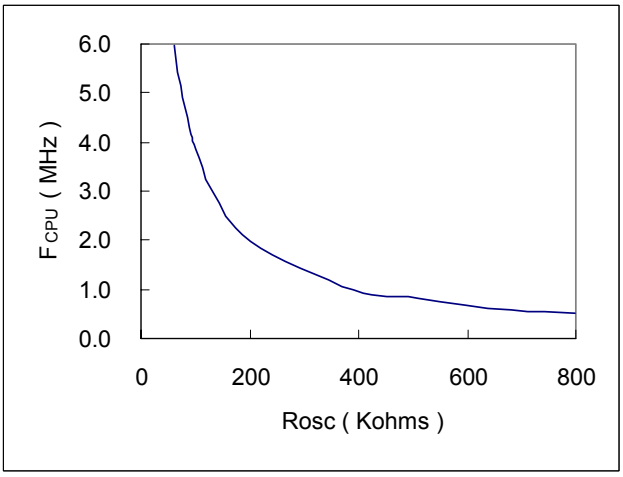
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I (IOC, IOD)	I_{OH}	-1.0	-	-	mA	VDD = 5.0V, V_{OH} = 4.2V
Output Sink I (IOC, IOD)	I_{OL}	4.0	-	-	mA	VDD = 5.0V, V_{OL} = 0.8V
Input Resistor (IOD)	R_{IN}	-	60	-	Kohm	Pull Low, VDD = 5.0V

7.5. The Relationship between the R_{OSC} and the F_{CPU}

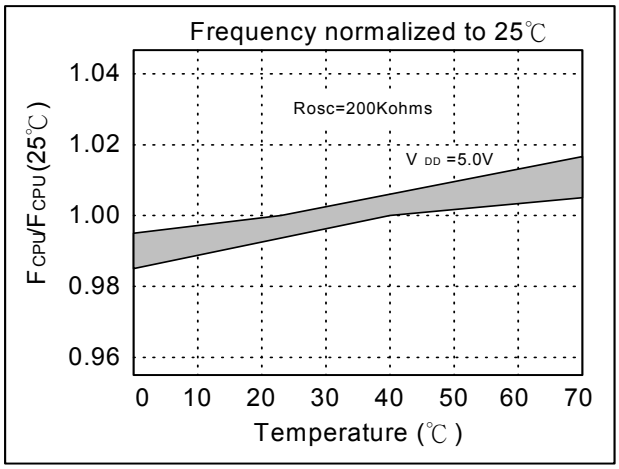
7.5.1. VDD = 3.0V, T_A = 25℃



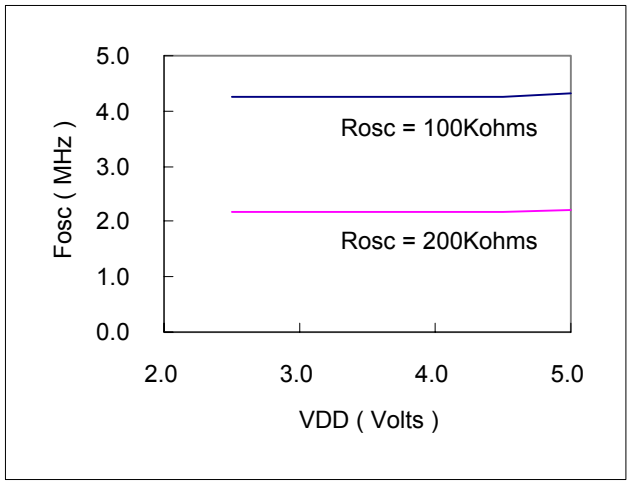
7.5.2. VDD = 4.5V , T_A = 25℃



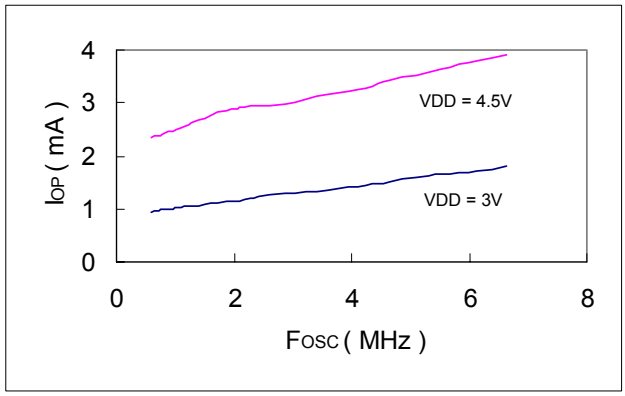
7.5.3. Frequency vs. temperature



7.5.4. Frequency vs. VDD

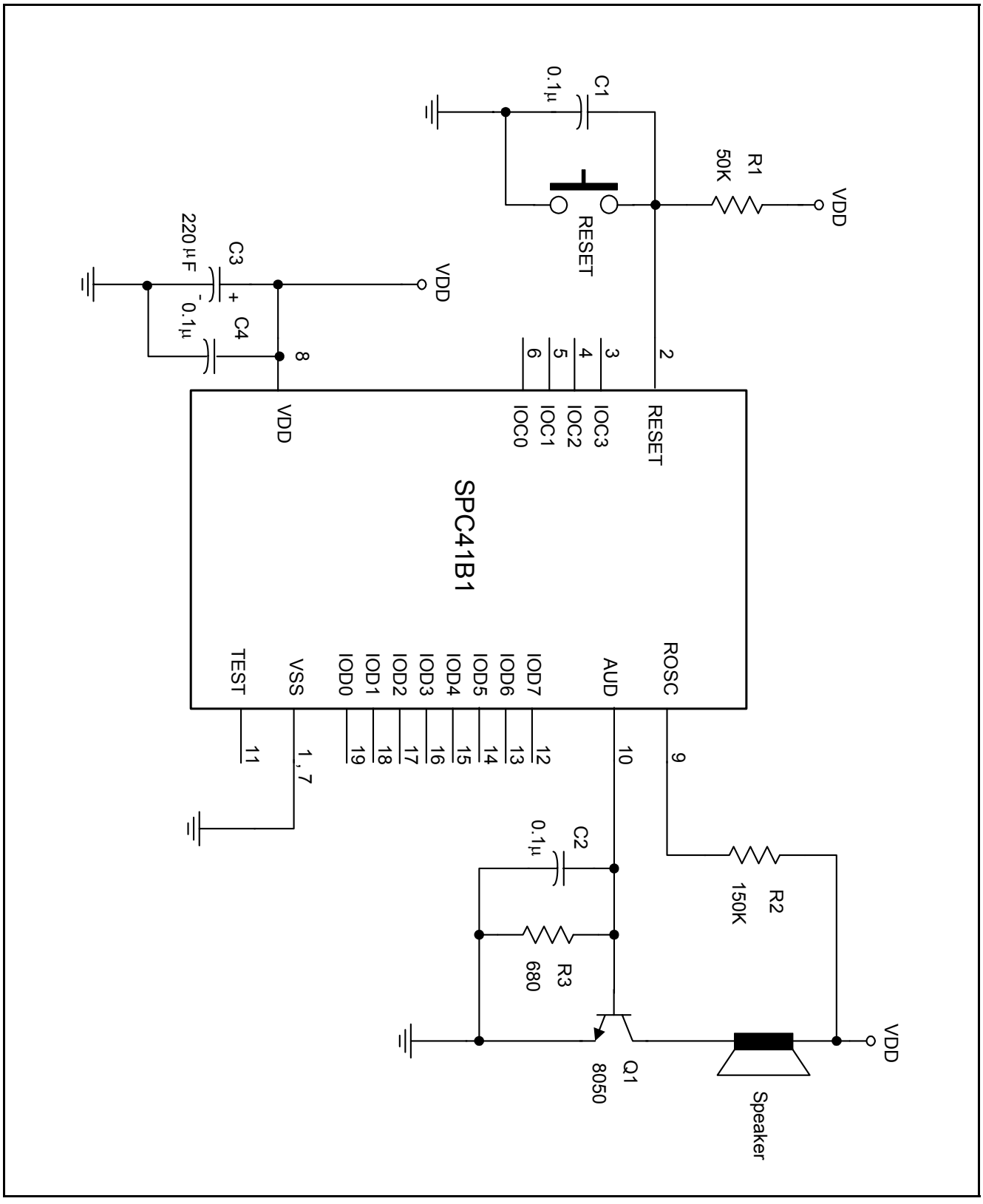


7.5.5. Operating current vs. frequency vs. VDD



8. APPLICATION CIRCUITS

8.1. Application Circuit



8.2. Current Mode DAC Speaker Driver

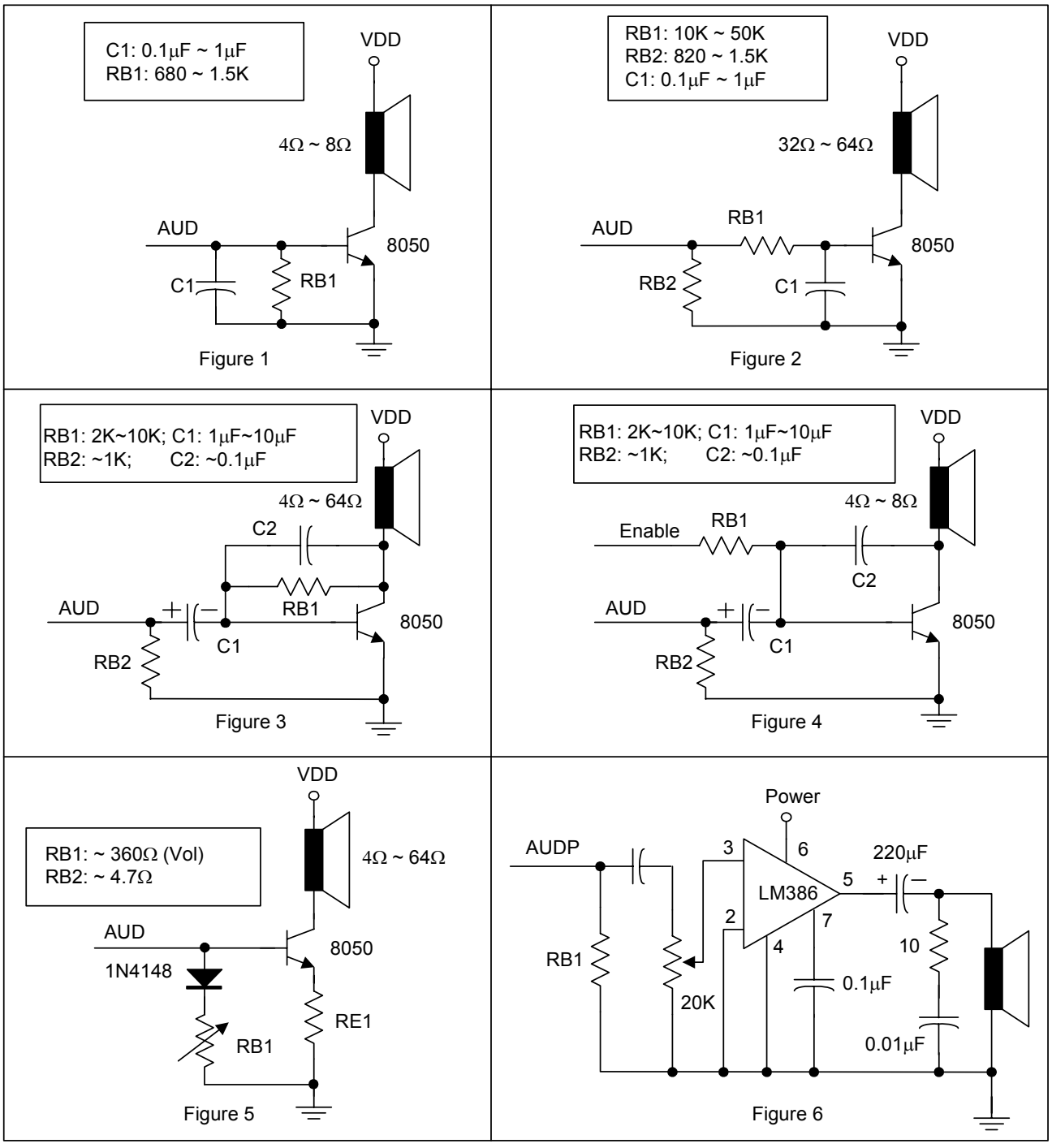
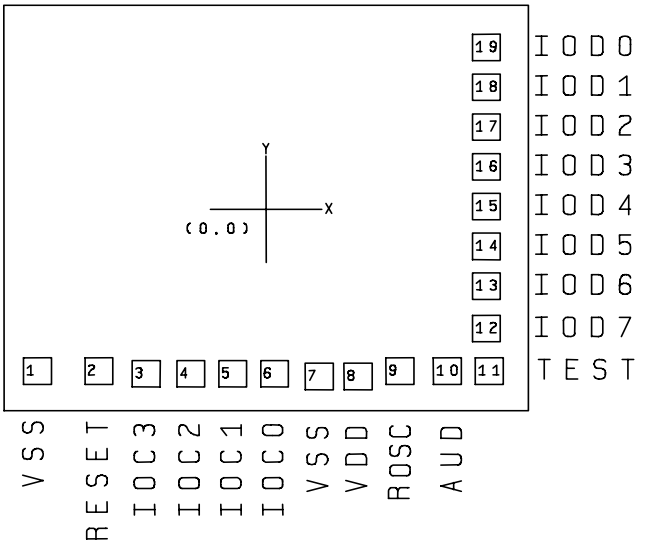


Figure 1: The simplest CKT uses with low impedance speaker. It has high operation current, but the cost is the cheapest.
Figure 2: It is the same as Figure 1 but a high impedance speaker is used.
Figure 3: The CKT contains a low pass filter. It is capable to provide higher speech quality, but it always takes higher operation current.
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.
Figure 5: The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.
Figure 6: High quality, low operation current CKT, but more expensive.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 2000μm x 1660μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure IC function properly, please bond all of the VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC41B1-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	VSS	-819	-615
2	RESET	-601	-615
3	IOC3	-429	-625
4	IOC2	-273	-625
5	IOC1	-122	-625
6	IOC0	33	-625
7	VSS	189	-630
8	VDD	329	-630
9	ROSC	485	-615
10	AUD	651	-615
11	TEST	803	-615
12	IOD7	786	-450
13	IOD6	786	-297
14	IOD5	786	-149
15	IOD4	786	4
16	IOD3	786	151
17	IOD2	786	304
18	IOD1	786	452
19	IOD0	786	605

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

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11. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 06, 1998	0.1	Original	
MAY. 13, 1998	0.2	Add "Note2: To ensure IC function properly, please bond all of the VDD and VSS pins."	
MAY. 21, 1998	0.3	Add, Low voltage reset function description	
JUN. 02, 1998	0.4	1. Revise the grammars and spelling in "*GENERAL DESCRIPTION*", "*FEATURES*", "*BLOCK DIAGRAM*", "*FUNCTIONAL DESCRIPTIONS*", "*TIMER/COUNTER*", "*SPEECH AND MELODY*", and "*APPLICATION CIRCUITS*" 2. Describe there are two D/As in the (only one) audio current output in "*GENERAL DESCRIPTION*"	
JUN. 10, 1998	0.5	1. Delete "The average instruction cycle is around 2.5 clock cycles. It means the 4MHz clock can offer approxinately 750ns per instruction cycle. 2. Delete "(minimun.)" in the "*FEATURES*"	
OCT. 19, 1998	1.0	Delete "*PRELIMINARY*"	
NOV. 04, 1999	1.1	Renew to a new document format	
OCT. 30, 2000	1.2	1. Feature: 13 sec. Speech @ 6KHz sampling rates with 4-bit ADPCM 2. Block Diagram: Two 8-bit D/A (current) - one AUD output pin	
SEP. 04, 2001	1.3	1. Correct chip size 2. Add Note1 and Note3 in the "*9.1 PAD Assignment*" 3. Renew to a new document format	12 12