DATA SHEET

凌陽科技
SUNPLUS

SPC41A

40KB Sound Controller

SEP. 04, 2001

Version 1.8

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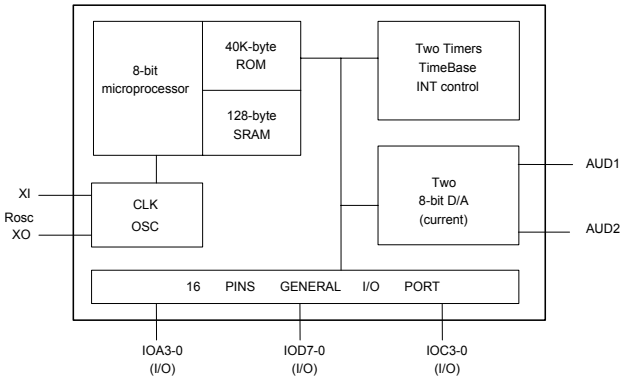
40KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC41A is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 40K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 13 sec speech duration @ 6KHz sampling rate) and 128-byte working SRAM. It includes two Timer/Counters, 16 Software Selectable I/Os, and two 8-bit current outputs (D/A). For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V. In addition, the SPC41A has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPC41A includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- **Provides 40K-byte ROM for program and audio data**
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports Crystal Resonator or Rosc (with Mask option)
- Max. CPU clock: 4.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 16 general I/Os**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake -up function
- **Approx. 13 sec speech**
  @ 6KHz sampling rate with 4-bit ADPCM
- **Two 8-bit current outputs(D/A)**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS**

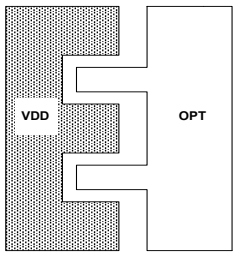
Mnemonic	PIN No.	Type	Description
VDD	12	I	POWER VDD
VSS	5, 11	I	POWER VSS
XI	15	I	CRYSTAL OSC IN or RESISTOR
XO	14	O	CRYSTAL OSC OUT
OPT*	13	I	Rosc OPTION connect to VDD
TEST	18	I	TEST MODE
RESET	6	I	RESET
AUD1 AUD2	16 17	O	AUDIO OUTPUT
IOA0 IOA1 IOA2 IOA3	4 3 2 1	I/O I/O I/O I/O	Port A is a 4-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A can be either Buffer or Open-drain NMOS types (Sink current). ***See note 1 and 2 below.
IOC0 IOC1 IOC2 IOC3	10 9 8 7	I/O I/O I/O I/O	Port C is a 4-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer type or Open-drain NMOS type (sink current). IOC1: EXT INT IN IOC2: EXT COUNT IN ***See note 1 and 2 below.
IOD0 IOD1 IOD2 IOD3 IOD4 IOD5 IOD6 IOD7	26 25 24 23 22 21 20 19	I/O I/O I/O I/O I/O I/O I/O I/O	Port D is an 8-bit bi-directional programmable Input/Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS type (send current). (Key change, Wake up I/O) ***See note 1 and 2 below.

* OPT is the selection pin for ROSC or X'TAL using the bonding option. The shape looks like the figure at the right. When ROSC is selected, OPT is connected to VDD. If X'TAL is selected, OPT is floating. The reason OPT is near VDD is that when ROSC is selected, it is easy to make the connection between VDD and OPT.

** Refer to SPC Programming Guide for complete information.

*** **Note:** 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output <sink>.



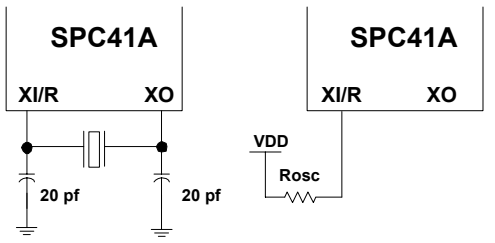
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit microprocessor of SPC41A is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC41A is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. Oscillator

The SPC41A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by using the bonding option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



(a) Crystal or Ceramic Resonator Connections

(b) RC Oscillator Connections

6.3. Bonding Option

The SPC41A has the following bonding option:

- Supports Crystal Resonator or Rosc (with bonding option).

6.4. ROM Area

The SPC41A provides a 40K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.5. RAM Area

The SPC41A total RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

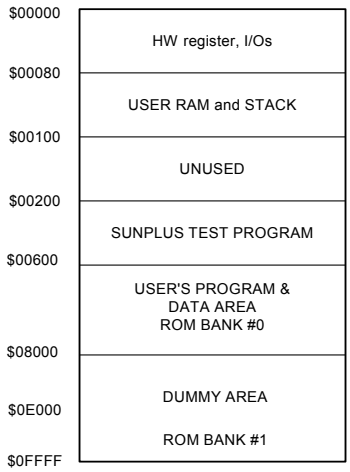
6.6. Map of Memory and I/Os

*I/O PORT:
- PORT IOA $0002
  IOC $0004
  IOD $0005
- I/O CONFIG $0000
  $0001

*NMI SOURCE:
- INTA (from TIMER A)

*INT SOURCE:
- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

*MEMORY MAP (From ROM view)



6.7. Speech and Melody

Since the SPC41A provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the SPC41A can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPC41A provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

6.8. Power Savings Mode

The SPC41A provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the SPC41A. After the SPC41A is awakened, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (FIG.1).

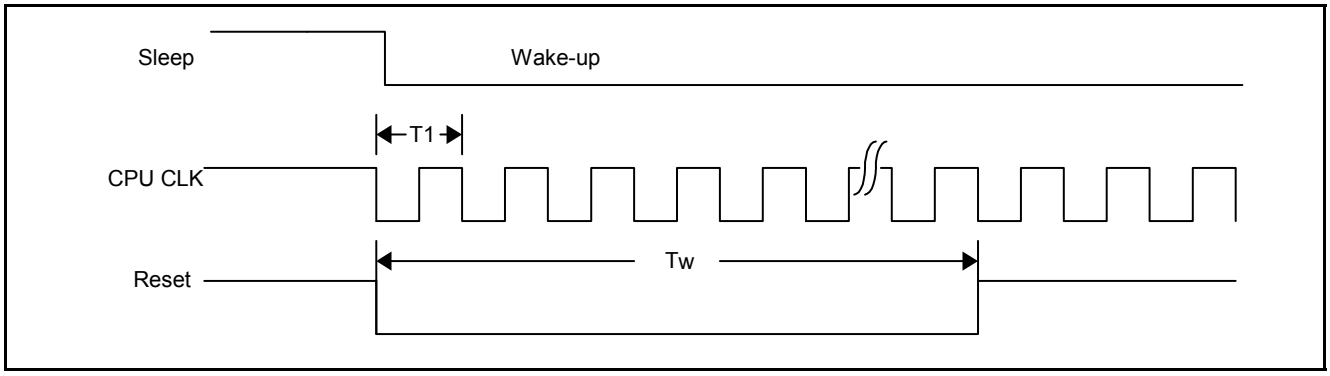
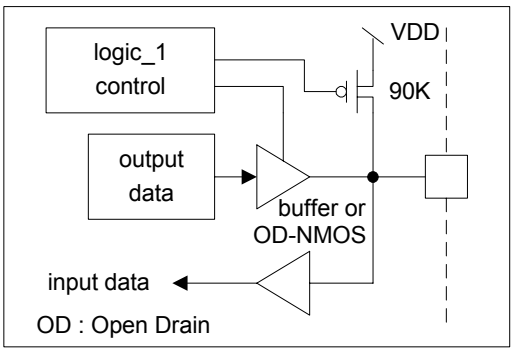


FIG. 1

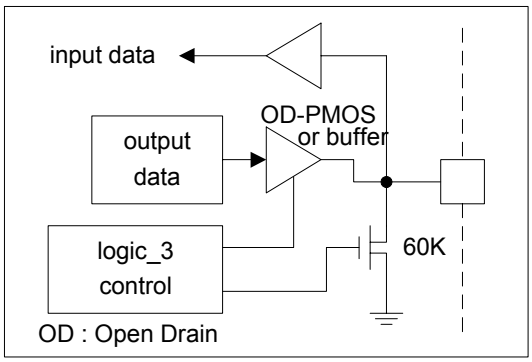
T1 = 1 / (F_{CPU}), Tw ≧65536 x T1

6.9. I/O Port Configuration

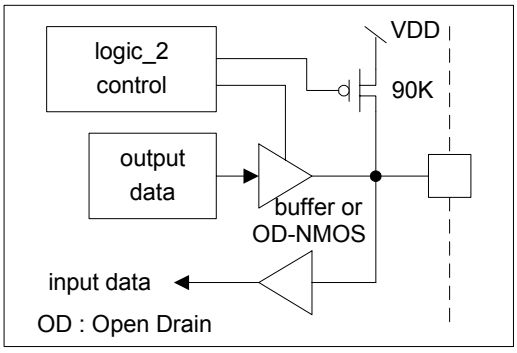
Input/Output IOA port : IOA3 - 0



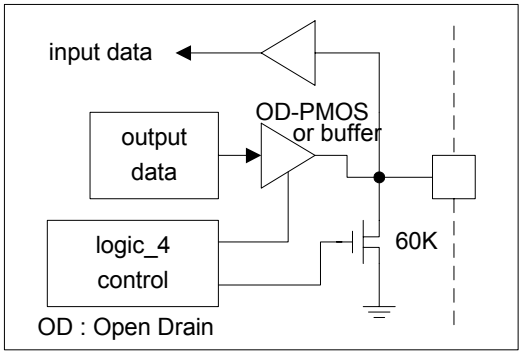
Input/Output IOD port : IOD3 - 0



Input/Output IOC port : IOC3 - 0



Input/Output IOD port : IOD7 - 4



*Values shown are for VDD = 5.0V test conditions only.

6.10. Timer/Counter

The SPC41A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time. The read instruction will not affect the value of the counter or reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
CPU Clock	F_{CPU}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

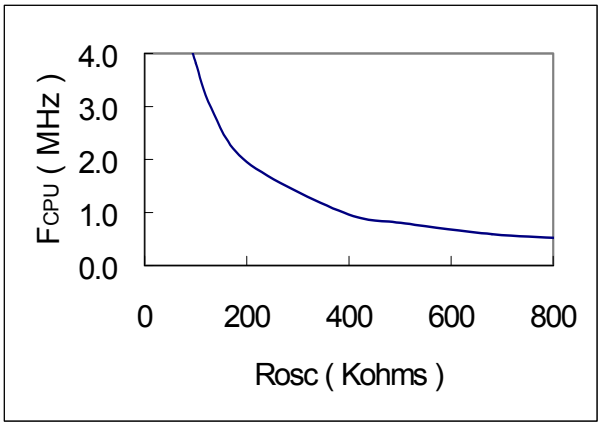
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I IOA, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink I IOA, IOC, IOD	I_{OL}	2.0	-	-	mA	VDD = 3.0V V_{OL} = 0.8V
Input Resistor IOD	R_{IN}	-	100	-	Kohm	Pull Low VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

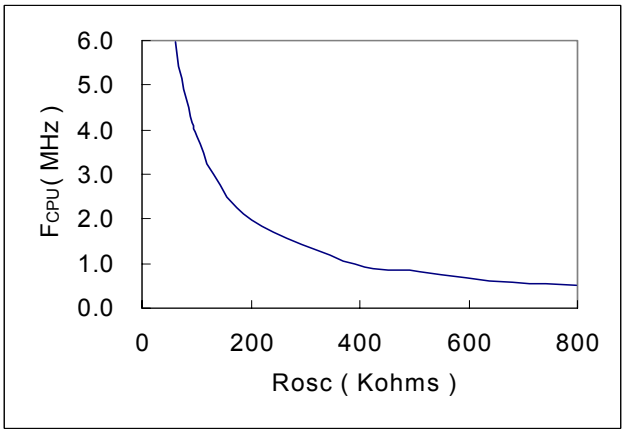
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I IOA, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5.0V V_{OH} = 4.2V
Output Sink I IOA, IOC, IOD	I_{OL}	4.0	-	-	mA	VDD = 5.0V V_{OL} = 0.8V
Input Resistor IOD	R_{IN}	-	60	-	Kohm	Pull Low VDD = 5.0V

7.5. The Relationship between the R_{OSC} and the F_{CPU}

7.5.1. VDD = 3.0V, T_A = 25℃

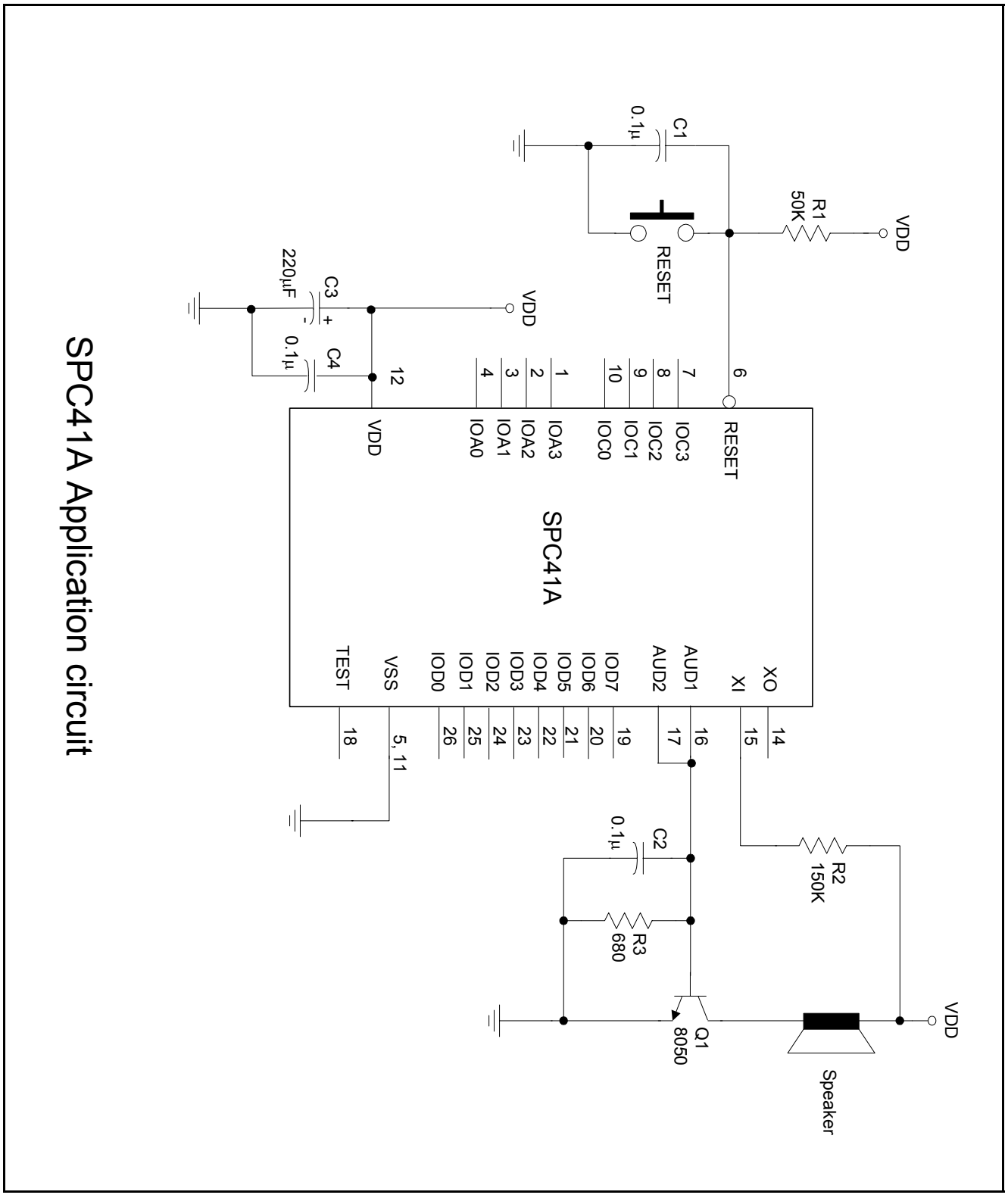


7.5.2. VDD = 4.5V, T_A = 25℃

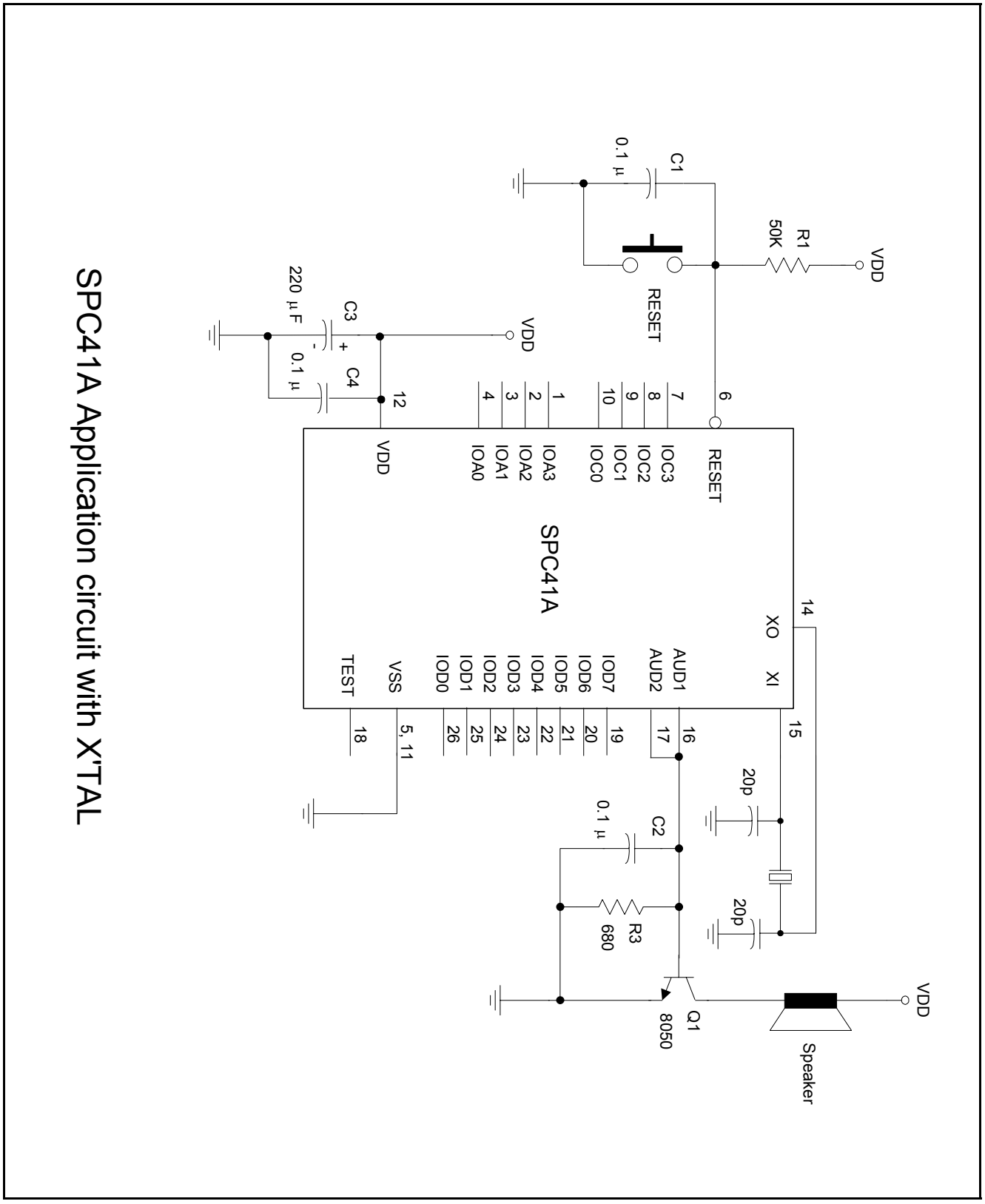


8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)



8.2. Application Circuit - (2)



8.3. Current Mode DAC Speaker Driver

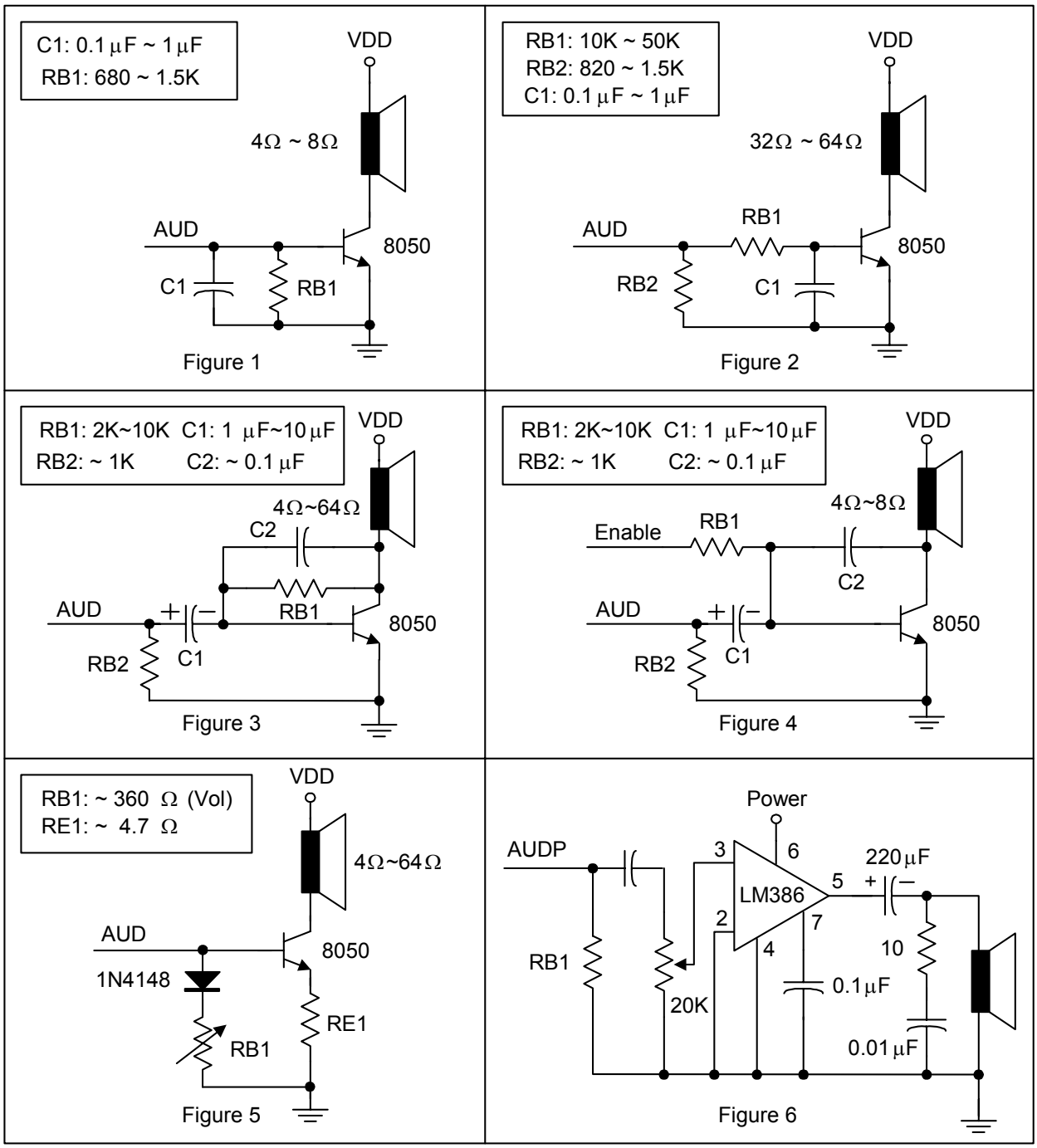
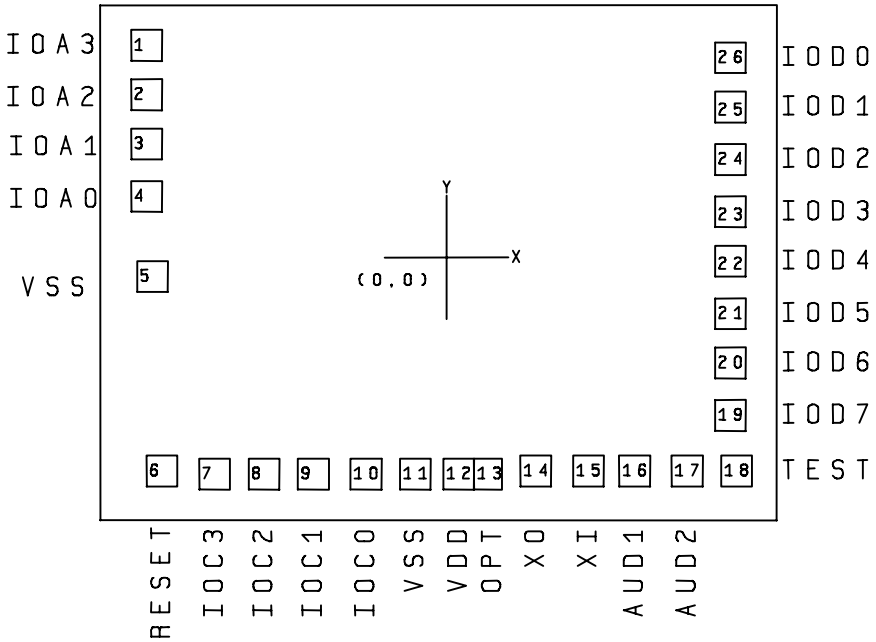


Figure 1:The simplest CKT uses a low impedance speaker. It has high operation current, but lowest cost.
Figure 2: It is the same as Figure 1 but a high impedance speaker is used.
Figure 3: The CKT contains a low pass filter. It is capable of providing higher speech quality, but it always takes higher operation current.
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.
Figure 5: The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.
Figure 6: High quality, low operation current CKT, but more expensive.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip size: 2290μm x 1820μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC function properly, bond all VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC41A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	IOA3	-948	708
2	IOA2	-948	547
3	IOA1	-948	382
4	IOA0	-948	220
5	VSS	-934	-29
6	RESET	-896	-676
7	IOC3	-729	-688
8	IOC2	-564	-688
9	IOC1	-402	-688
10	IOC0	-237	-688
11	VSS	-76	-688
12	VDD	64	-688
13	OPT	164	-688
14	XO	319	-676
15	XI	484	-676
16	AUD1	640	-676
17	AUD2	806	-676
18	TEST	961	-676
19	IOD7	946	-491
20	IOD6	946	-322
21	IOD5	946	-160
22	IOD4	946	9
23	IOD3	946	170
24	IOD2	946	340
25	IOD1	946	501
26	IOD0	946	670

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
DEC. 30, 1996	0.1	Original	
MAR. 10, 1997	0.2	1. Add "*BLOCK DIAGRAM*" 2. Add "*PAD LOCATIONS*"	10 12 - 13
MAR. 24, 2997	0.3	Modify Fosc2 (max.) value: 3.0MHz @ 3.0V to 3.58MHz @ 3.0V	6
NOV. 28, 1997	1.0	Delete "*PRELIMINARY*"	
DEC. 05, 1997	1.1	1. Renew to a new document format 2. Add "The Relationship between the R_{OSC} and the F_{CPU}"	
MAY. 13, 1998	1.2	Add "Note2: To ensure that the IC function properly, bond all VDD and VSS pins."	
JUN. 02, 1998	1.3	Revise the grammars and spelling in "*GENERAL DESCRIPTION*", "*FEATURES*", "*FUNCTIONAL DESCRIPTIONS*", "*TIMER/COUNTER*", "*SPEECH AND MELODY*", and "*APPLICATION CIRCUITS*"	
JUN. 09, 1998	1.4	1. Delete "The average instruction cycle is around 2.5 clock cycles. It means the 4MHz clock can offer approxinately 750ns per instruction cycle. 2. Delete "(minimun.)" in the "*FEATURES*" 3. Add OPT pin description in the "SIGNAL DESCRIPTIONS"	
NOV. 04, 1999	1.5	Renew to a new document format	
FEB. 22, 2000	1.6	Modify VDD/OPT (Rosc) to VDD in the "*APPLICATION CIRCUITS*"	
NOV. 08, 2000	1.7	1. VDD = 2.4V - 3.6V for 2-battery application. 2. Speech duration @ 6KHz sampling rates with 4-bit ADPCM. 3. Approx. 13 sec. speech.	
SEP. 04, 2001	1.8	1. Correct chip size 2. Add Note1 and Note3 in the "*9.1 PAD Assignment*" 3. Renew to a new document format	13 13