DATA SHEET

凌陽科技
SUNPLUS

SPC122A

Sound Controller with 128KB Flash Memory

Preliminary

SEP. 07, 2001

Version 0.9

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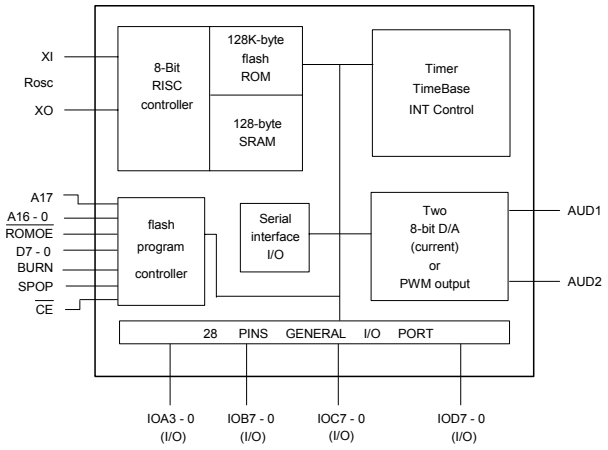
SOUND CONTROLLER WITH 128KB FLASH MEMORY

1. GENERAL DESCRIPTION

The SPC122A is a two-channel speech/melody synthesizer including a 8-bit CMOS microprocessor with 69 instructions, 128K-bytes of Flash ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 40 sec speech duration @ 6KHz sampling rate) and 128-byte working SRAM. Its external memory is capable of being extended up to 256K. It provides Multi-Duty-Cycle output that can be implemented for remote-control purposes. Other features such as two Timer/Counters, 28 Software Selectable I/Os, 2 audio current D/A outputs (or one PWM audio output), serial interface I/O port, and volume control are also built in SPC122A. For audio processing, melody and speech can be mixed into one output. It operates in a wide voltage range of 2.4V - 5.5V with the maximum clock speed of 6MHz. In addition, the SPC122A has a Clock Stop mode for power savings. The power saving mode saves the RAM contents, but freezes the oscillator to lead all other functions to standby mode.

2. BLOCKDIAGRAM



3. FEATURES

- 8-bit microprocessor
- **Provides 128K-byte Flash ROM for program and audio data**
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 2.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports Crystal Resonator or Rosc (with bonding option)
- Max. CPU clock: 2.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 28 general I/Os**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- **Approx. 40 sec speech**
  @ 6KHz sampling rate with 4-bit ADPCM
- **Two 8-bit D/A output**
- **One PWM audio output (single speaker)**
- **Volume control function**
- **Multi-Duty-Cycle outputs (1/2, 1/3, 1/4 duty)**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS**

Mnemonic	PIN No.	Type	Description
VDD	5 29 34 45 57	I	Positive supply for logic and I/O pins
VSS	17 27 50 66	I	Ground reference for logic and I/O pins
XI	32	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	31	O	Oscillator crystal output
OPT*	30	I	For ROSC option, OPT should be connected to VDD.
BURN	15	I	Burn, This pin is an active high to select the flash ROM program function
$\overline{CE}$	16	I	This pin is an active low to select this chip as a 1Mbits memory
$\overline{ROMOE}$	14	I/O	Data Output enable
SPOP	18	I	Serial program option
RESET	19	I	This pin is an active low reset to the chip.
TEST	36	I	TEST MODE
AUD1 AUD2	33 35	O O	AUDIO OUTPUT
D7 - 0	6 - 13	I/O	Data Bus
A17	4	O	Extended Memory Enable
A13 - 0 A16 - 14	74 - 60 3 - 1	I/O	Address Bus
IOA0 IOA1 IOA2 IOA3	46 47 48 49	I/O I/O I/O I/O	Port A is an 8-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A can be either Buffer or Open-drain NMOS types (Sink current). IOA0: Serial programming clock output IOA2: Multi-duty cycle output ***See note 1 and 2 below.
IOB0 IOB1 IOB2 IOB4 IOB5 IOB6 IOB7	59 58 56 54 53 52 51	I/O I/O I/O I/O I/O I/O I/O	Port B is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current). ***See note 1 and 2 below.

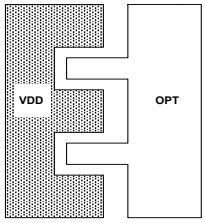
Mnemonic	PIN No.	Type	Description
IOC0	28	I/O	Port C is an 8-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer or Open-drain NMOS type (sink current).
IOC1	26	I/O	
IOC2	25	I/O	IOC0: Serial programming Data
IOC3	24	I/O	IOC1: EXT INT PIN
IOC4	23	I/O	IOC2: EXT COUNT IN
IOC5	22	I/O	
IOC6	21	I/O	
IOC7	20	I/O	***See note 1 and 2 below.
IOD0	44	I/O	Port D is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS (send current). (Port D can be software programmed for wake up I/O)
IOD1	43	I/O	
IOD2	42	I/O	
IOD3	41	I/O	
IOD4	40	I/O	
IOD5	39	I/O	
IOD6	38	I/O	
IOD7	37	I/O	***See note 1 and 2 below.

*OPT is the selection pin for ROSC or X'TAL using the bonding option. The shape looks like the figure at the right. When ROSC is selected, OPT is connected to VDD. If X'TAL is selected, OPT is floating. The reason OPT is near VDD is that when ROSC is selected, it is easy to make the connection between VDD and OPT.

**Refer to SPC Programming Guide for complete information.

***Note**: 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output (sink).



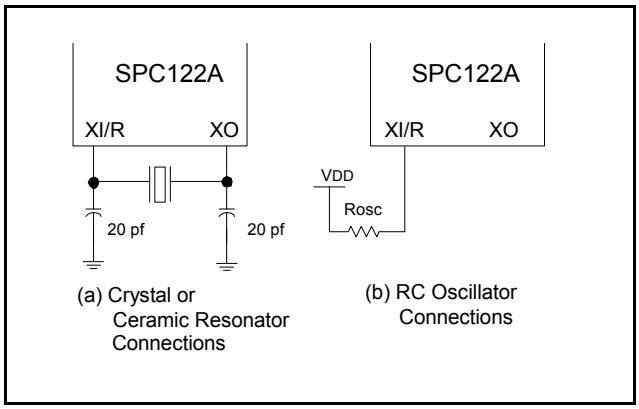
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The CPU of SPC122A is a high performance 8-bit processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed is up to 6MHz.

6.2. Oscillator

The SPC122A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources. The OSC options can be selected through bonding option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations if necessary. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



6.3. Bonding Option

The SPC122A has the following bonding option:

- Supports Crystal Resonator or Rosc (with bonding option).

6.4. ROM Area

The SPC122A provides a 128K-byte of Flash ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data. The combination of $\overline{CE}$ and Burn pins is capable of programming the Flash ROM as parallel mode. In contrast, using $\overline{CE}$ and SPOP pins can program the Flash ROM as serial mode. In addition, pin AD17 and $\overline{CE}$ can be used to extend the memory from 128K to 256K with external memory.

6.5. RAM Area

The total RAM size is 128 bytes (including Stack), located from $80 through $FF.

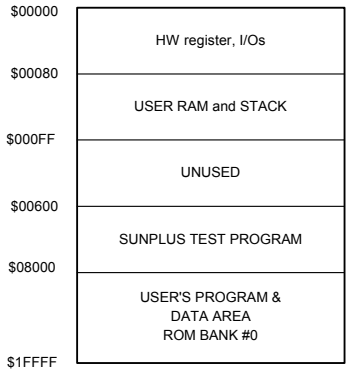
6.6. Map of Memory and I/Os

*I/O PORT:
- PORT IOA $0002
  IOB $0003
  IOC $0004
  IOD $0005
- I/O CONFIG $0000
  $0001

*NMI SOURCE:
- INTA (from TIMER A)

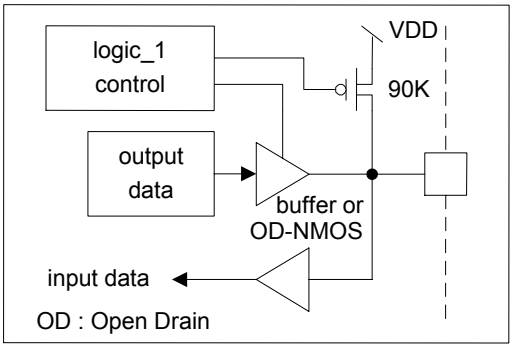
*INT SOURCE:
- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT
- Capable of being extended to 256K with external memory

*MEMORY MAP (From ROM view)

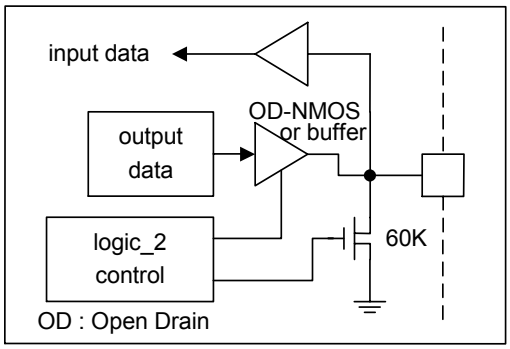


6.7. I/O Port Configuration*

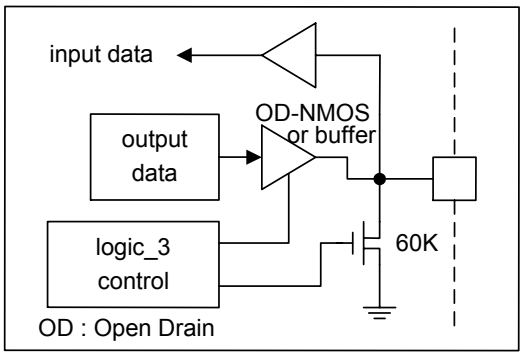
Input/Output IOA port : IOA3 - 0



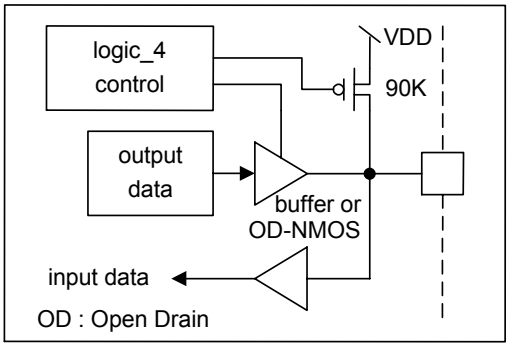
Input/Output IOB port : IOB2 - 0



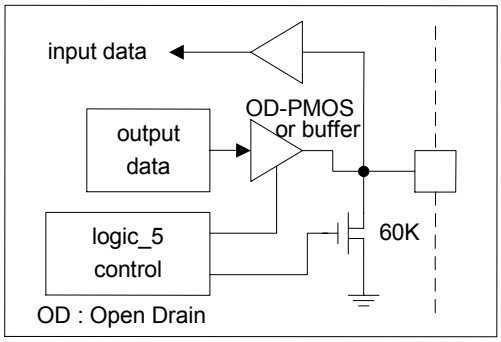
Input/Output IOB port : IOB5 - 4



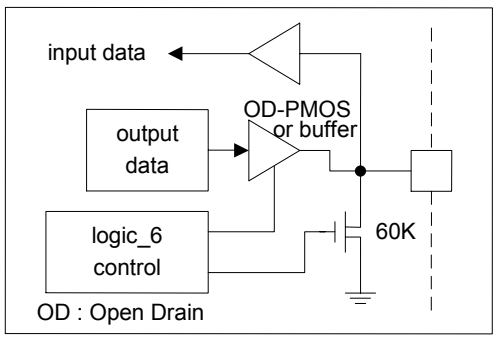
Input/Output IOC port : IOC3 - 0



Input/Output IOD port : IOD3 - 0



Input/Output IOD port : IOD7 - 4

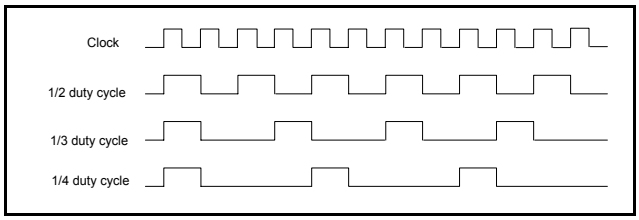


*Values shown are for VDD = 5.0V test conditions only.

6.8. Multi-Duty Cycle Mode

The SPC122A offers three unique output waveforms, 1/2, 1/3, and 1/4 duty cycles. The Control Register should be configured to select 1/2, 1/3, or 1/4 duty cycle and the IOA2 should be programmed as the multi-duty cycle output port. Programmers can use the combinations of these duty cycles for remote-control purpose.

6.9. 1/2, 1/3, 1/4 Duty Cycle Outputs



6.10. Serial Interface I/O

The SPC122A provides serial interface I/O mode for extending size of ROM/RAM. Serial Interface I/O Port can be used to read/write data from/to extra memory. The interface I/O Register is the control register for programming interface I/O.

6.11. Speech and Melody

For speech synthesis, the SPC122A can provide NMI for precise sampling frequency. Users can record or synthesize the sound and store it into ROM. The sound data can be played back according to the program's design. Several algorithms are recommended for high fidelity and compression of sound such as PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPC122A offers two-channel(dual) tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate specific frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

6.12. Power Saving Mode

The SPC122A provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states CPU wakes up. Port IOD7 - 0 is the only wake-up source in the SPC122A. After the SPC122A wakes up, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue to execute the rest of program. Wakeup Reset will not influence RAM or I/Os (See FIG.1).

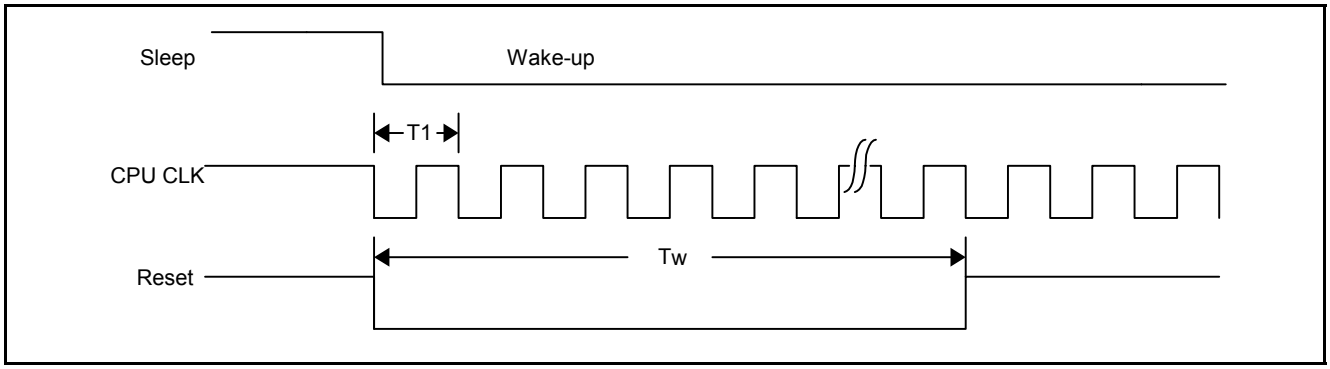


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧ 65536 x T1

6.13. Timer/Counter

The SPC122A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal leads the timer to reload the user's pre-set value and continue to count again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Timer/Counter Clock source can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.14. Volume Control Function

A volume control function provides 8-step volume controller to control current D/A output. The volume level can be controlled through software programming. For more information on how to adjust a volume level, please refer to SPC programming guide.

Differences between SPC121A and SPC122A

	SPC121A	SPC122A
Work range	F_{CPU} (max.)=4.0MHz @VDD=2.4V-3.6V F_{CPU} (max.)=6.0MHz @VDD=3.6V-5.5V	F_{CPU} (max.)=2.0MHz @VDD=2.4V-3.6V F_{CPU} (max.)=6.0MHz @VDD=3.6V-5.5V
ROM type	Mask	Flash
ROM SIZE	120K	128K
I/O port	21	28
SIO	×	✓
PWM Output	×	✓
Multiphase Output	×	✓
Volume Control	×	✓

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{CPU}	-	1.0	2.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery
CPU Clock	F_{CPU}	-	-	6.0	MHz	F_{CPU} = F_{OSC2} @ 5.0V

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

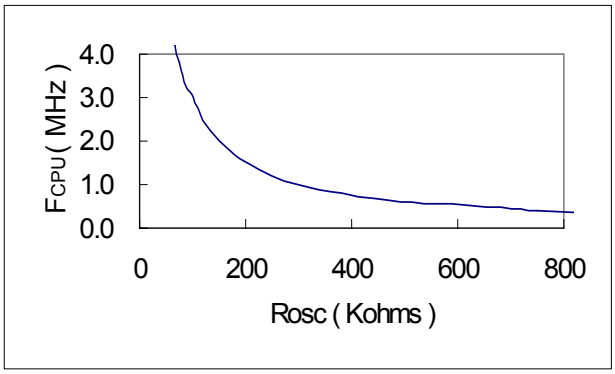
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 2.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.8	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I IOA, IOB, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink I IOA, IOB, IOC, IOD	I_{OL}	2.0	-	-	mA	VDD = 3.0V V_{OL} = 0.8V
Input Resistor IOB, IOD	R_{IN}	-	120	-	Kohm	Pull Low, VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

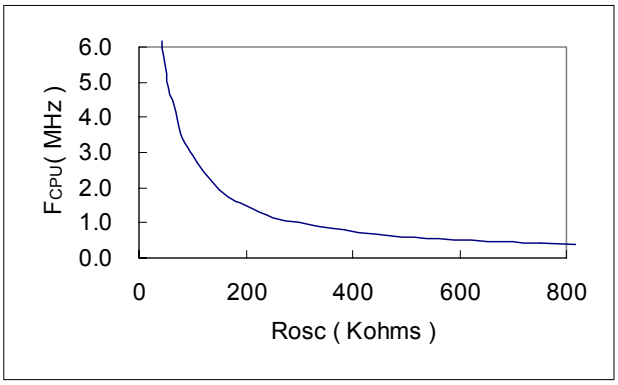
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	6.5	8.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V
Input high level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output high I IOA, IOB, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5.0V V_{OH} = 4.2V
Output sink I IOA, IOB, IOD	I_{OL}	4.0	-	-	mA	VDD = 5.0V V_{OL} = 0.8V
Input resistor IOA, IOB, IOC, IOD	R_{IN}	-	60	-	kohm	Pull Low VDD = 5.0V

7.5. The Relationship between the R_{OSC} and the F_{OSC}

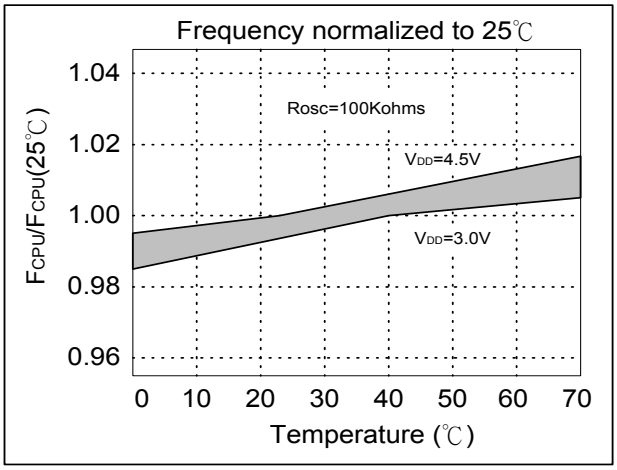
7.5.1. VDD = 3.0V, T_A = 25℃



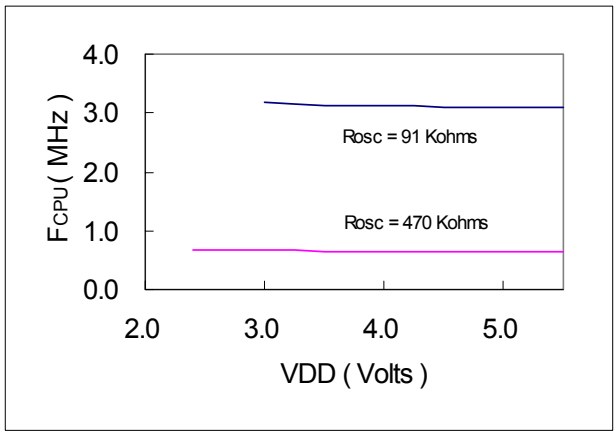
7.5.2. VDD = 4.5V, T_A = 25℃



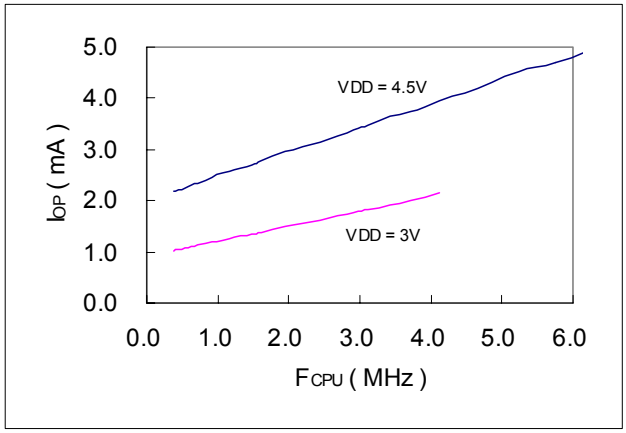
7.5.3. Frequency vs. temperature



7.5.4. Frequency vs. VDD

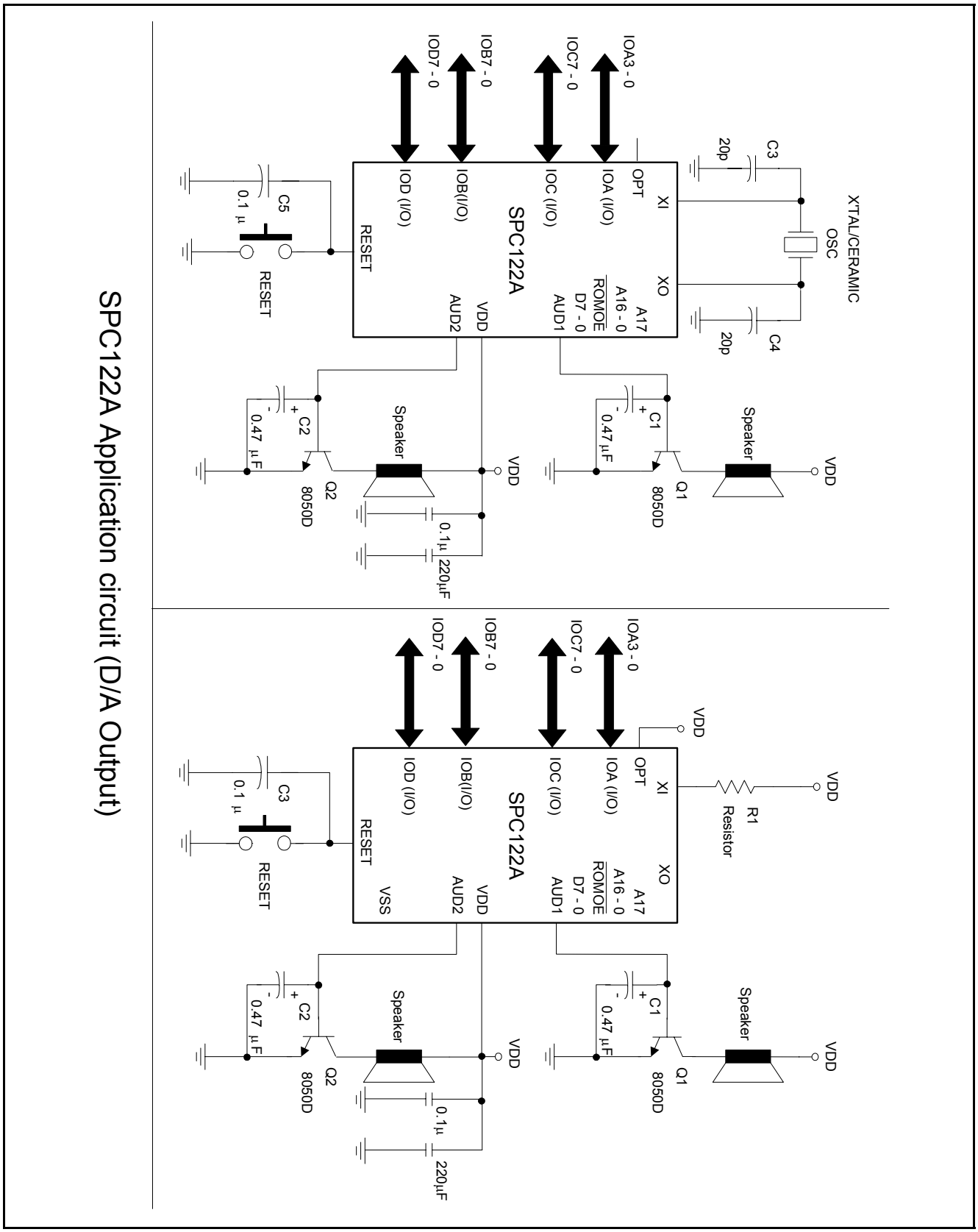


7.5.5. Operating current vs. frequency vs. VDD

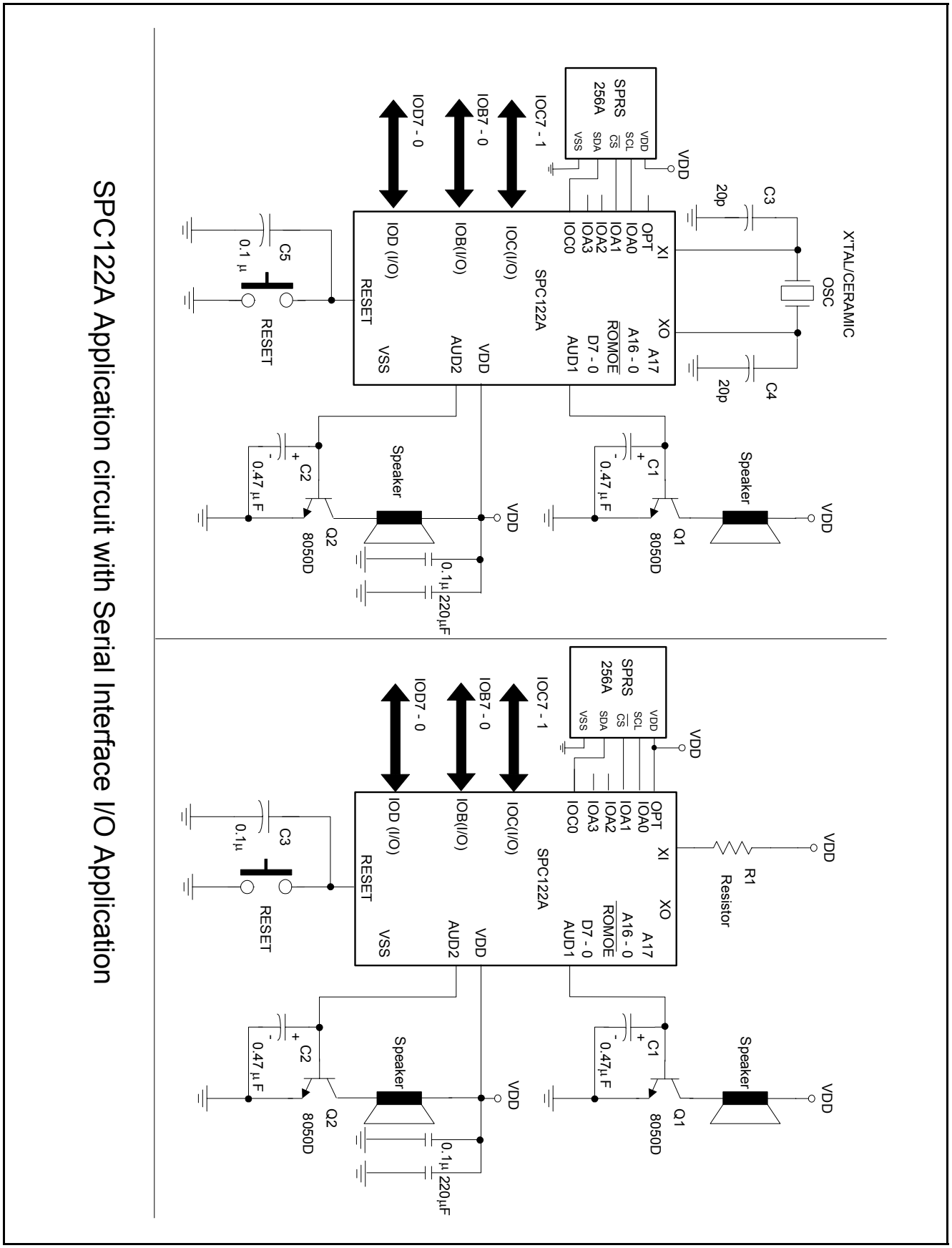


8. APPLICATION CIRCUITS

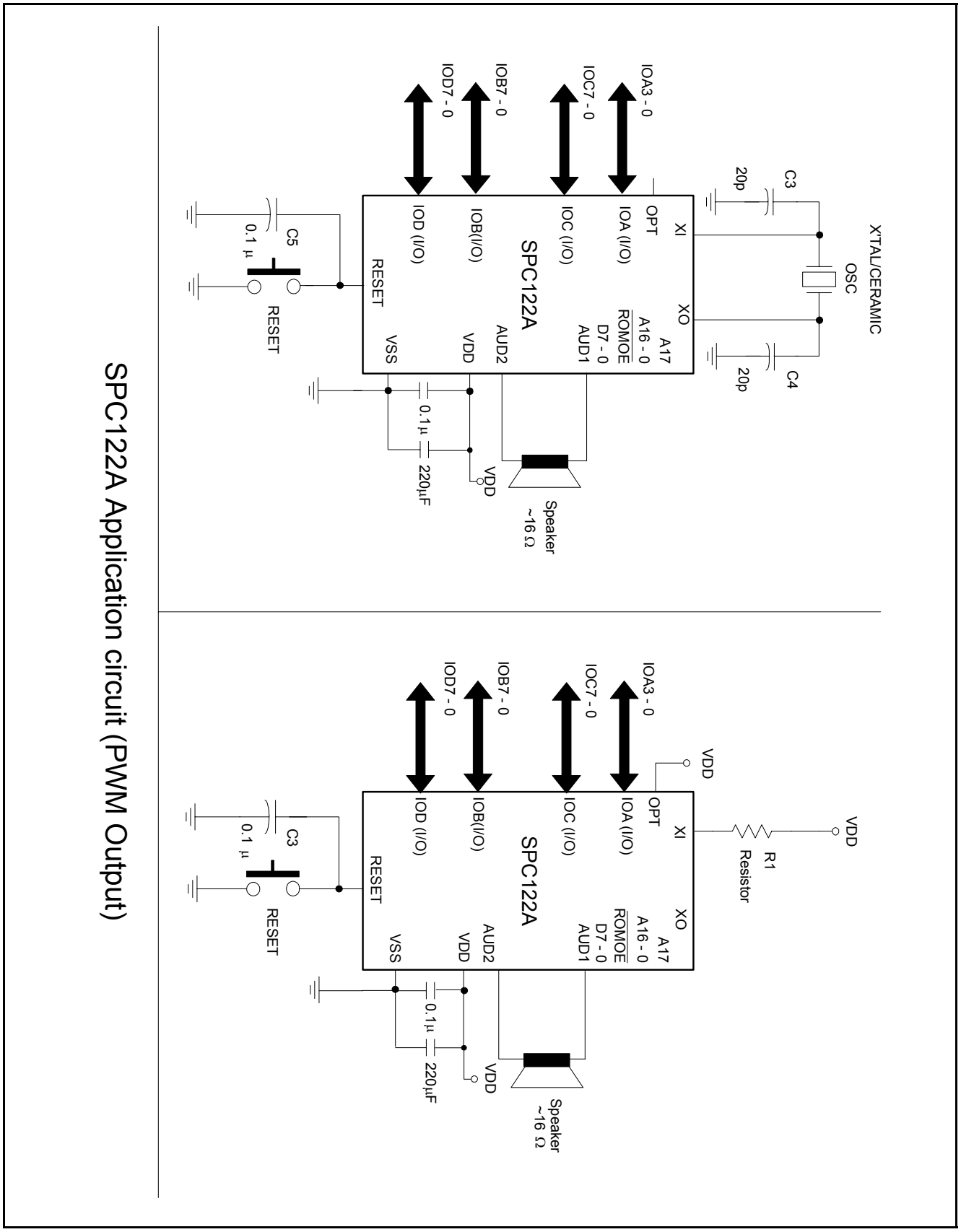
8.1. Application Circuit - (1)



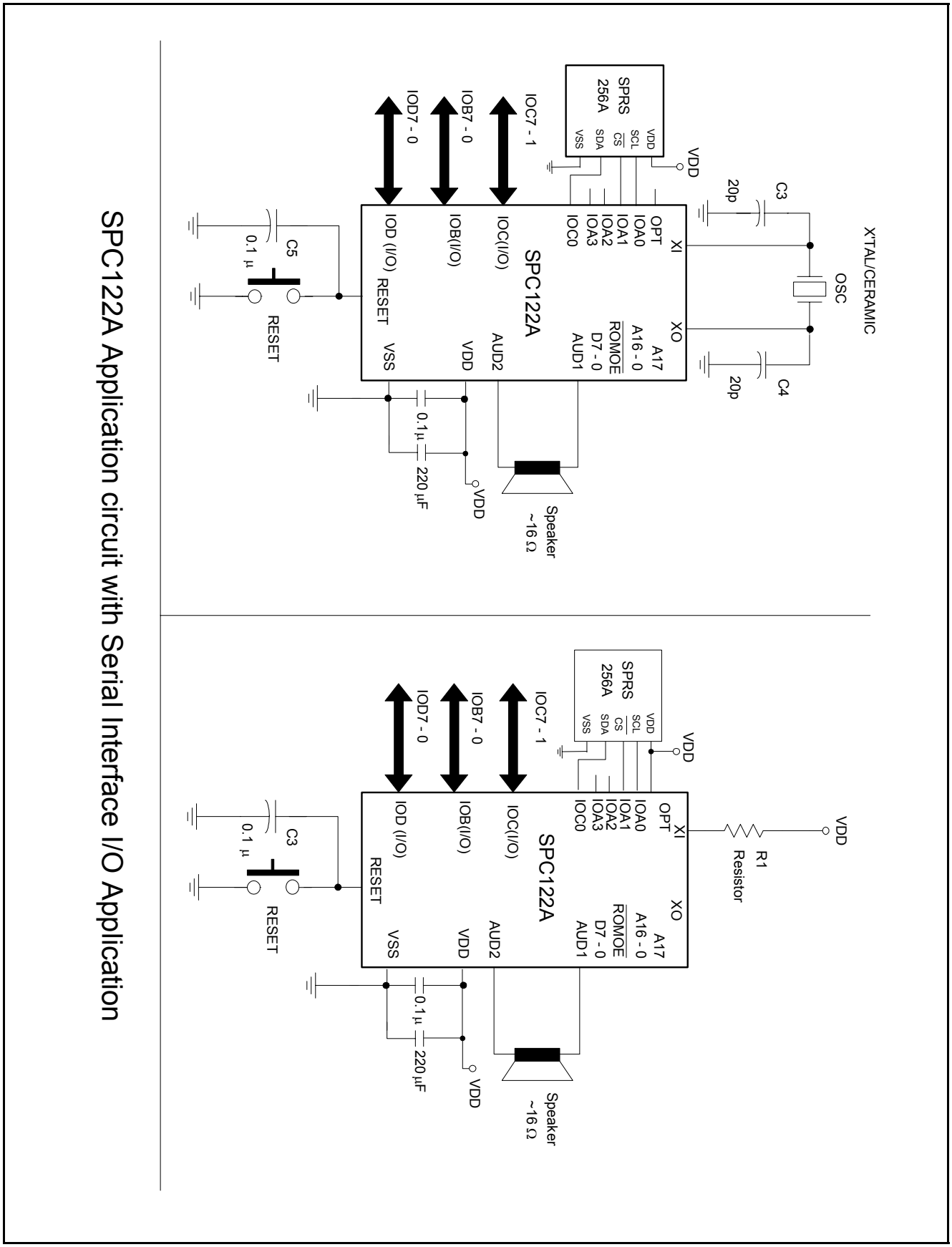
8.2. Application Circuit - (2)



8.3. Application Circuit - (3)

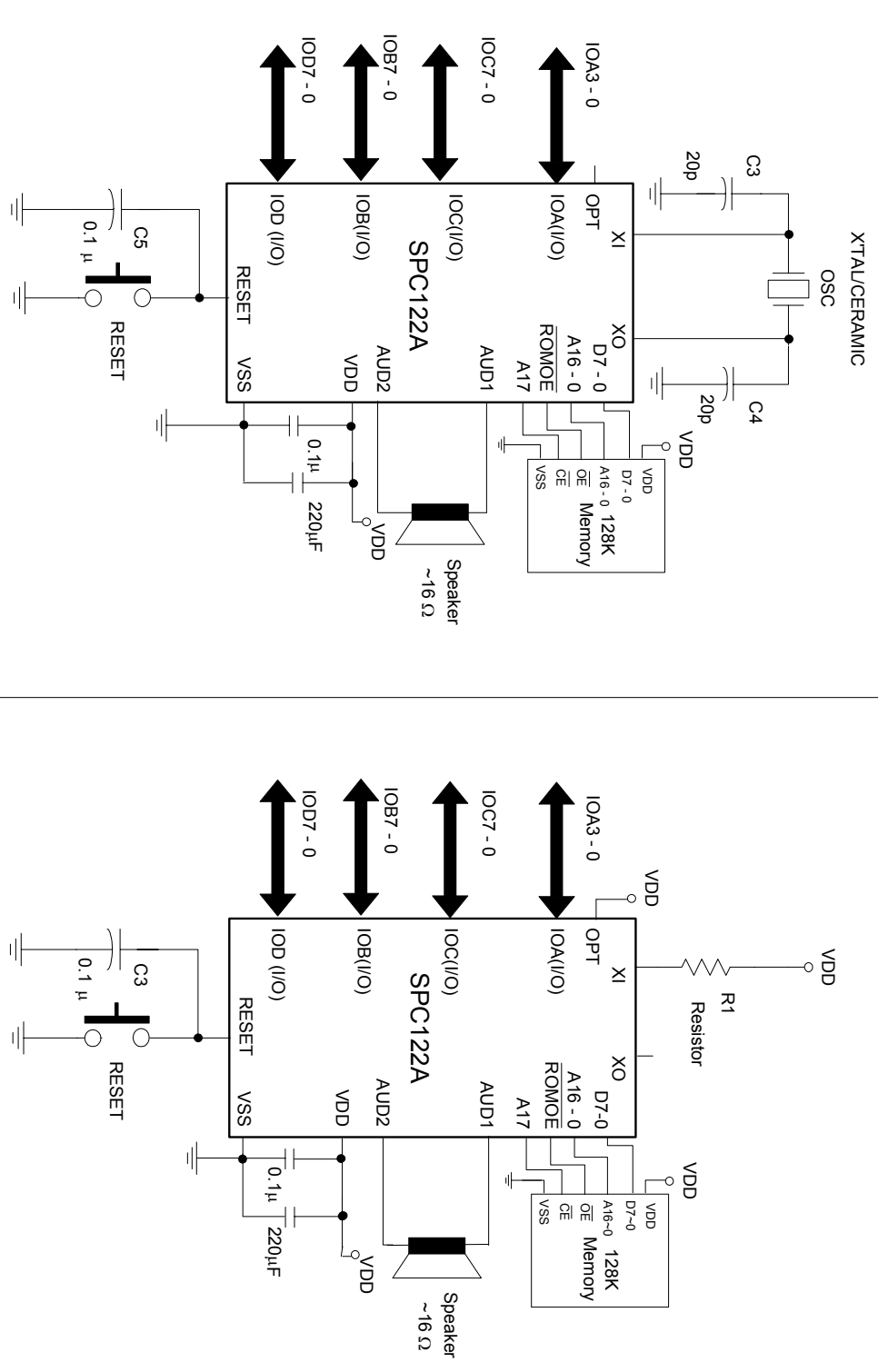


8.4. Application Circuit - (4)

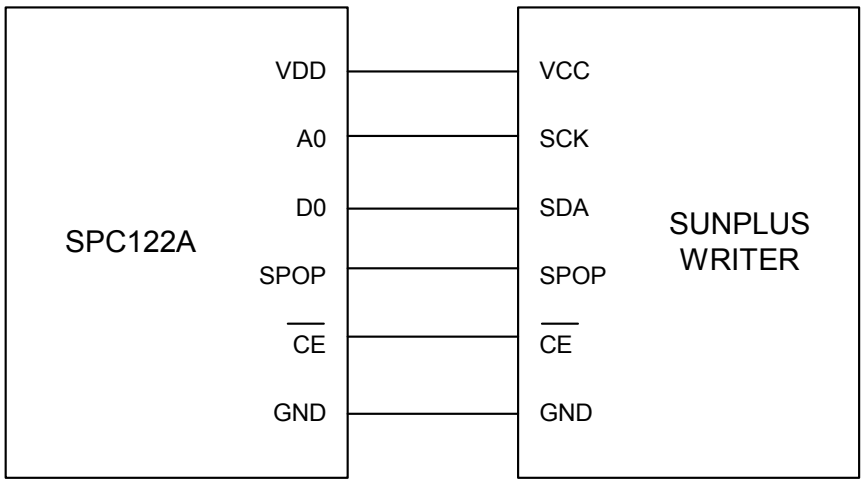


8.5. Application Circuit - (5)

SPC122A Application circuit with extension memory from 128K to 256K



8.6. Application Circuit - (6)



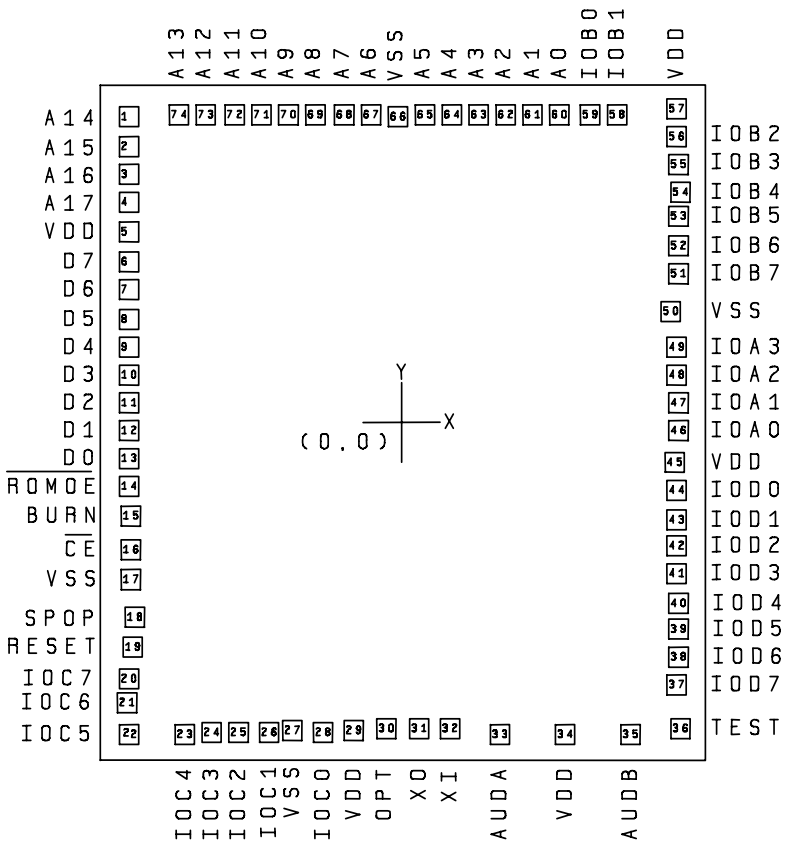
A0 : Address 0

D0 : Data 0

SPC122A SERIAL PROGRAMMING METHOD

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 3500μm x 3300μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC function properly, bond all VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC122A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	A14	-1429	1538	38	IOD6	1432	-1182
2	A15	-1429	1388	39	IOD5	1432	-1038
3	A16	-1429	1247	40	IOD4	1434	-906
4	A17	-1429	1107	41	IOD3	1426	-759
5	VDD	-1424	956	42	IOD2	1427	-620
6	D7	-1429	806	43	IOD1	1427	-485
7	D6	-1429	666	44	IOD0	1424	-342
8	D5	-1429	525	45	VDD	1416	-197
9	D4	-1429	385	46	IOA0	1433	-43
10	D3	-1429	245	47	IOA1	1433	98
11	D2	-1429	104	48	IOA2	1426	238
12	D1	-1429	-36	49	IOA3	1428	381
13	D0	-1429	-176	50	VSS	1400	564
14	$\overline{\text{ROMOE}}$	-1429	-316	51	IOB7	1432	754
15	BURN	-1417	-466	52	IOB6	1437	895
16	$\overline{\text{CE}}$	-1417	-641	53	IOB5	1432	1040
17	VSS	-1417	-791	54	IOB4	1443	1164
18	SPOP	-1397	-979	55	IOB3	1440	1303
19	RESET	-1401	-1126	56	IOB2	1426	1441
20	IOC7	-1422	-1285	57	VDD	1421	1582
21	IOC6	-1433	-1412	58	IOB1	1113	1547
22	IOC5	-1424	-1570	59	IOB0	972	1547
23	IOC4	-1134	-1568	60	A0	816	1547
24	IOC3	-994	-1557	61	A1	675	1547
25	IOC2	-851	-1558	62	A2	535	1547
26	IOC1	-699	-1559	63	A3	394	1547
27	VSS	-573	-1547	64	A4	254	1547
28	IOC0	-416	-1562	65	A5	113	1547
29	VDD	-259	-1549	66	VSS	-29	1537
30	OPT	-81	-1541	67	A6	-169	1547
31	XO	81	-1542	68	A7	-309	1547
32	XI	247	-1542	69	A8	-458	1547
33	AUD1	508	-1574	70	A9	-598	1547
34	VDD	847	-1574	71	A10	-739	1547
35	AUD2	1186	-1574	72	A11	-879	1547
36	TEST	1441	-1542	73	A12	-1020	1547
37	IOD7	1426	-1320	74	A13	-1160	1547

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 02, 1998	0.1	Original	
JUN. 09, 1999	0.2	Modify: IOA0 -> A0; IOC0 -> D0	17
NOV. 18, 1999	0.3	1. Modify format 2. Add "*The Relationship between the R_{osc} and The F_{osc}*"	
MAR. 23, 2000	0.4	Modify: IOA0 -> A0, IOC0 -> D0	16
JUN. 16, 2000	0.5	Add Operating Current : F_{CPU} = 2.0MHz @ 3.0V, no load	
NOV. 08, 2000	0.6	1. VDD = 2.4V - 3.6V for 2-battery application. 2. Speech duration @ 6KHz sampling rate with 4-bit ADPCM 3. Approx. 40 sec. speech.	
DEC. 20, 2000	0.7	1. Modify Application Circuit (6): Serial Programming Method 2. Add "*REVISION HISTORY*" 3. Renew to a new document format	15 19
FEB. 16, 2001	0.8	1. Remove "PWM mode" from "*VOLUME CONTROL FUNCTION*" 2. Add "Note: The 0.1uF capacitor between VDD and VSS…"	4 16
SEP. 07, 2001	0.9	1. Correct chip size 2. Add Note1 in the "*9.1 PAD Assignment*" 3. Renew to a new document format	17 17