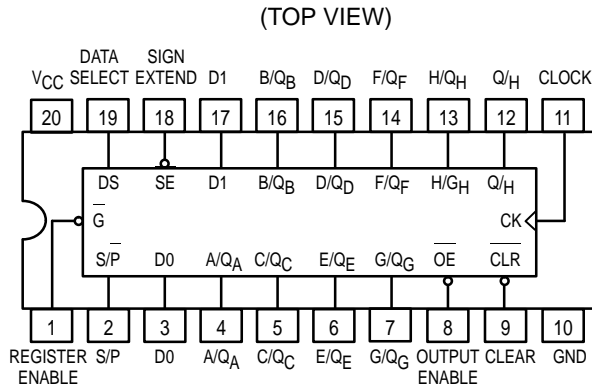




8-BIT SHIFT REGISTERS WITH SIGN EXTEND

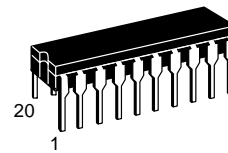
These 8-bit shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D0 or D1 inputs as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data is entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip-flop during shifting. An overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Sign Extend Function
- Direct Overriding Clear
- 3-State Outputs Drive Bus Lines Directly

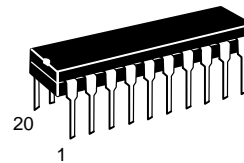


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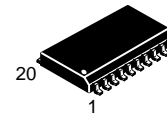
8-BIT SHIFT REGISTERS WITH SIGN EXTEND
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

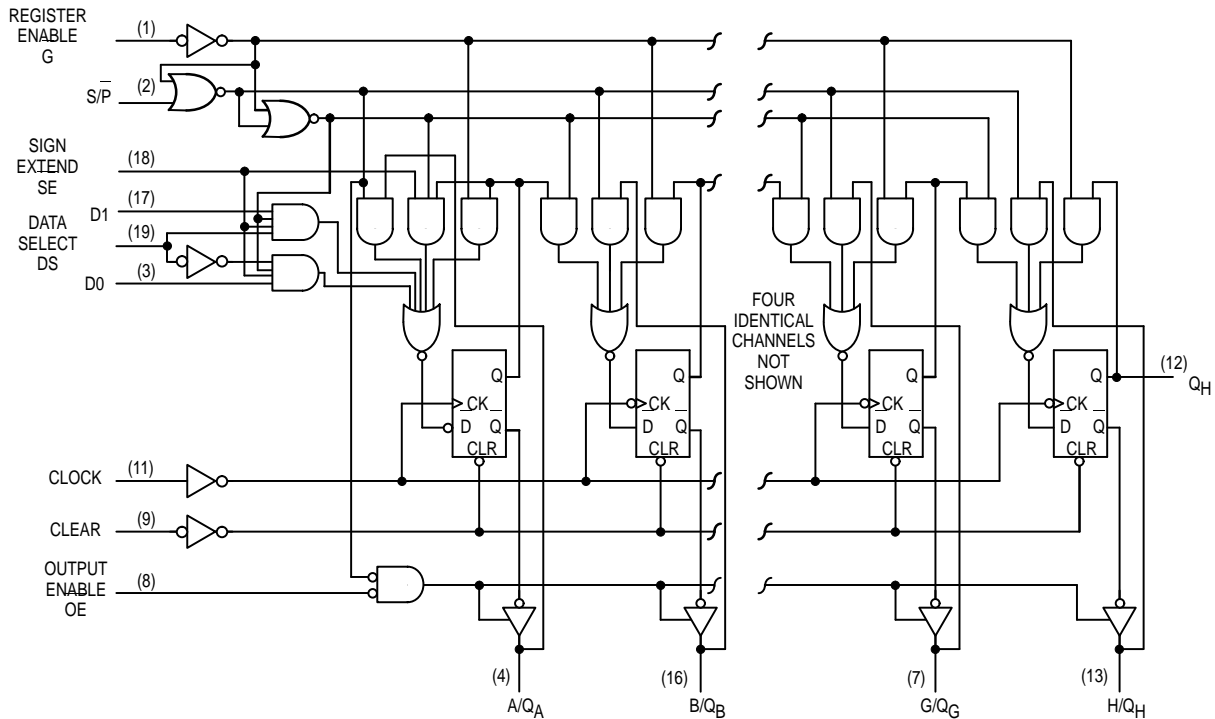
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-----------------|--|----------|-------------|------------|--------------|------|
| V _{CC} | Supply Voltage | 54 74 | 4.5 4.75 | 5.0 5.0 | 5.5 5.25 | V |
| T _A | Operating Ambient Temperature Range | 54 74 | -55 0 | 25 25 | 125 70 | °C |
| I _{OH} | Output Current — High Q _H ' | 54, 74 | | | -0.4 | mA |
| I _{OL} | Output Current — Low Q _H ' | 54 74 | | | 4.0 8.0 | mA |
| I _{OH} | Output Current — High Q _A -Q _H | 54 74 | | | -1.0 -2.6 | mA |
| I _{OL} | Output Current — Low Q _A -Q _H | 54 74 | | | 12 24 | mA |

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BLOCK DIAGRAM



FUNCTION TABLE

| OPERATION | INPUTS | | | | | | | INPUTS/OUTPUTS | | | | OUTPUT QH' |
|-------------|--------|--------------------|-----|----------------|----------------|------------------|-------|----------------|------|------------------|-----|---------------|
| | CLEAR | REGISTER ENABLE | S/P | SIGN EXTEND | DATA SELECT | OUTPUT ENABLE | CLOCK | A/QA | B/QB | C/QC ... H/QH | | |
| Clear | L | H | X | X | X | L | X | L | L | L | L | L |
| | L | X | H | X | X | L | X | L | L | L | L | L |
| Hold | H | H | X | X | X | L | X | QA0 | QB0 | QC0 | QH0 | QH0 |
| Shift Right | H | L | H | H | L | L | ↑ | D0 | QAn | QBn | QGn | QGn |
| | H | L | H | H | H | L | ↑ | D1 | QAn | QBn | QGn | QGn |
| Sign Extend | H | L | H | L | X | L | ↑ | QAn | QAn | QBn | QGn | QGn |
| Load | H | L | L | X | X | X | ↑ | a | b | c | h | h |

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = HIGH Level (steady state)

L = LOW Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from LOW to HIGH level

QA0...QH0 = the level of QA through QH, respectively, before the indicated steady-state conditions were established

QAn...QHn = the level of QA through QH, respectively, before the most recent ↑ transition of the clock

D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively

a...h = the level of steady-state inputs at inputs A through H respectively

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | | Limits | | | Unit | Test Conditions | |
|------------------|---|--------------------------------|--------|-------|--|------|---|---|
| | | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| V _{IL} | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| V _{IK} | Input Clamp Diode Voltage | | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA | |
| V _{OH} | Output HIGH Voltage Q _A -Q _H | 54 | 2.4 | 3.2 | | V | V _{CC} = MIN, I _{OH} = MAX | |
| | | 74 | 2.4 | 3.2 | | V | | |
| V _{OH} | Output HIGH Voltage Q _H ' | 54 | 2.5 | 3.4 | | V | V _{CC} = MIN, I _{OH} = MAX | |
| | | 74 | 2.7 | 3.4 | | V | | |
| V _{OL} | Output LOW Voltage Q _A -Q _H | 54, 74 | | 0.25 | 0.4 | V | I _{OL} = 12 mA | V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | I _{OL} = 24 mA | |
| V _{OL} | Output LOW Voltage Q _H ' | 54, 74 | | | 0.4 | V | I _{OL} = 4.0 mA | V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table |
| | | 74 | | | 0.5 | V | I _{OL} = 8.0 mA | |
| I _{OZH} | Output Off Current HIGH Q _A -Q _H | | | | 40 | μA | V _{CC} = MAX, V _{OUT} = 2.7 V | |
| I _{OZL} | Output Off Current LOW Q _A -Q _H | | | | -400 | μA | V _{CC} = MAX, V _{OUT} = 0.4 V | |
| I _{IH} | Input HIGH Current | Other | | | 20 | μA | V _{CC} = MAX, V _{IN} = 2.7 V | |
| | | A-H, Data Select | | | 40 | μA | | |
| | | Sign Extend | | | 60 | μA | | |
| | | Other | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V | |
| | | Data Select | | | 0.2 | mA | | |
| | | Sign Extend | | | 0.3 | mA | | |
| A-H | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 5.5 V | | | |
| I _{IL} | Input LOW Current | Other | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V | |
| | | Data Select | | | -0.8 | mA | | |
| | | Sign Extend | | | -1.2 | mA | | |
| I _{OS} | Short Circuit Current (Note 1) | Q _H ' | -20 | | -100 | mA | V _{CC} = MAX | |
| | | Q _A -Q _H | -30 | | -130 | mA | V _{CC} = MAX | |
| I _{CC} | Power Supply Current | | | | 60 | mA | V _{CC} = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

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AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|--------------------------------------|--|--------|----------|----------|------|---|
| | | Min | Typ | Max | | |
| f _{MAX} | Maximum Clock Frequency | 25 | 35 | | MHz | C _L = 15 pF |
| t _{PHL} t _{PLH} | Propagation Delay, Clock to Q _H ' | | 26 22 | 35 33 | ns | |
| t _{PHL} | Propagation Delay, Clear to Q _H ' | | 27 | 35 | ns | |
| t _{PHL} t _{PLH} | Propagation Delay, Clock to Q _A -Q _H | | 22 16 | 33 25 | ns | C _L = 45 pF, R _L = 667 Ω |
| t _{PHL} | Propagation Delay, Clear to Q _A -Q _H | | 22 | 35 | ns | |
| t _{PZH} t _{PZL} | Output Enable Time | | 15 15 | 35 35 | ns | |
| t _{PHZ} t _{PLZ} | Output Disable Time | | 15 15 | 25 25 | ns | C _L = 5.0 pF |

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|------------------|------------------------|--------|-----|-----|------|-------------------------|
| | | Min | Typ | Max | | |
| t _W | Clock Pulse Width HIGH | 25 | | | ns | V _{CC} = 5.0 V |
| t _W | Clock Pulse Width LOW | 15 | | | ns | |
| t _W | Clear Pulse Width LOW | 20 | | | ns | |
| t _S | Data Setup Time | 20 | | | ns | |
| t _S | Select Setup Time | 15 | | | ns | |
| t _H | Data Hold Time | 0 | | | ns | |
| t _H | Select Hold Time | 10 | | | ns | |
| t _{rec} | Recovery Time | 20 | | | ns | |

DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.