



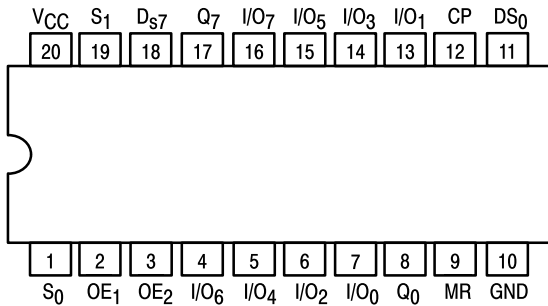
# 8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q<sub>0</sub> and Q<sub>7</sub> to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

## CONNECTION DIAGRAM DIP (TOP VIEW)

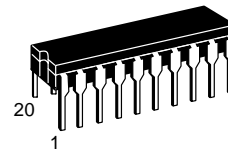


NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

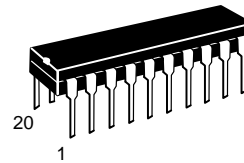
## SN54/74LS299

### 8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

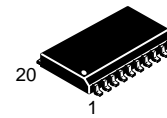
#### LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 732-03



**N SUFFIX**  
PLASTIC  
CASE 738-03



**DW SUFFIX**  
SOIC  
CASE 751D-03

### ORDERING INFORMATION

SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic  
SN74LSXXXDW SOIC

### PIN NAMES

|                                   |   |
|-----------------------------------|---|
| CP                                | Clock Pulse (active positive-going edge) Input            |
| DS0                               | Serial Data Input for Right Shift                         |
| DS7                               | Serial Data Input for Left Shift                          |
| I/O <sub>n</sub>                  | Parallel Data Input or Parallel Output (3-State) (Note c) |
| OE <sub>1</sub> , OE <sub>2</sub> | 3-State Output Enable (active LOW) Inputs                 |
| Q <sub>0</sub> , Q <sub>7</sub>   | Serial Outputs (Note b)                                   |
| MR                                | Asynchronous Master Reset (active LOW) Input              |
| S <sub>0</sub> , S <sub>1</sub>   | Mode Select Inputs  |

### NOTES:

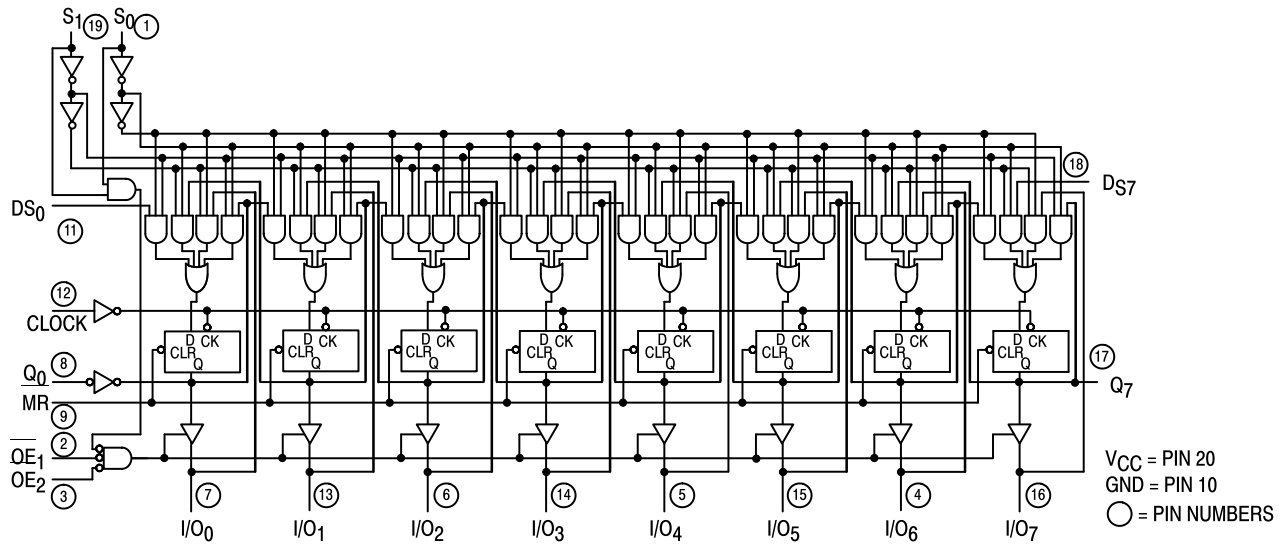
- 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
- The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74). The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

### LOADING (Note a)

| HIGH         | LOW           |
|--------------|---------------|
| 0.5 U.L.     | 0.25 U.L.     |
| 0.5 U.L.     | 0.25 U.L.     |
| 0.5 U.L.     | 0.25 U.L.     |
| 0.5 U.L.     | 0.25 U.L.     |
| 65 (25) U.L. | 15 (7.5) U.L. |
| 0.5 U.L.     | 0.25 U.L.     |
| 10 U.L.      | 5 (2.5) U.L.  |
| 0.5 U.L.     | 0.25 U.L.     |
| 1 U.L.       | 0.5 U.L.      |

# SN54/74LS299

## LOGIC DIAGRAM



## FUNCTION TABLE

| INPUTS |                |                |                 |                 |    |                 |                 | RESPONSE   |
|--------|----------------|----------------|-----------------|-----------------|----|-----------------|-----------------|--|
| MR     | S <sub>1</sub> | S <sub>0</sub> | OE <sub>1</sub> | OE <sub>2</sub> | CP | DS <sub>0</sub> | DS <sub>7</sub> |  |
| L      | X              | X              | H               | X               | X  | X               | X               | Asynchronous Reset; Q <sub>0</sub> = Q <sub>7</sub> = LOW<br>I/O Voltage Undetermined  |
| L      | X              | X              | X               | H               | X  | X               | X               | Asynchronous Reset; Q <sub>0</sub> = Q <sub>7</sub> = LOW<br>I/O Voltage LOW   |
| L      | H              | H              | X               | X               | X  | X               | X               |  |
| L      | L              | X              | L               | L               | X  | X               | X               | Shift Right; D <sub>0</sub> Q <sub>0</sub> Q <sub>1</sub> ; etc.<br>Shift Right; D <sub>0</sub> & I/O <sub>0</sub> ; Q <sub>0</sub> O <sub>1</sub> & I/O <sub>1</sub> ; etc. |
| H      | L              | H              | X               | X               | ⌋  | D               | X               |  |
| H      | L              | H              | L               | L               | ⌋  | D               | X               | Shift Left; D <sub>7</sub> Q <sub>7</sub> Q <sub>6</sub> ; etc.<br>Shift Left; D <sub>7</sub> & I/O <sub>7</sub> ; Q <sub>7</sub> Q <sub>6</sub> & I/O <sub>6</sub> ; etc.   |
| H      | H              | L              | X               | X               | ⌋  | X               | D               |  |
| H      | H              | L              | L               | L               | ⌋  | X               | D               | Parallel Load; I/O <sub>n</sub> Q <sub>n</sub>   |
| H      | H              | H              | X               | X               | ⌋  | X               | X               |  |
| H      | L              | L              | H               | X               | X  | X               | X               | Hold: I/O Voltage undetermined   |
| H      | L              | L              | X               | H               | X  | X               | X               |  |
| H      | L              | L              | L               | L               | X  | X               | X               | Hold: I/O <sub>n</sub> = Q <sub>n</sub>  |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |                                     | Min    | Typ | Max  | Unit |
|-----------------|-------------------------------------|-------------------------------------|--------|-----|------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54                                  | 4.5    | 5.0 | 5.5  | V    |
|                 |                                     | 74                                  | 4.75   | 5.0 | 5.25 |      |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54                                  | -55    | 25  | 125  | °C   |
|                 |                                     | 74                                  | 0      | 25  | 70   |      |
| I <sub>OH</sub> | Output Current — High               | Q <sub>0</sub> , Q <sub>7</sub>     | 54, 74 |     | -0.4 | mA   |
| I <sub>OL</sub> | Output Current — Low                | Q <sub>0</sub> , Q <sub>7</sub>     | 54     |     | 4.0  | mA   |
|                 |                                     | I/O <sub>0</sub> , I/O <sub>7</sub> | 74     |     | 8.0  |      |
| I <sub>OH</sub> | Output Current — High               | I/O <sub>0</sub> —I/O <sub>7</sub>  | 54     |     | -1.0 | mA   |
|                 |                                     | I/O <sub>0</sub> —I/O <sub>7</sub>  | 74     |     | -2.6 |      |
| I <sub>OL</sub> | Output Current — Low                | I/O <sub>0</sub> —I/O <sub>7</sub>  | 54     |     | 12   | mA   |
|                 |                                     | I/O <sub>0</sub> —I/O <sub>7</sub>  | 74     |     | 24   |      |

## FAST AND LS TTL DATA

# SN54/74LS299

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol           | Parameter   |   | Limits |       |      | Unit | Test Conditions                                 |   |
|------------------|---|---|--------|-------|------|------|---|---|
|                  |   |   | Min    | Typ   | Max  |      |   |   |
| V <sub>IH</sub>  | Input HIGH Voltage  |   | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs    |   |
| V <sub>IL</sub>  | Input LOW Voltage   | 54  |        |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs     |   |
|                  |   | 74  |        |       | 0.8  |      |   |   |
| V <sub>IK</sub>  | Input Clamp Diode Voltage                                     |   |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA |   |
| V <sub>OH</sub>  | Output HIGH Voltage<br>I/O <sub>0</sub> -I/O <sub>7</sub>     | 54  | 2.4    | 3.2   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX    |   |
|                  |   | 74  | 2.4    | 3.1   |      | V    |   |   |
| V <sub>OH</sub>  | Output HIGH Voltage<br>Q <sub>0</sub> , Q <sub>7</sub>        | 54  | 2.5    | 3.4   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX    |   |
|                  |   | 74  | 2.7    | 3.4   |      | V    |   |   |
| V <sub>OL</sub>  | Output LOW Voltage<br>I/O <sub>0</sub> -I/O <sub>7</sub>      | 54, 74  |        | 0.25  | 0.4  | V    | I <sub>OL</sub> = 12 mA                         | V <sub>CC</sub> = V <sub>CC</sub> MIN,<br>V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>per Truth Table |
|                  |   | 74  |        | 0.35  | 0.5  | V    | I <sub>OL</sub> = 24 mA                         |   |
| V <sub>OL</sub>  | Output LOW Voltage<br>I/O <sub>0</sub> -I/O <sub>7</sub>      | 54, 74  |        |       | 0.4  | V    | I <sub>OL</sub> = 4.0 mA                        | V <sub>CC</sub> = V <sub>CC</sub> MIN,<br>V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>per Truth Table |
|                  |   | 74  |        |       | 0.5  | V    | I <sub>OL</sub> = 8.0 mA                        |   |
| I <sub>OZH</sub> | Output Off Current HIGH<br>I/O <sub>0</sub> -I/O <sub>7</sub> |   |        |       | 40   | μA   | V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V |   |
| I <sub>OZL</sub> | Output Off Current LOW<br>I/O <sub>0</sub> -I/O <sub>7</sub>  |   |        |       | -400 | μA   | V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V |   |
| I <sub>IH</sub>  | Input HIGH Current  | Others  |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V  |   |
|                  |   | S <sub>0</sub> , S <sub>1</sub> ,<br>I/O <sub>0</sub> -I/O <sub>7</sub> |        |       | 40   | μA   |   |   |
|                  |   | Others  |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V  |   |
|                  |   | S <sub>0</sub> , S <sub>1</sub><br>I/O <sub>0</sub> -I/O <sub>7</sub>   |        |       | 0.2  | mA   |   |   |
| I <sub>IL</sub>  | Input LOW Current   | Others  |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V  |   |
|                  |   | S <sub>0</sub> , S <sub>1</sub>   |        |       | -0.8 | mA   |   |   |
| I <sub>OS</sub>  | Short Circuit Current<br>(Note 1)                             | Q <sub>0</sub> , Q <sub>7</sub>   | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX                           |   |
|                  |   | I/O <sub>0</sub> -I/O <sub>7</sub>                                      | -30    |       | -130 | mA   | V <sub>CC</sub> = MAX                           |   |
| I <sub>CC</sub>  | Power Supply Current  |   |        |       | 53   | mA   | V <sub>CC</sub> = MAX                           |   |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN54/74LS299

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

| Symbol                               | Parameter  | Limits |          |          | Unit | Test Conditions                                   |
|--------------------------------------|--|--------|----------|----------|------|---|
|                                      |  | Min    | Typ      | Max      |      |   |
| f <sub>MAX</sub>                     | Maximum Clock Frequency  | 25     | 35       |          | MHz  | C <sub>L</sub> = 15 pF                            |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay, Clock to Q <sub>0</sub> or Q <sub>7</sub>   |        | 26<br>22 | 39<br>33 | ns   |   |
| t <sub>PHL</sub>                     | Propagation Delay, Clear to Q <sub>0</sub> or Q <sub>7</sub>   |        | 27       | 40       | ns   |   |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay, Clock to I/O <sub>0</sub> –I/O <sub>7</sub> |        | 26<br>17 | 39<br>25 | ns   | C <sub>L</sub> = 45 pF,<br>R <sub>L</sub> = 667 Ω |
| t <sub>PHL</sub>                     | Propagation Delay, Clear to I/O <sub>0</sub> –I/O <sub>7</sub> |        | 26       | 40       | ns   |   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time   |        | 13<br>19 | 21<br>30 | ns   |   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time  |        | 10<br>10 | 15<br>15 | ns   | C <sub>L</sub> = 5.0 pF                           |

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

| Symbol           | Parameter              | Limits |     |     | Unit | Test Conditions         |
|------------------|------------------------|--------|-----|-----|------|-------------------------|
|                  |                        | Min    | Typ | Max |      |                         |
| t <sub>W</sub>   | Clock Pulse Width HIGH | 25     |     |     | ns   | V <sub>CC</sub> = 5.0 V |
| t <sub>W</sub>   | Clock Pulse Width LOW  | 13     |     |     | ns   |                         |
| t <sub>W</sub>   | Clear Pulse Width LOW  | 20     |     |     | ns   |                         |
| t <sub>S</sub>   | Data Setup Time        | 20     |     |     | ns   |                         |
| t <sub>S</sub>   | Select Setup Time      | 35     |     |     | ns   |                         |
| t <sub>H</sub>   | Data Hold Time         | 0      |     |     | ns   |                         |
| t <sub>H</sub>   | Select Hold Time       | 10     |     |     | ns   |                         |
| t <sub>rec</sub> | Recovery Time          | 20     |     |     | ns   |                         |

# SN54/74LS299

## 3-STATE WAVEFORMS

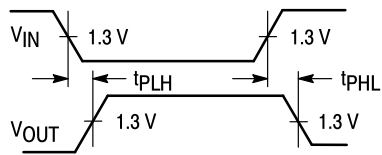


Figure 1

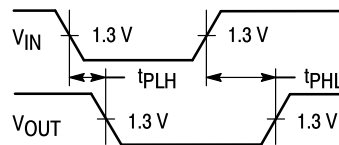


Figure 2

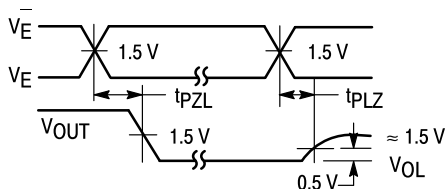


Figure 3

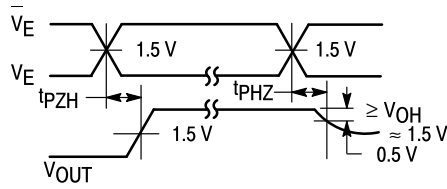
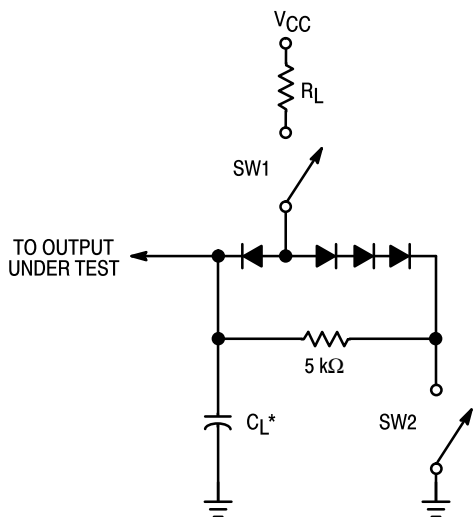


Figure 4

## AC LOAD CIRCUIT



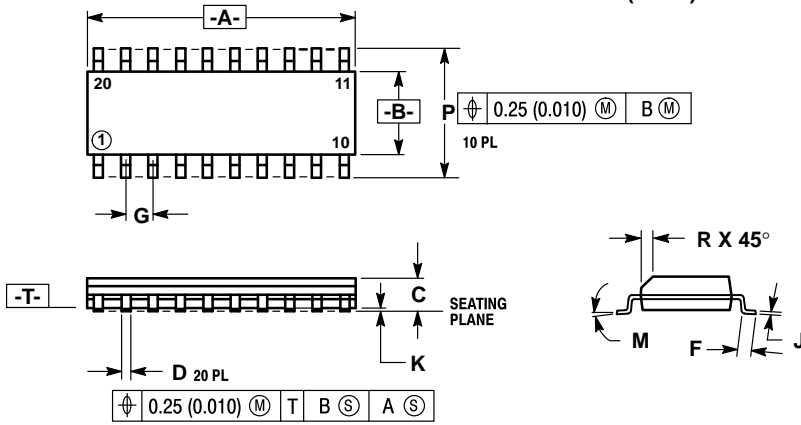
\* Includes Jig and Probe Capacitance.

### SWITCH POSITIONS

| SYMBOL           | SW1    | SW2    |
|------------------|--------|--------|
| t <sub>PZH</sub> | Open   | Closed |
| t <sub>PZL</sub> | Closed | Open   |
| t <sub>PLZ</sub> | Closed | Closed |
| t <sub>PHZ</sub> | Closed | Closed |

Figure 5

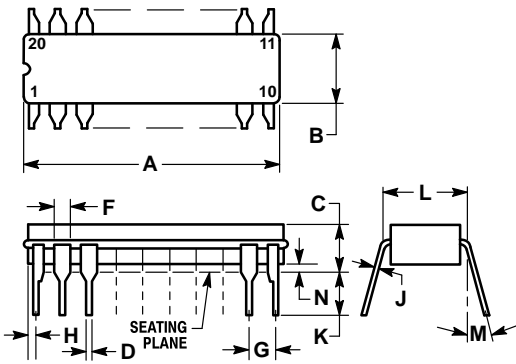
**Case 751D-03 DW Suffix  
20-Pin Plastic  
SO-20 (WIDE)**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 12.65       | 12.95 | 0.499     | 0.510 |
| B   | 7.40        | 7.60  | 0.292     | 0.299 |
| C   | 2.35        | 2.65  | 0.093     | 0.104 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.50        | 0.90  | 0.020     | 0.035 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.25        | 0.32  | 0.010     | 0.012 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 10.05       | 10.55 | 0.395     | 0.415 |
| R   | 0.25        | 0.75  | 0.010     | 0.029 |

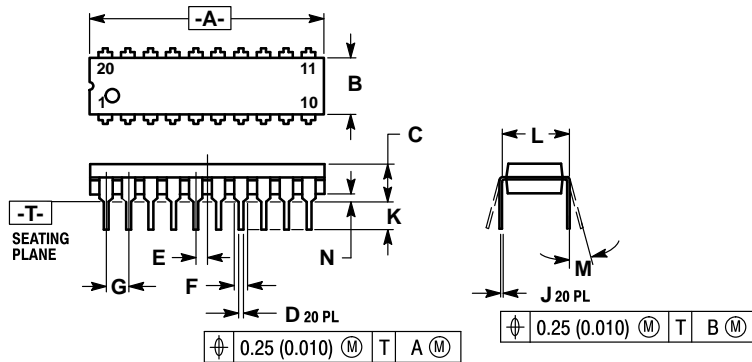
**Case 732-03 J Suffix  
20-Pin Ceramic Dual In-Line**



- NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
  2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIM A AND B INCLUDES MENISCUS.


| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 23.88       | 25.15 | 0.940     | 0.990 |
| B   | 6.60        | 7.49  | 0.260     | 0.295 |
| C   | 3.81        | 5.08  | 0.150     | 0.200 |
| D   | 0.38        | 0.56  | 0.015     | 0.022 |
| F   | 1.40        | 1.65  | 0.055     | 0.065 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.51        | 1.27  | 0.020     | 0.050 |
| J   | 0.20        | 0.30  | 0.008     | 0.012 |
| K   | 3.18        | 4.06  | 0.125     | 0.160 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | 0°          | 15°   | 0°        | 15°   |
| N   | 0.25        | 1.02  | 0.010     | 0.040 |

**Case 738-03 N Suffix  
20-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. 738-02 OBSOLETE, NEW STANDARD 738-03.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 25.66       | 27.17 | 1.010     | 1.070 |
| B   | 6.10        | 6.60  | 0.240     | 0.260 |
| C   | 3.81        | 4.57  | 0.150     | 0.180 |
| D   | 0.39        | 0.55  | 0.015     | 0.022 |
| E   | 1.27 BSC    |       | 0.050 BSC |       |
| F   | 1.27        | 1.77  | 0.050     | 0.070 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| J   | 0.21        | 0.38  | 0.008     | 0.015 |
| K   | 2.80        | 3.55  | 0.110     | 0.140 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | 0°          | 15°   | 0°        | 15°   |
| N   | 0.51        | 1.01  | 0.020     | 0.040 |

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**Literature Distribution Centers:**

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

| SYMBOL | SW1    | SW2    |
|--------|--------|--------|
| tPZH   | Open   | Closed |
| tPZL   | Closed | Open   |
| tPLZ   | Closed | Closed |

