DATA SHEET

凌陽科技
SUNPLUS

SPC1000A

1024KB Sound Controller

SEP. 14, 2001

Version 2.6

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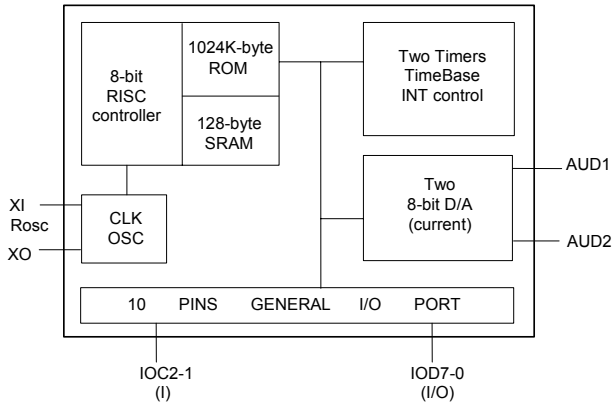
1024KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC1000A is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 1024K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 340 sec speech duration @ 6KHz sampling rate) and 128-byte working SRAM. It includes two Timer/Counters, 8 programmable I/Os with 2 input pins, and two 8-bit current output (D/A). For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V. In addition, the SPC1000A has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPC1000A includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- **Provides 1024K-byte ROM for program and audio data**
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports Crystal Resonator or Rosc (with Mask option)
- Max. CPU clock: 4.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 8 general I/Os + 2 inputs**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- **Approx. 340 sec speech**
  @ 6KHz sampling rate with 4-bit ADPCM
- **Two 8-bit current outputs(D/A)**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	16	I	POWER VDD
VSS	11	I	POWER VSS
XI	10	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	9	O	Oscillator crystal output
RESET	14	I	This pin is an active low reset for the chip
TEST	15	I	TEST MODE
AUD1	13	O	AUDIO OUTPUT
AUD2	12		
IOC1	8	I	Port C is an input port only. As inputs, Port C can be in either the Pure or Pull-high states.
IOC2	7	I	**See note 1 and 2 below.
IOD0	6	I/O	Port D is an 8-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS type (send current). (Key change, Wake up I/O)
IOD1	5	I/O	
IOD2	4	I/O	
IOD3	3	I/O	
IOD4	2	I/O	
IOD5	1	I/O	
IOD6	18	I/O	
IOD7	17	I/O	**See note 1 and 2 below.

* Refer to SPC Programming Guide for complete information.

****Note:** 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), Open Drain NMOS output (sink).

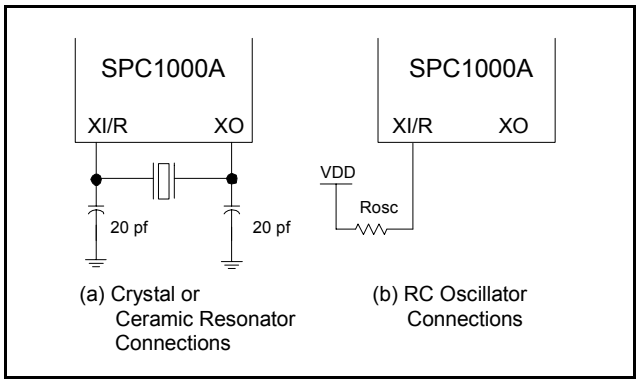
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit microprocessor of SPC1000A is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC1000A is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. Oscillator

The SPC1000A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



(a) Crystal or Ceramic Resonator Connections

(b) RC Oscillator Connections

6.3. Mask Option

The SPC1000A has the following mask option:

- Supports Crystal Resonator or Rosc (with mask option).

6.4. ROM Area

The SPC1000A provides a 1024K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.5. RAM Area

The SPC1000A total RAM consists of 128-bytes (including Stack) at locations from $80 through $FF.

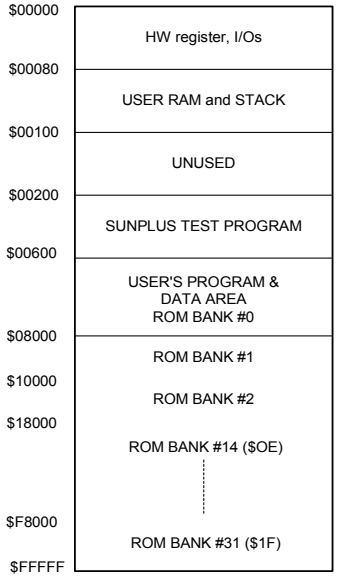
6.6. Map of Memory and I/Os

*I/O PORT:
- PORT IOC $0004
  IOD $0005
- I/O CONFIG $0000
  $0001

*NMI SOURCE:
- INTA (from TIMER A)

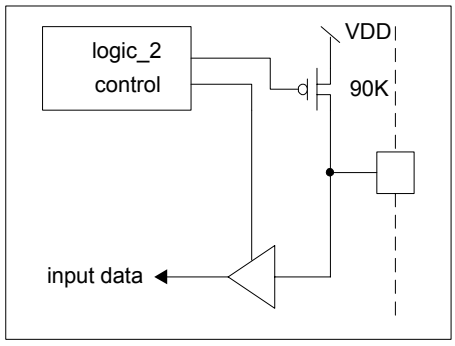
*INT SOURCE:
- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

*MEMORY MAP (From ROM view)

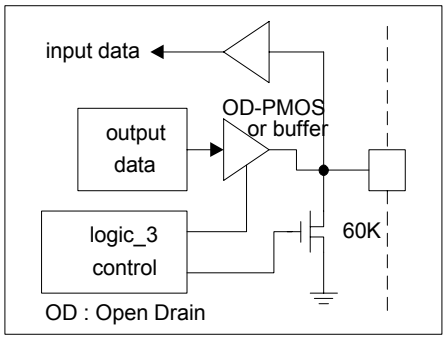


6.7. I/O Port Configuration*

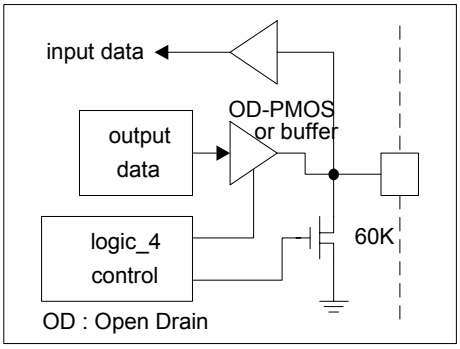
Input IOC port : IOC2 - 1



Input/Output IOD port : IOD3 - 0



Input/Output IOD port : IOD7 - 4



*Values shown are for VDD = 5.0V test conditions only.

6.8. Timer/Counter

The SPC1000A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.9. Speech and Melody

Since the SPC1000A provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the SPC1000A can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPC1000A provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

6.10. Power Savings Mode

The SPC1000A provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the SPC1000A. After the SPC1000A is awakened, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (FIG.1).

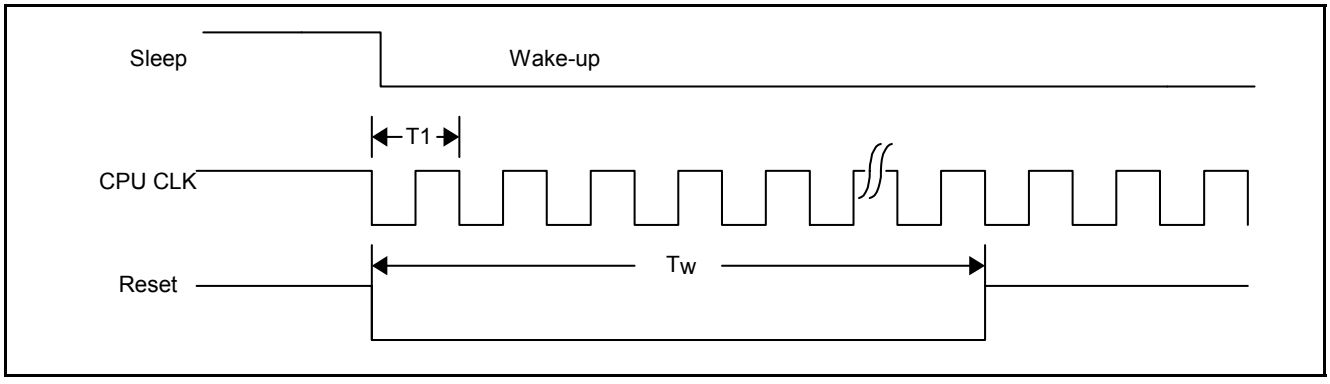


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧ 65536 x T1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
CPU Clock	F_{CPU}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

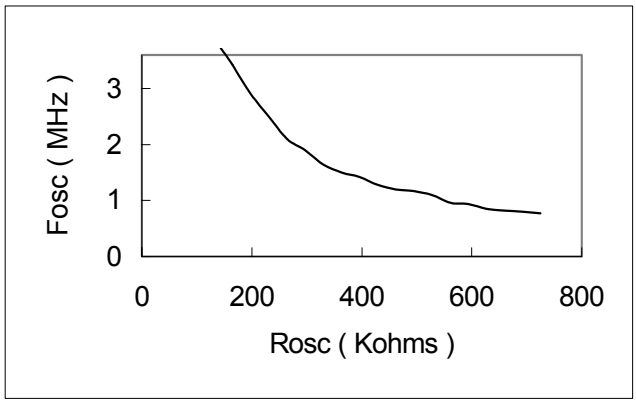
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-0.8	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (IOD)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Output Sink I (IOD)	I_{OL}	2.0	-	-	mA	VDD = 3.0V, V_{OL} = 0.8V
Input Resistor (IOD)	R_{IN}	-	100	-	Kohm	Pull Low, VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

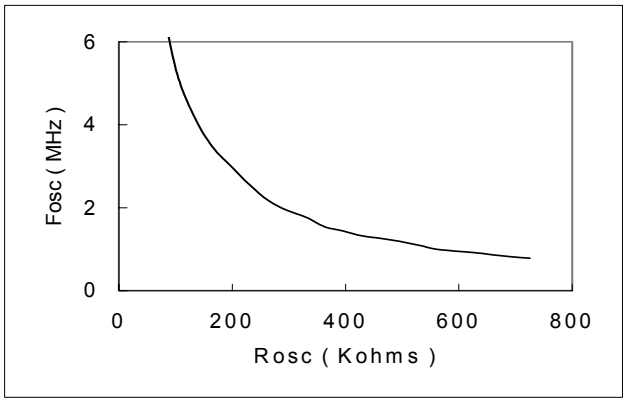
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	5.0	6.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-1.8	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I (IOD)	I_{OH}	-1.0	-	-	mA	VDD = 5.0V, V_{OH} = 4.2V
Output Sink I (IOD)	I_{OL}	4.0	-	-	mA	VDD = 5.0V, V_{OL} = 0.8V
Input Resistor (IOD)	R_{IN}	-	60	-	Kohm	Pull Low, VDD = 5.0V

7.5. The Relationship between the R_{osc} and the F_{osc}

7.5.1. VDD = 3.0V, T_A = 25℃

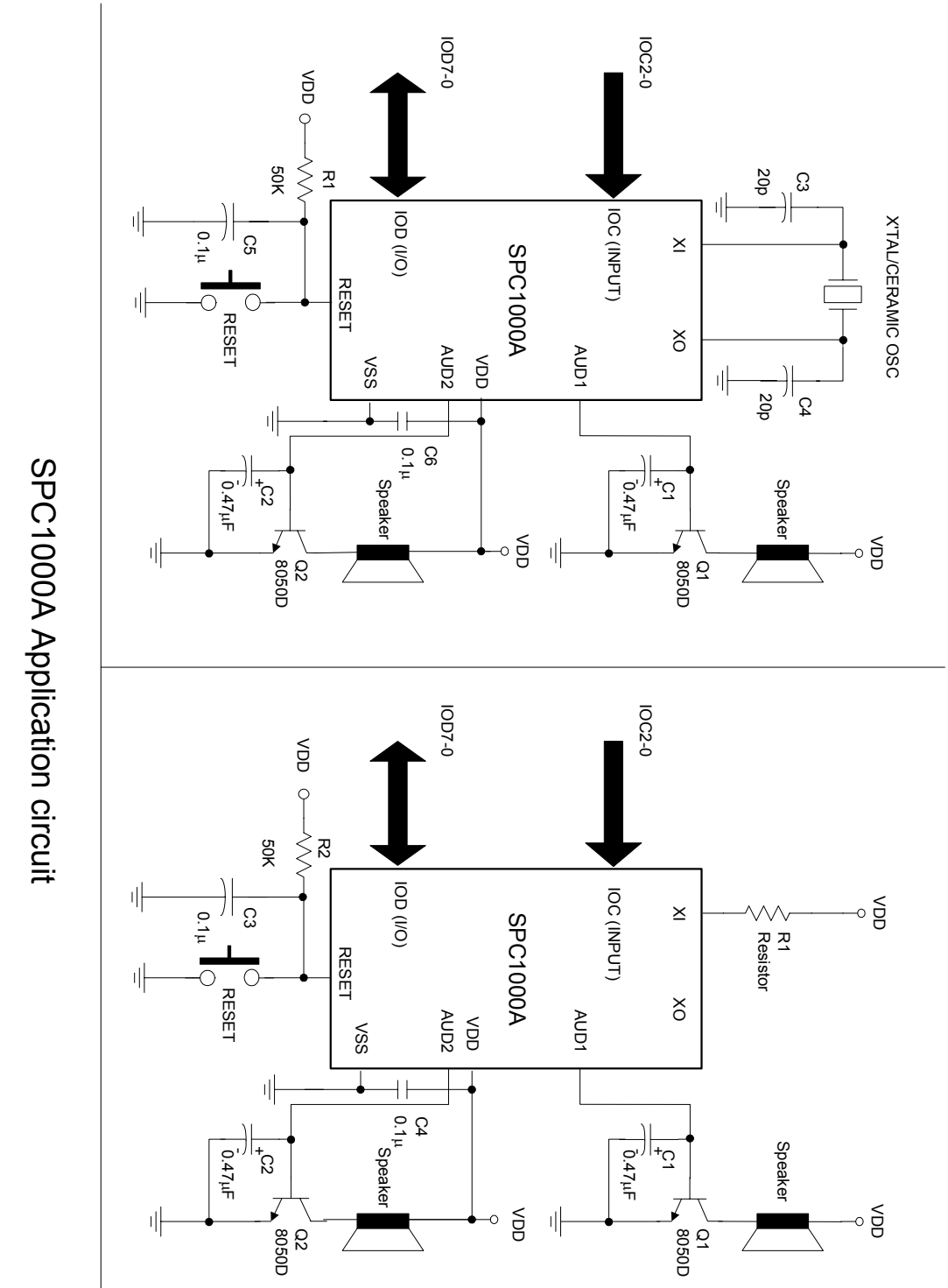


7.5.2. VDD = 4.5V, T_A = 25℃



8. APPLICATION CIRCUITS

8.1. Application Circuit



8.2. Current Mode DAC Speaker Driver

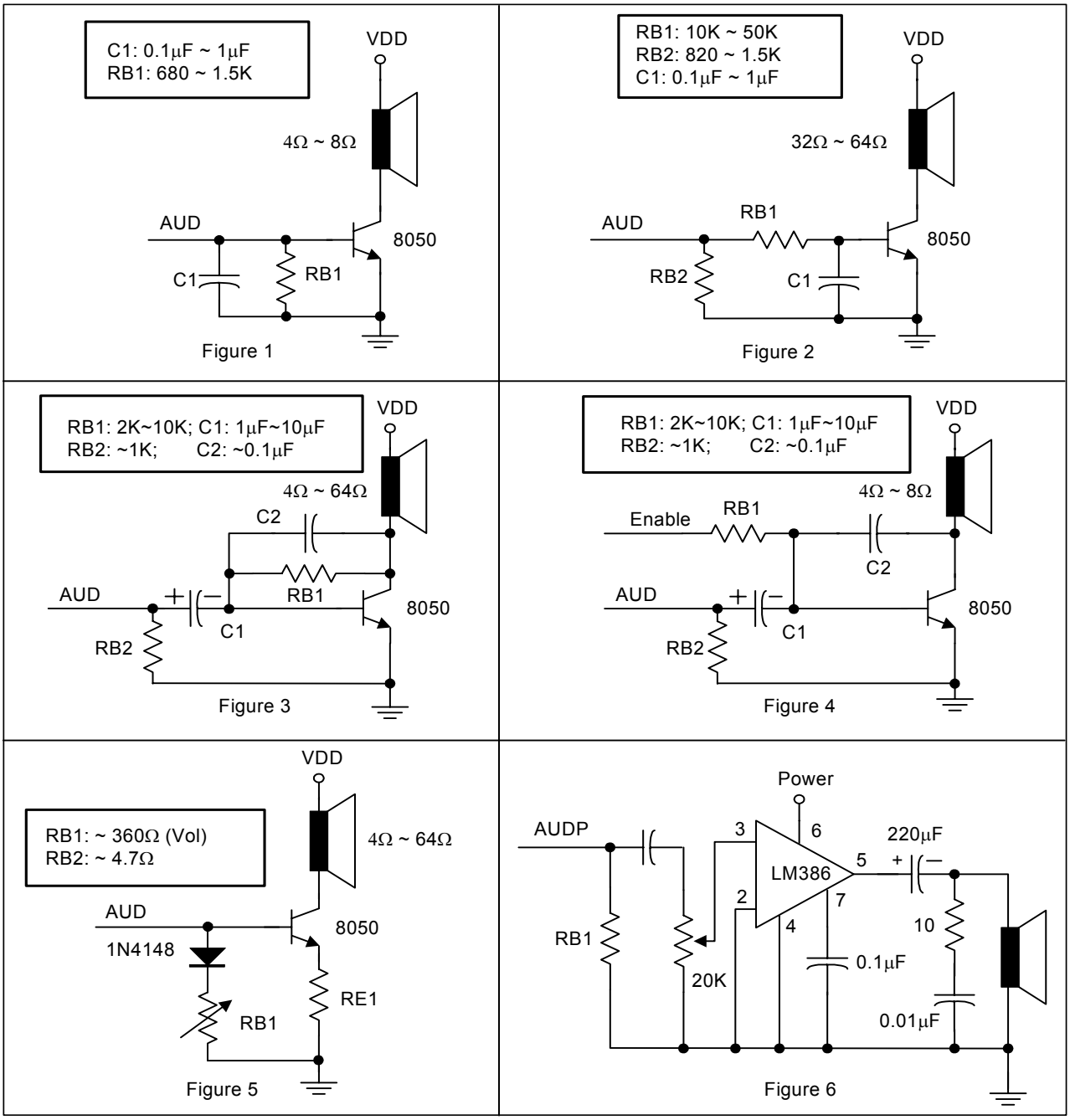


Figure 1:The simplest CKT uses a low impedance speaker. It has high operation current, but the lowest cost.

Figure 2: It is the same as Figure 1 but a high impedance speaker is used.

Figure 3: The CKT contains a low pass filter. It is capable of providing higher speech quality, but it takes higher operation current.

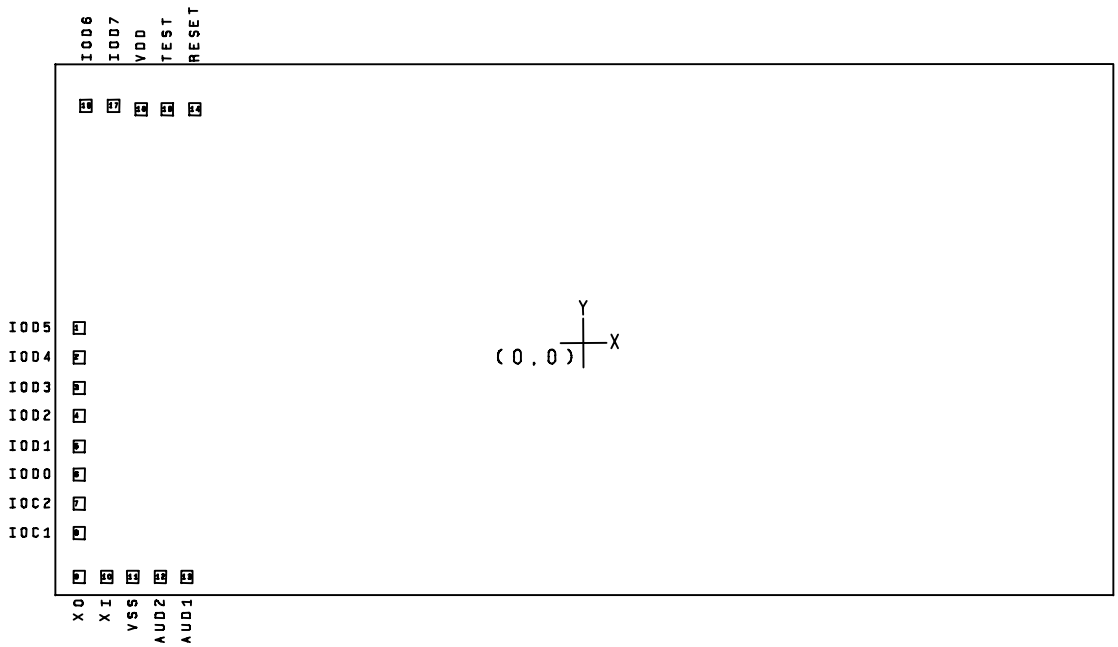
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.

Figure 5: The current mirror mode. It is able to control the volume. In addition, it is more stable and has lower operation current than Figure 1-3.

Figure 6: High quality, low operation current CKT, but more expensive.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 6110μm x 2980μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC1000A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	IOD5	-2869	78
2	IOD4	-2869	-75
3	IOD3	-2869	-235
4	IOD2	-2869	-389
5	IOD1	-2869	-548
6	IOD0	-2871	-701
7	IOC2	-2871	-858
8	IOC1	-2871	-1013
9	XO	-2867	-1247
10	XI	-2715	-1247
11	VSS	-2562	-1247
12	AUD2	-2409	-1247
13	AUD1	-2254	-1247
14	RESET	-2211	1242
15	TEST	-2364	1242
16	VDD	-2517	1242
17	IOD7	-2672	1260
18	IOD6	-2826	1260

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
DEC. 30, 1997	2.0	Original	
DEC. 05, 1997	2.1	1. Add "The Relationship between the R_{OSC} and the F_{OSC}" 2. Renew to a new document format	
JUN. 08, 1998	2.2	1. Add "Note: To ensure that the IC functions properly, bond all VDD and VSS pins." 2. Revise the grammars and spelling in "*GENERAL DESCRIPTION*", "*FEATURES*", "*FUNCTIONAL DESCRIPTIONS*", "*TIMER/COUNTER*", "*SPEECH AND MELODY*", and "*APPLICATION CIRCUITS*"	
NOV. 17, 1998	2.3	Renew to a new document format	
JUN. 16, 2000	2.4	1. Delete IOC2 - 1 output data in the "*I/O PORT CONFIGURATION*" 2. Modify, Audio output driving <laud> typical value: VDD = 5.0V, laud = -1.8mA (old -3mA) VDD = 3.0V, laud = -0.8mA (old -1.5mA)	4 5 - 8
NOV. 08, 2000	2.5	1. VDD = 2.4V - 3.6V for 2-battery application 2. Speech duration @ 6KHz sampling rate with 4-bit ADPCM 3. Approx. 340 sec. speech	
SEP. 14, 2001	2.6	1. Correct chip size 2. Add Note1 and Note2 in the "*9.1 PAD Assignment*" 3. Delete "Note: To ensure that the IC functions properly, bond all VDD and VSS pins." 4. Renew to a new document format	11 11 11