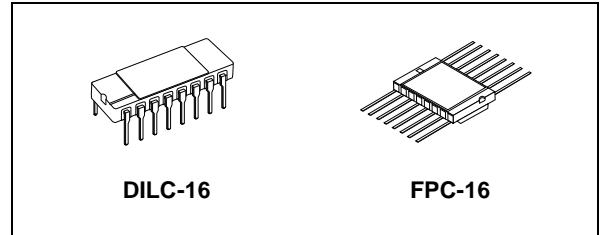


RAD-HARD 8 BIT LATCH/SHIFT REGISTER

- HIGH SPEED:
 $f_{MAX} = 50 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 597
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9306-054

DESCRIPTION

The M54HC597 is an high speed CMOS 8 BIT PIPO SHIFT REGISTER fabricated with silicon gate C²MOS technology.



ORDER CODES

PACKAGE	FM	EM
DILC	M54HC597D	M54HC597D1
FPC	M54HC597K	M54HC597K1

This devices comes in a 16-pin package and consist of an 8-bit storage latch feeding a parallel in, serial out 8-bit shift register. Both the storage register and shift register have positive edge triggered clocks. The shift register also has direct load (from storage) and clear inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

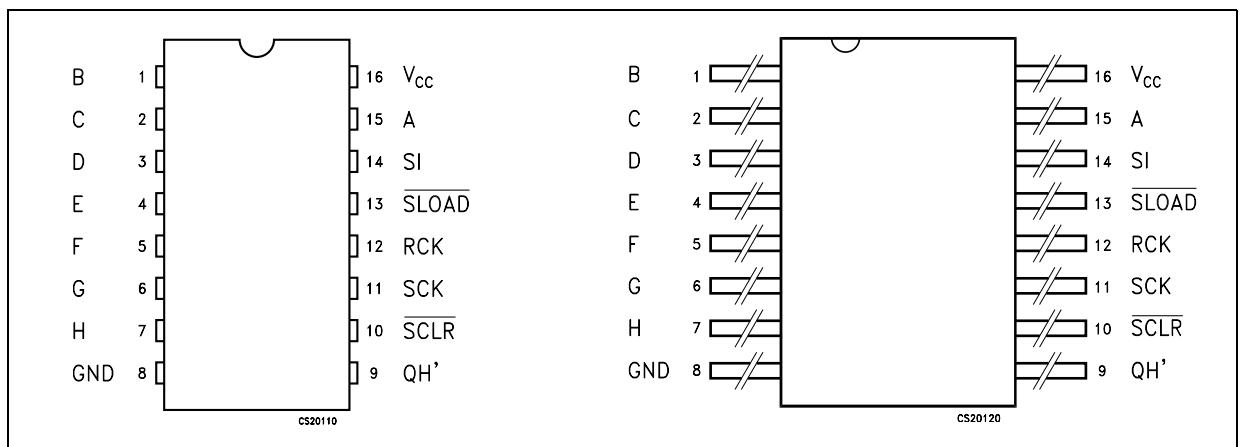


Figure 1: IEC Logic Symbols

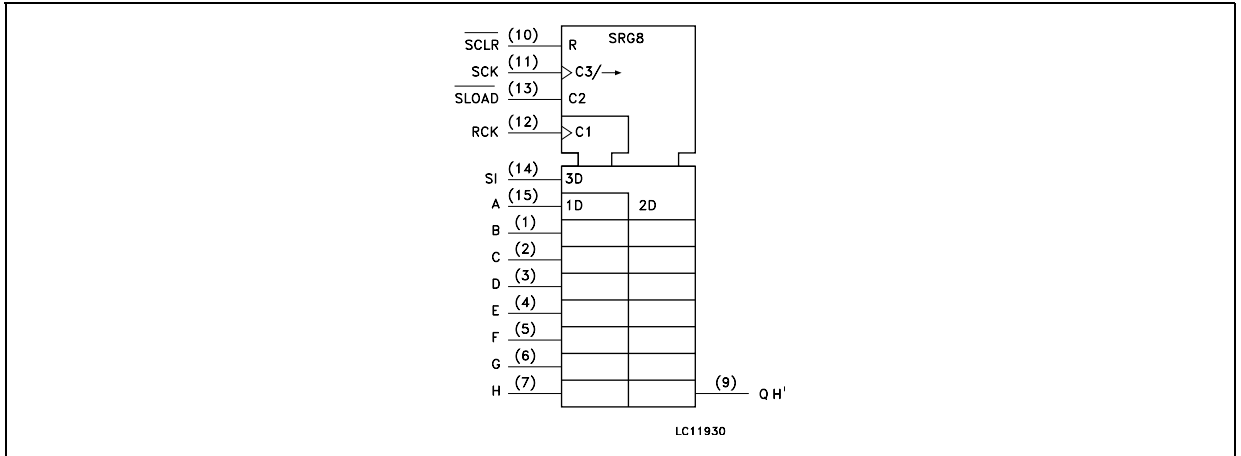


Figure 2: Input And Output Equivalent Circuit

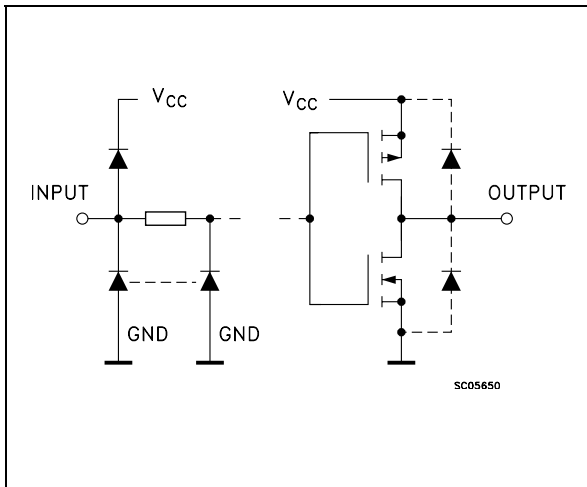


Table 1: Pin Description

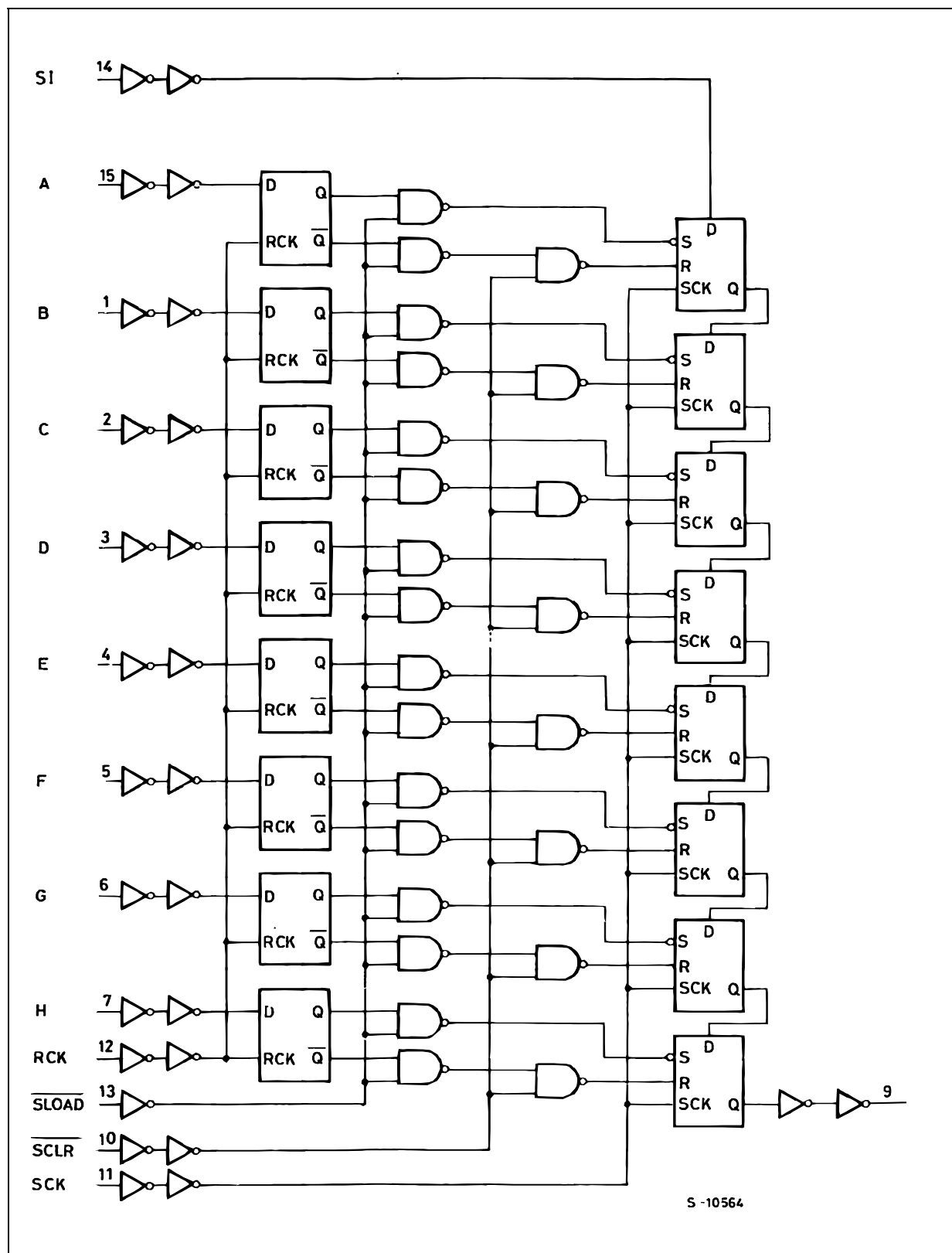
PIN N°	SYMBOL	NAME AND FUNCTION
9	QH'	Serial Data Outputs
10	$\overline{\text{SCLR}}$	Asynchronous Reset Input (Active LOW)
11	SCK	Shift Clock Input (LOW to HIGH Edge-triggered)
12	RCK	Storage Clock Input (LOW to HIGH Edge-triggered)
13	$\overline{\text{SLOAD}}$	Parallel Data Input (Active Low)
10	SI	Serial Data Input
15, 1, 2, 3, 4, 5, 6, 7	A to H	Parallel Data Inputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUTS					OUTPUT
SI	SCK	$\overline{\text{SCLR}}$	$\overline{\text{SLOAD}}$	RCK	
X	X	L	H	X	S.R. IS CLEARED TO "L"
X	X	H	L	X	INPUT REGISTER DATA IS STORED INTO S.R.
L		H	H	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H		H	H	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X		H	H	X	STATE OF S.R. IS NOT CHANGED
X	X	X	X		INPUT DATA ON A ~ H LINE IS STORED INTO INPUT REGISTER
X	X	X	X		STORAGE REGISTER STATE IS NOT CHANGED

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not been used to estimate propagation delays

Figure 4: Timing Chart

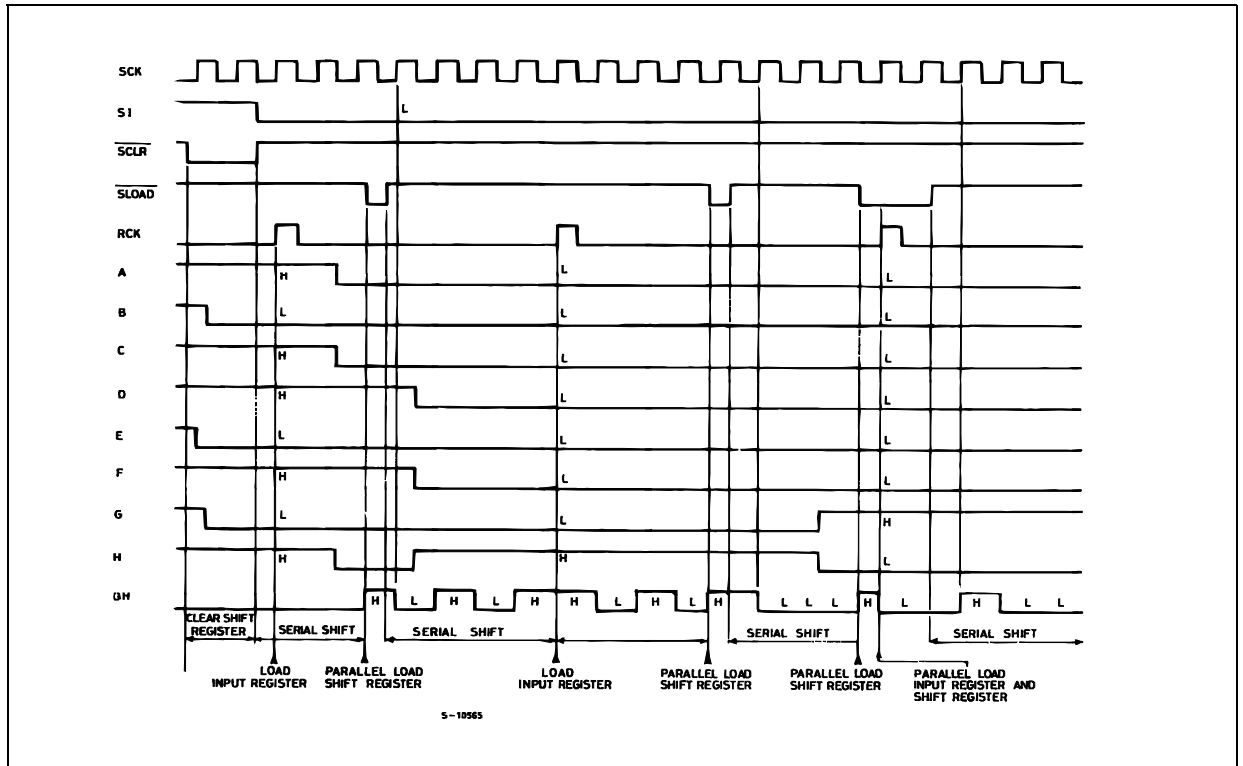


Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	265	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ C$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	$I_O = -20 \mu A$	1.9	2.0		1.9		1.9		V
		4.5	$I_O = -20 \mu A$	4.4	4.5		4.4		4.4		
		6.0	$I_O = -20 \mu A$	5.9	6.0		5.9		5.9		
		4.5	$I_O = -4.0 mA$	4.18	4.31		4.13		4.10		
		6.0	$I_O = -5.2 mA$	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	V
		4.5	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	
		6.0	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	
		4.5	$I_O = 4.0 mA$		0.17	0.26		0.33		0.40	
		6.0	$I_O = 5.2 mA$		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	μA

Table 6: AC Electrical Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

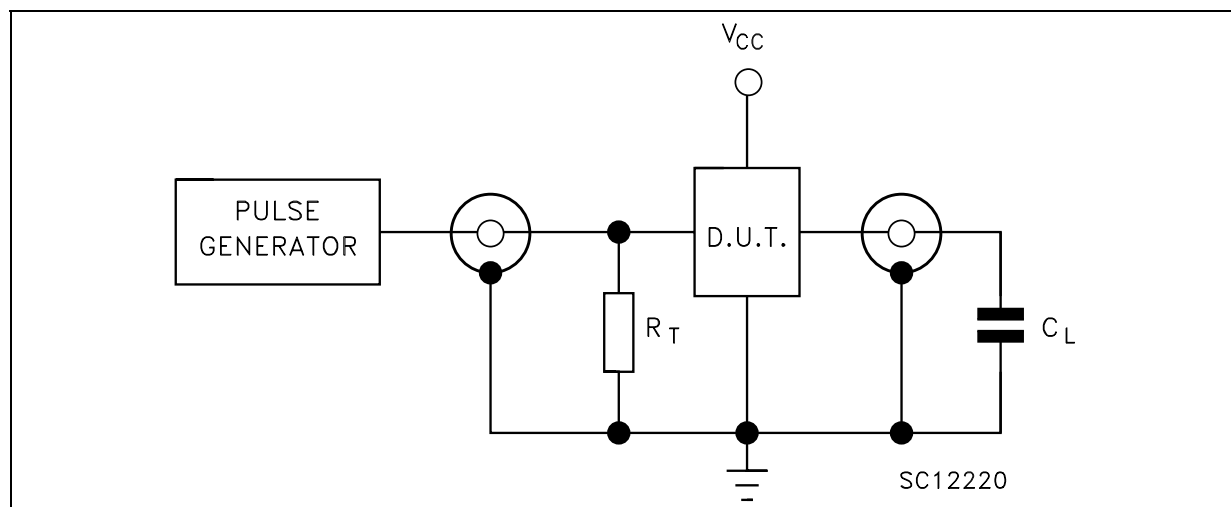
Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK - QH')	2.0			78	145		180		220	ns
		4.5			20	29		36		44	
		6.0			16	25		31		37	
t_{PLH} t_{PHL}	Propagation Delay Time (SCLR - QH')	2.0			90	175		220		265	ns
		4.5			24	35		44		53	
		6.0			20	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (SLOAD - QH')	2.0			80	175		220		265	ns
		4.5			22	35		44		53	
		6.0			18	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - QH')	2.0	SLOAD = "L"		112	210		265		315	ns
		4.5			30	42		53		63	
		6.0			24	36		45		54	
f_{MAX}	Maximum Clock Frequency	2.0		6.0	12		4.8		4.0		MHz
		4.5		30	48		24		20		
		6.0		35	50		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (SCK, RCK)	2.0			20	75		95		110	ns
		4.5			7	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (SCLR, SLOAD)	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time (RCK - SLOAD)	2.0			48	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_s	Minimum Set-up Time (SI, SCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_s	Minimum Set-up Time (PI, RCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			12	75		95		115	ns
		4.5			4	15		19		23	
		6.0			3	13		16		20	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			60						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Table 8: Test Circuit



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5: Waveform - Minimum Pulse Width, Propagation Delay Time (f=1MHz; 50% duty cycle)

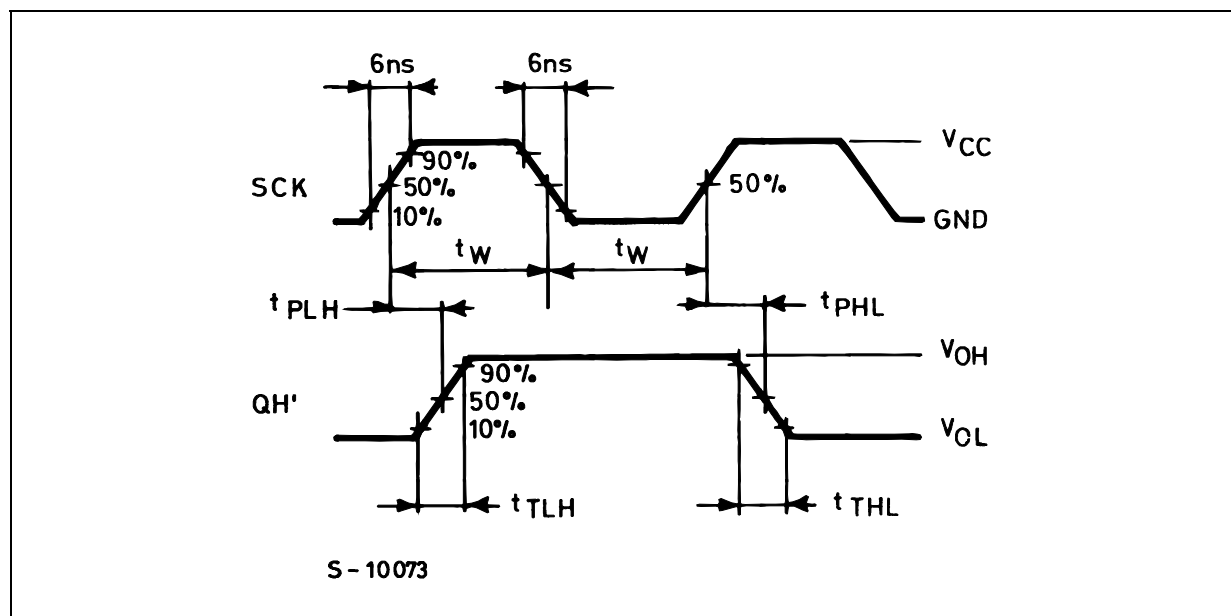


Figure 6: Waveform - Minimum Pulse Width, Propagation Delay Time (f=1MHz; 50% duty cycle)

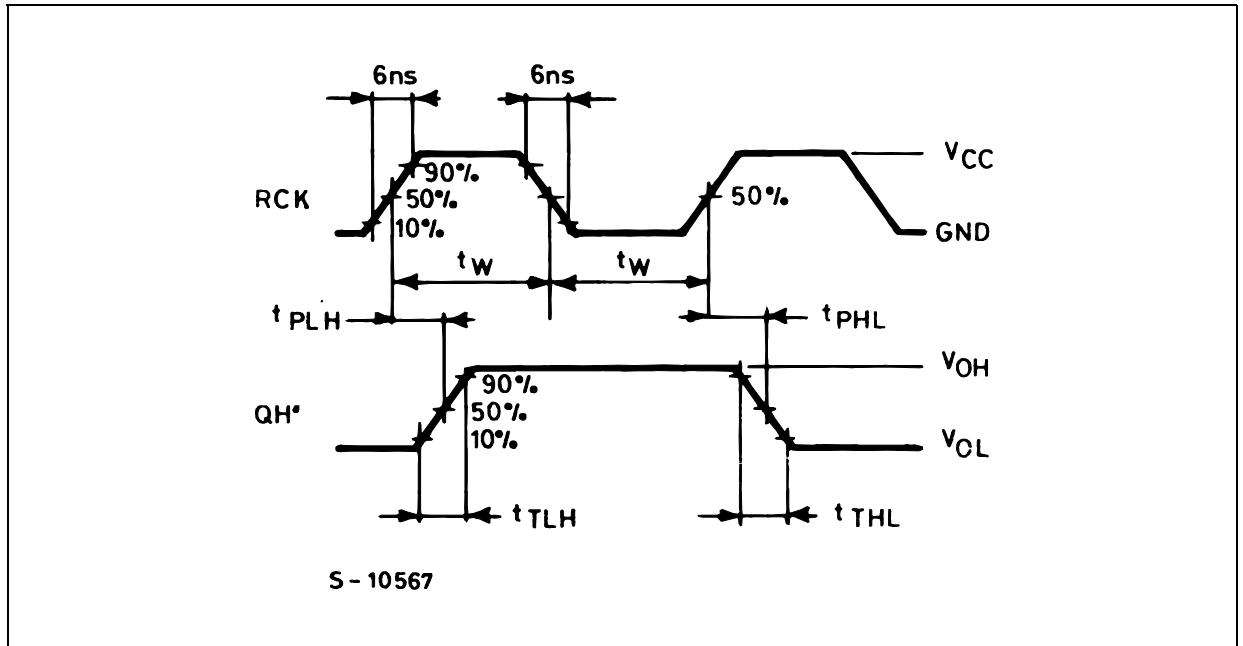


Figure 7: Waveform - Minimum Pulse Width And Removal Time (f=1MHz; 50% duty cycle)

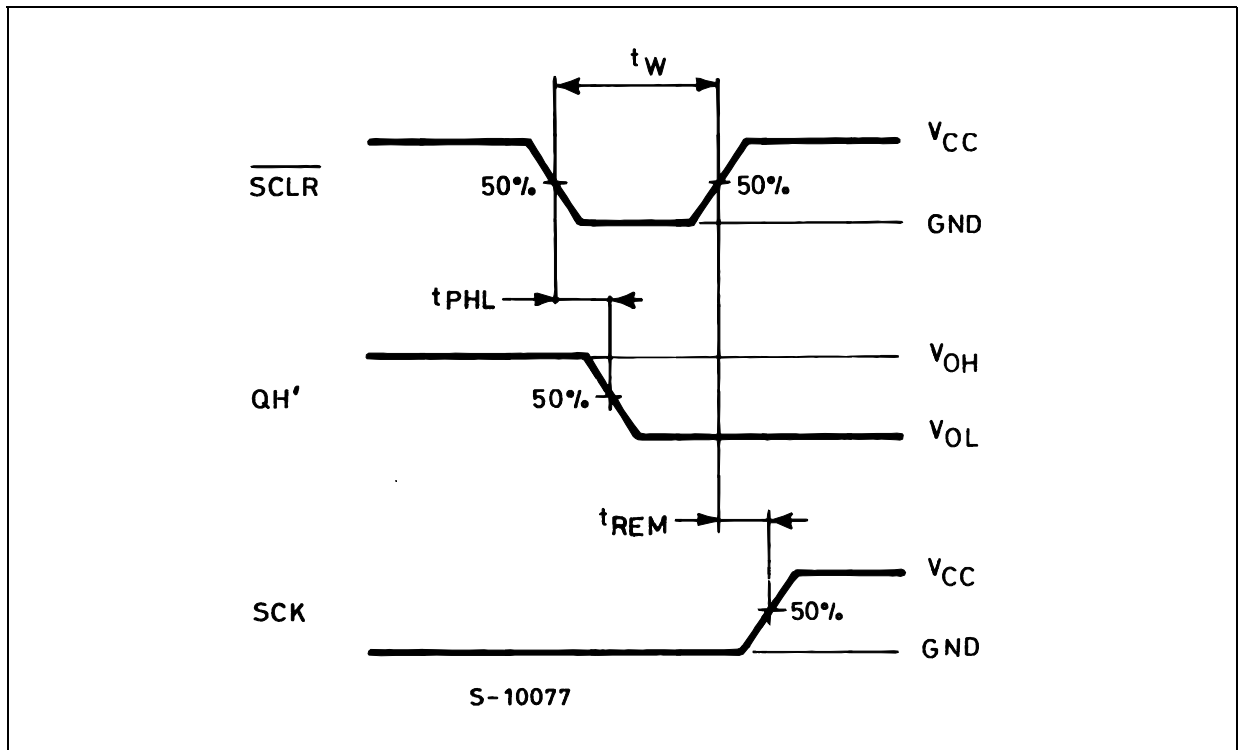


Figure 8: Waveform - Minimum Setup And Hold Time ($f=1\text{MHz}$; 50% duty cycle)

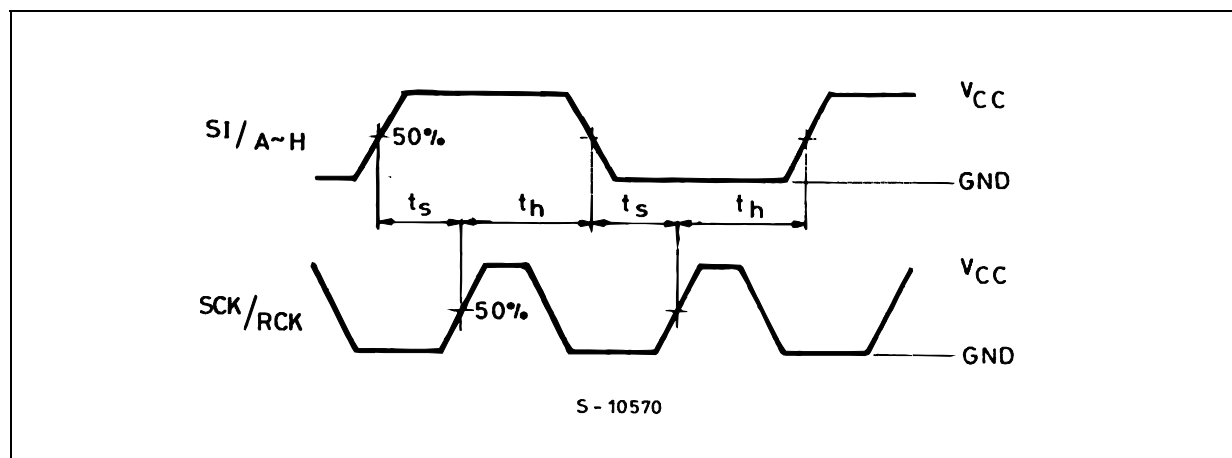


Figure 9: Waveform - Propagation Delay, Minimum Pulse Width, Removal Time ($f=1\text{MHz}$; 50% duty cycle)

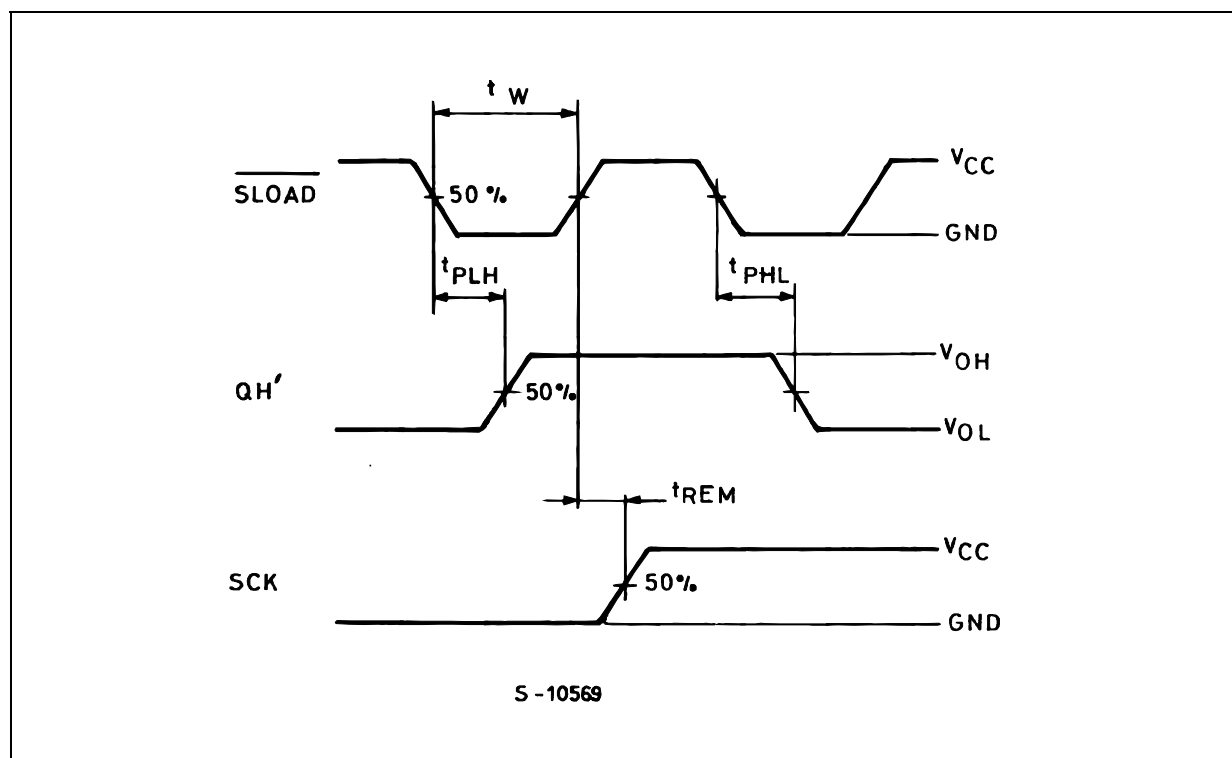
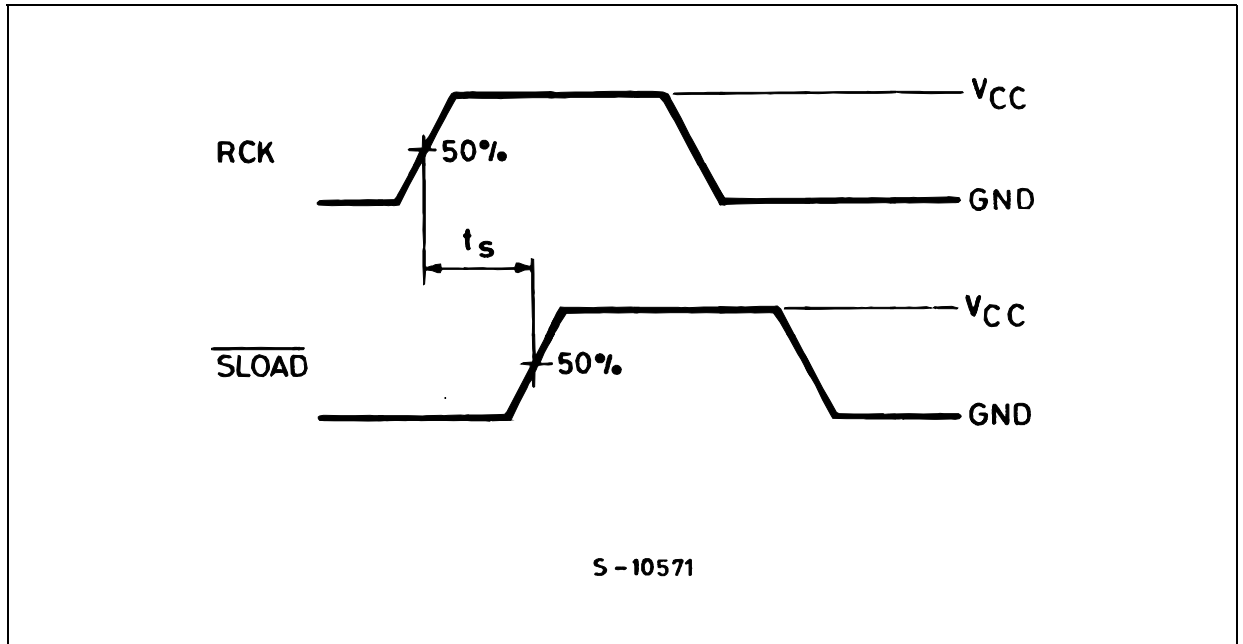
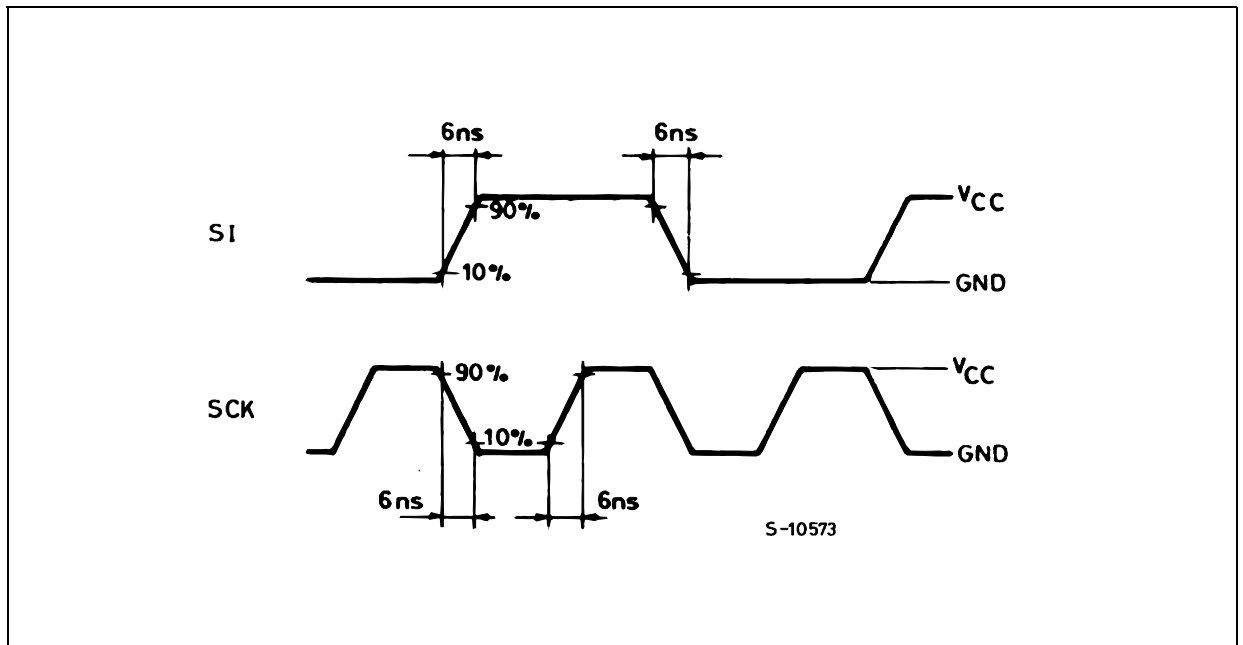
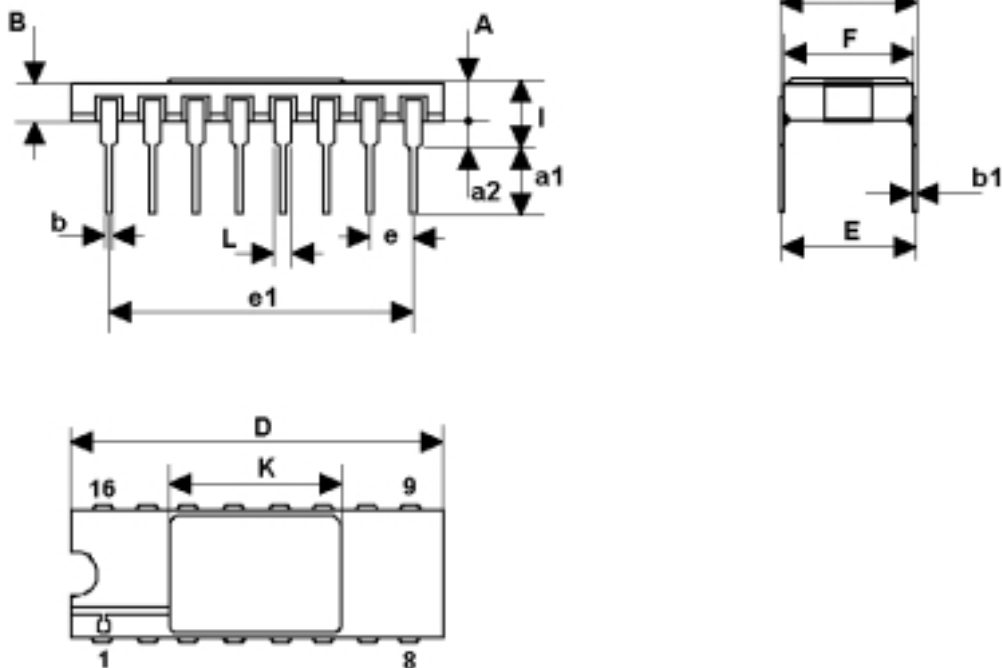


Figure 10: Waveform - Minimum Setup Time ($f=1\text{MHz}$; 50% duty cycle)Figure 11: Waveform - Input Waveform ($f=1\text{MHz}$; 50% duty cycle)

DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	17.65	17.78	17.90	0.695	0.700	0.705
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



0056437F

Table 9: Revision History

Date	Revision	Description of Changes
01-Jun-2004	1	First Release

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