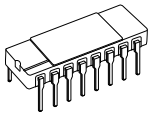
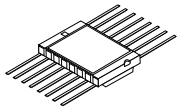
M54HC193

RAD-HARD SYNCHRONOUS UP/DOWN BINARY COUNTER

- HIGH SPEED: f_{MAX}=55MHz (TYP.) at V_{CC}=6V
- LOW POWER DISSIPATION: I_{CC} =4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 193
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9204-065



DILC-16



FPC-16

ORDER CODES

PACKAGE	FM	EM
DILC	M54HC193D	M54HC193D1
FPC	M54HC193K	M54HC193K1

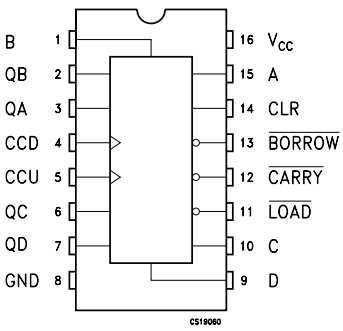
DESCRIPTION

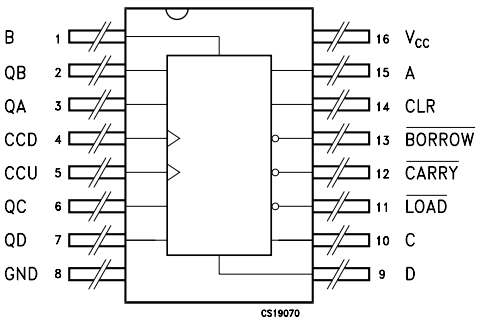
The M54HC193 is an high speed CMOS SYNCRONOUS UP/DOWN BINARY COUNTERS fabricated with silicon gate C^2MOS technology.

The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the $\overline{LOAD}$ input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the clear input. All 4 internal stages are set to low independently of either COUNT input. Both a $\overline{BORROW}$ and $\overline{CARRY}$ output are provided to enable cascading of both up and down counting functions. The $\overline{BORROW}$ output produces a negative going pulse when the counter underflows and the $\overline{CARRY}$ outputs a pulse when the counters overflows. The counter can be cascaded by connection the $\overline{CARRY}$ and $\overline{BORROW}$ outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

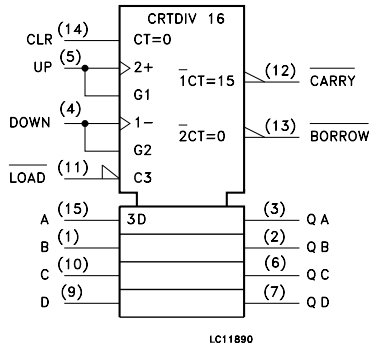
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

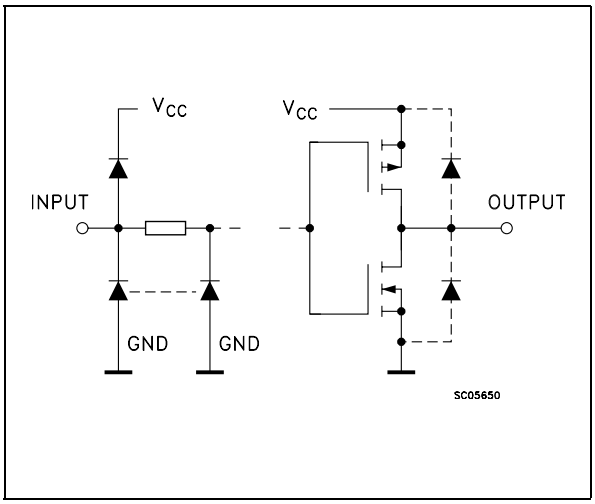




IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

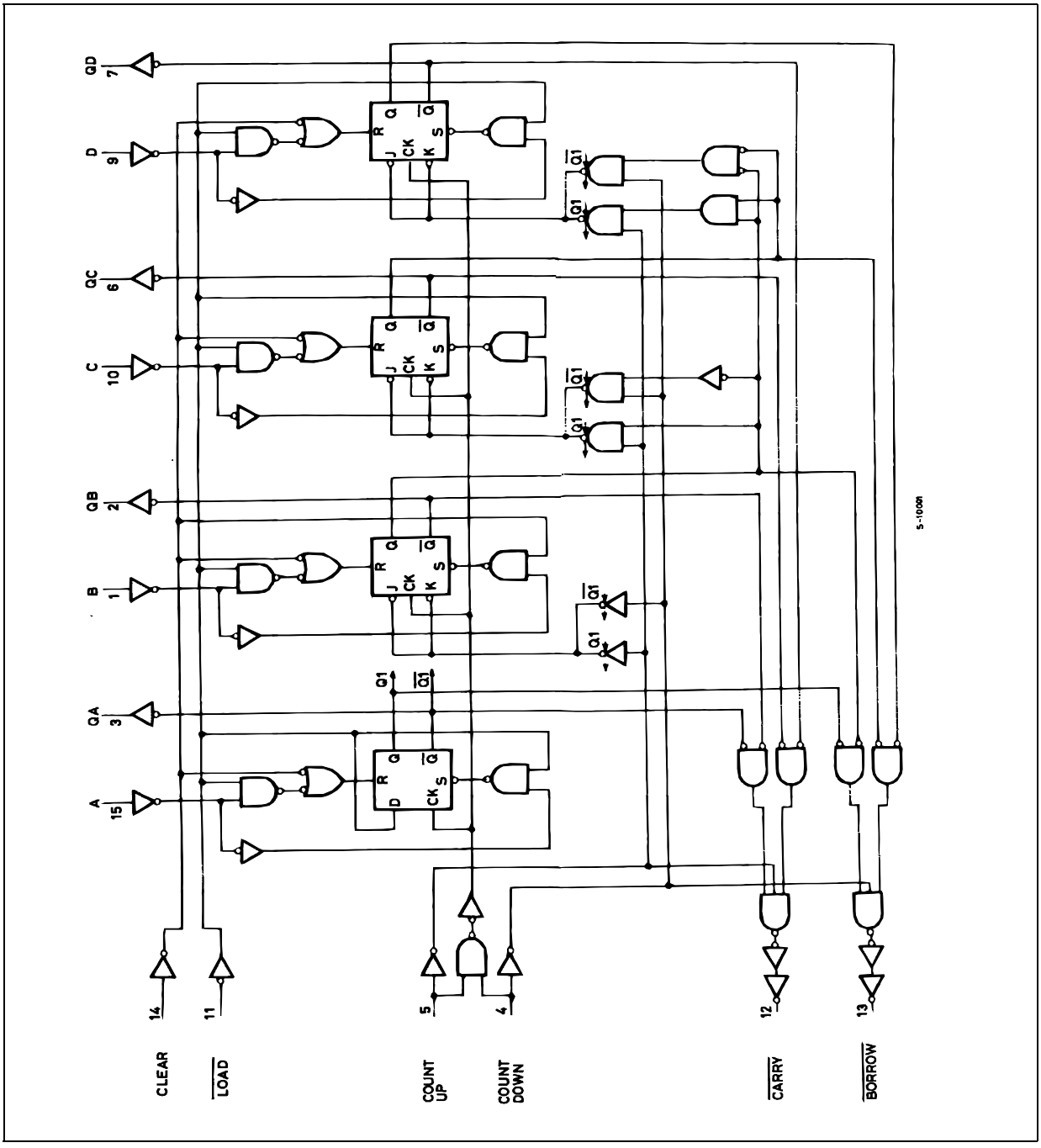
PIN N°	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	QA to QD	Flip-Flop Outputs
4	CCD	Count Down Clock Input
5	CCU	Count Up Clock Input
11	$\overline{\text{LOAD}}$	Asynchronous Parallel Load Input (Active LOW)
12	$\overline{\text{CARRY}}$	Count Up (Carry) Output (Active LOW)
13	$\overline{\text{BORROW}}$	Count Down (Borrow) Output (Active LOW)
14	CLR	Asynchronous Reset Input (Active High)
15, 1, 10, 9	A to D	Data Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

COUNT UP	COUNT DOWN	$\overline{\text{LOAD}}$	CLEAR	FUNCTION
⌐¯	H	H	L	COUNT UP
¯⌐	H	H	L	NO COUNT
H	⌐¯	H	L	COUNT DOWN
H	¯⌐	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

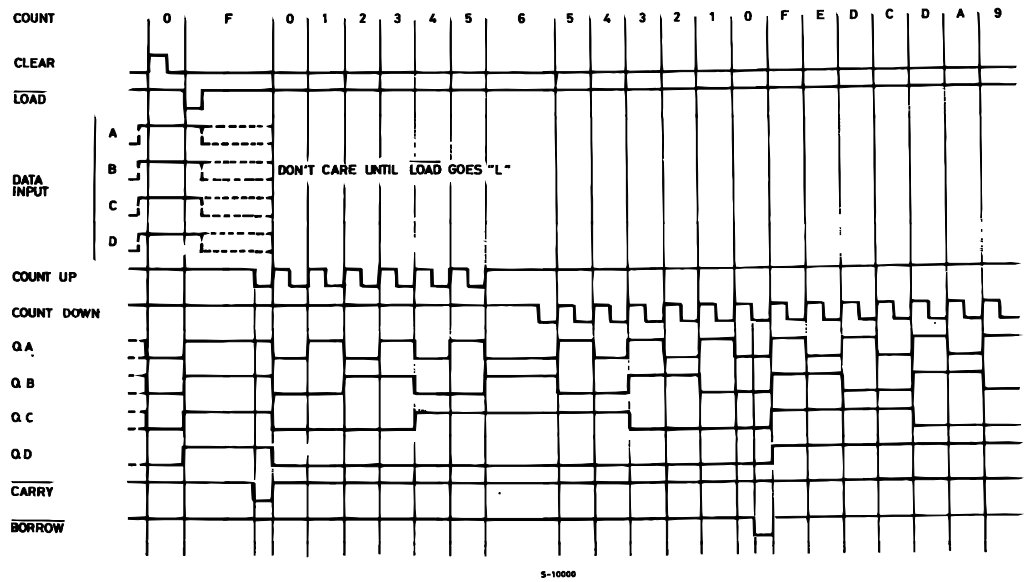
X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (COUNT UP, DOWN - Q)	2.0			65	190		240		285	ns
		4.5			20	38		48		57	
		6.0			16	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (COUNT UP - $\overline{\text{CARRY}}$)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (COUNT DOWN - $\overline{\text{BORROW}}$)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - Q)	2.0			85	220		275		330	ns
		4.5			25	44		55		66	
		6.0			20	37		47		56	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - $\overline{\text{CARRY}}$)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - $\overline{\text{BORROW}}$)	2.0			110	250		315		375	ns
		4.5			31	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q)	2.0			80	190		240		285	ns
		4.5			25	38		48		57	
		6.0			20	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - $\overline{\text{CARRY}}$)	2.0			120	250		315		375	ns
		4.5			34	50		63		75	
		6.0			28	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - $\overline{\text{BORROW}}$)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PHL}	Propagation Delay Time (CLEAR -Q)	2.0			100	225		280		340	ns
		4.5			30	45		56		68	
		6.0			25	38		48		58	
t_{PLH}	Propagation Delay Time (CLEAR -$\overline{\text{CARRY}}$)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
t_{PHL}	Propagation Delay Time (CLEAR - $\overline{\text{BORROW}}$)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
f_{MAX}	Maximum Clock Frequency	2.0		5	12		4		3.4		MHz
		4.5		25	48		20		17		
		6.0		30	55		24		20		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (COUNT UP/ DOWN)	2.0			34	100		125		150	ns
		4.5			9	20		25		30	
		6.0			7	17		21		26	

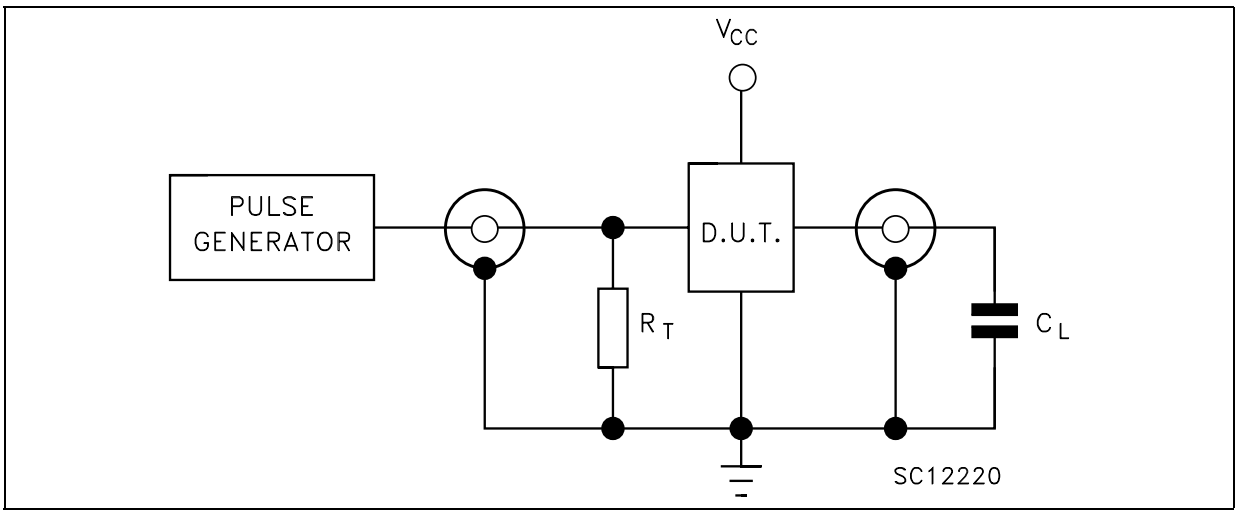
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(L)}$	Minimum Pulse Width (LOAD)	2.0			34	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			40	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_s	Minimum Set-up Time ($\overline{DATA}$ - $\overline{LOAD}$)	2.0			30	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{LOAD}$)	2.0			6	50		65		75	ns
		4.5			2	10		13		15	
		6.0			2	9		11		13	
t_{REM}	Minimum Removal Time (CLEAR)	2.0			14	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			67						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

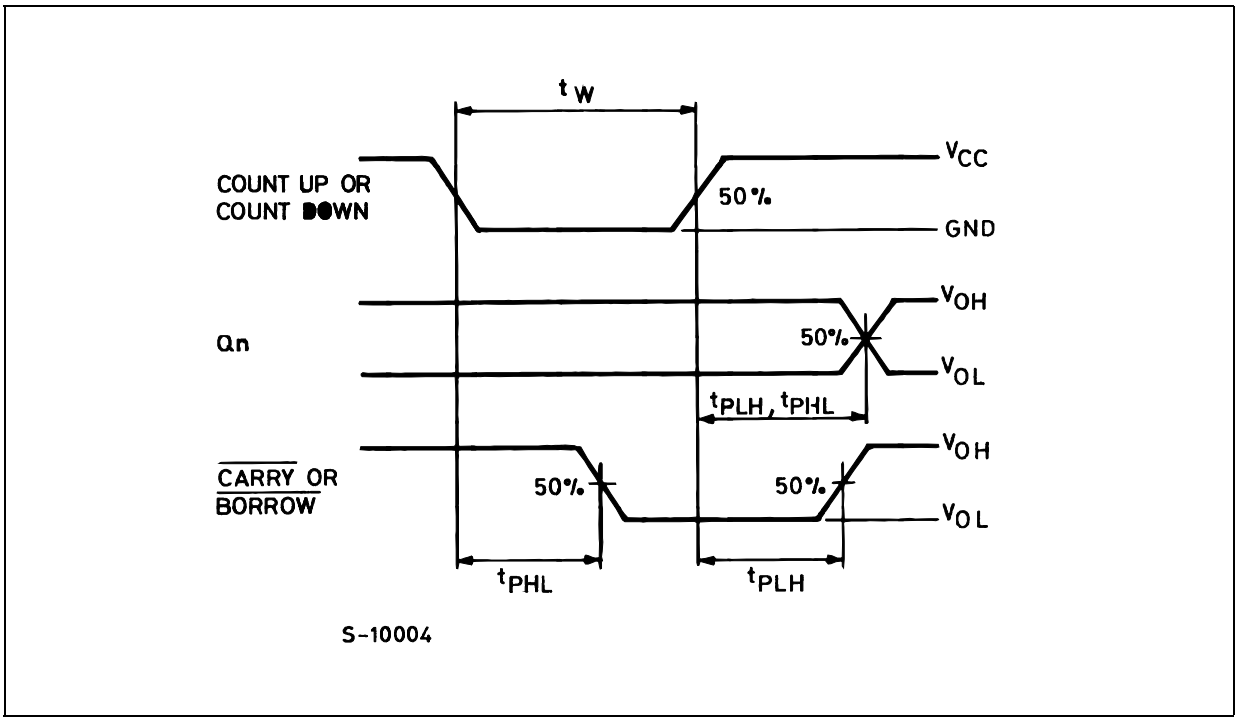
TEST CIRCUIT



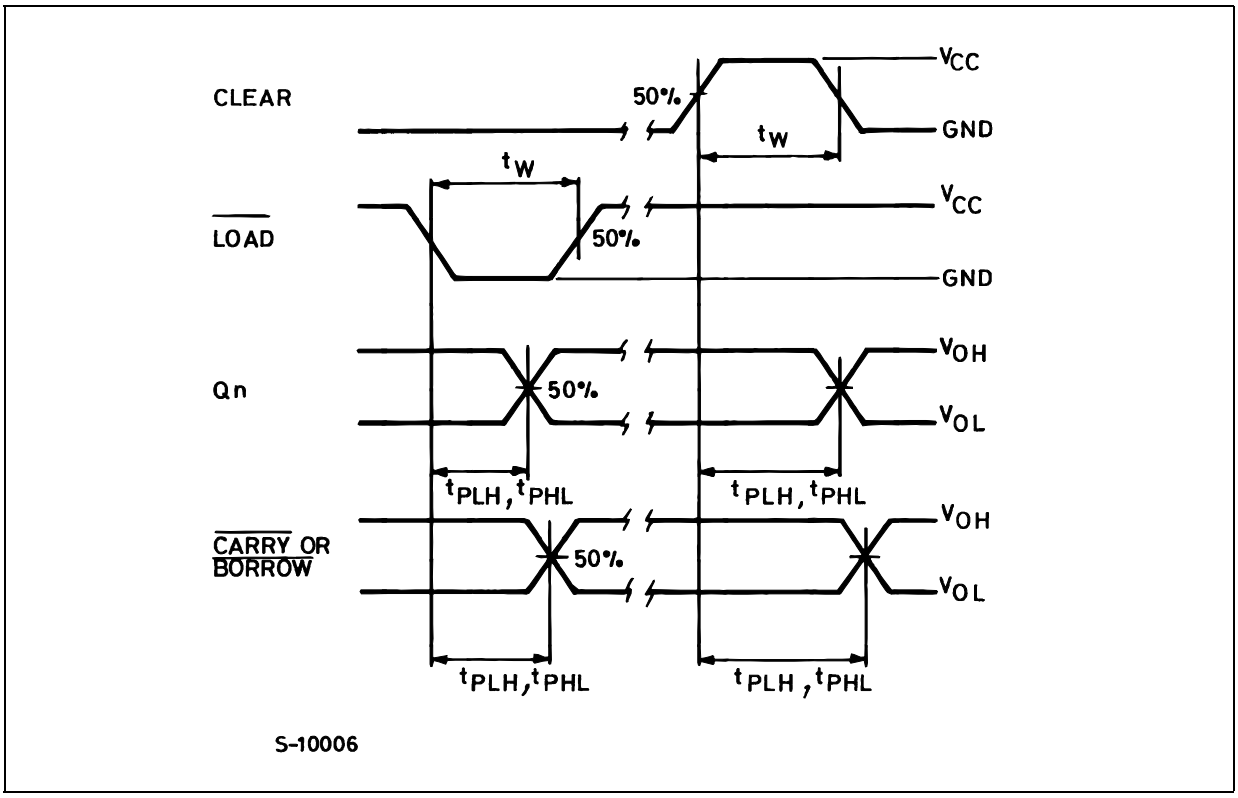
C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (COUNT UP OR DOWN)

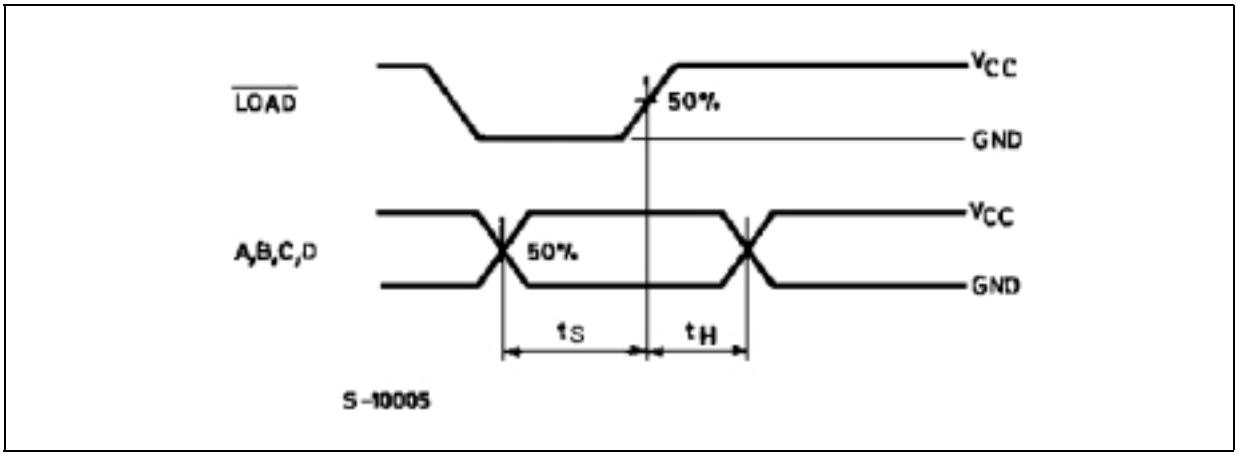
(f=1MHz; 50% duty cycle)



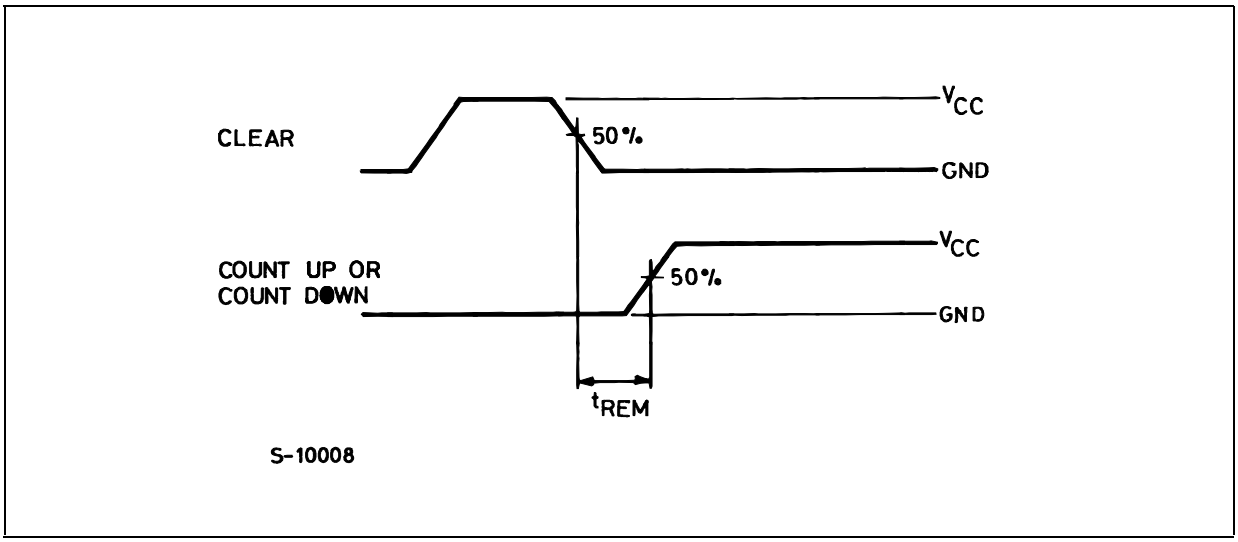
WAVEFORM 2: PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (CLEAR, $\overline{LOAD}$)
(f=1MHz; 50% duty cycle)



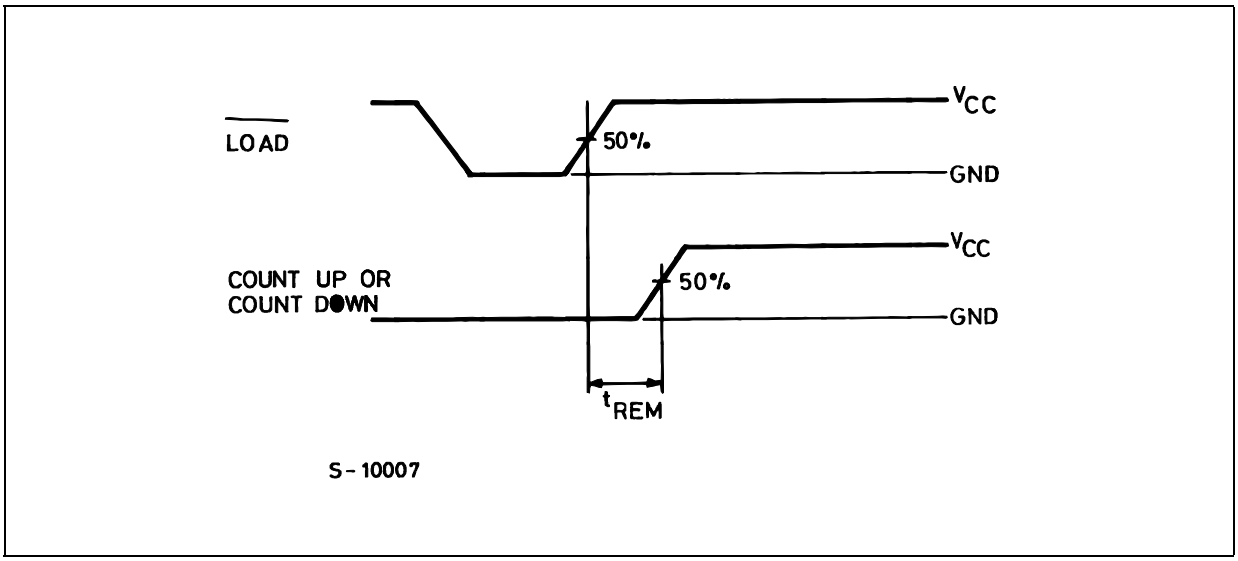
WAVEFORM 3: SETUP AND HOLD TIME (A, B, C, D to $\overline{LOAD}$) (f=1MHz; 50% duty cycle)



WAVEFORM 4: MINIMUM REMOVAL TIME (COUNT UP OR DOWN TO CLEAR)
(f=1MHz; 50% duty cycle)

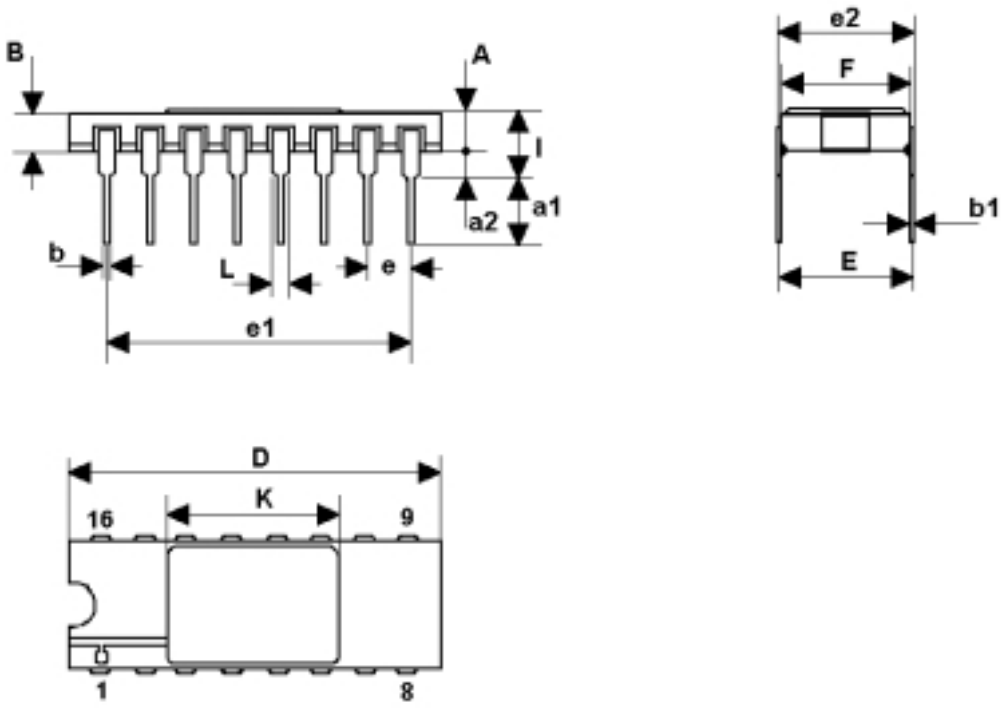


WAVEFORM 5:MINIMUM REMOVAL TIME (COUNT UP OR DOWN TO $\overline{\text{LOAD}}$)
(f=1MHz; 50% duty cycle)



DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	17.65	17.78	17.90	0.695	0.700	0.705
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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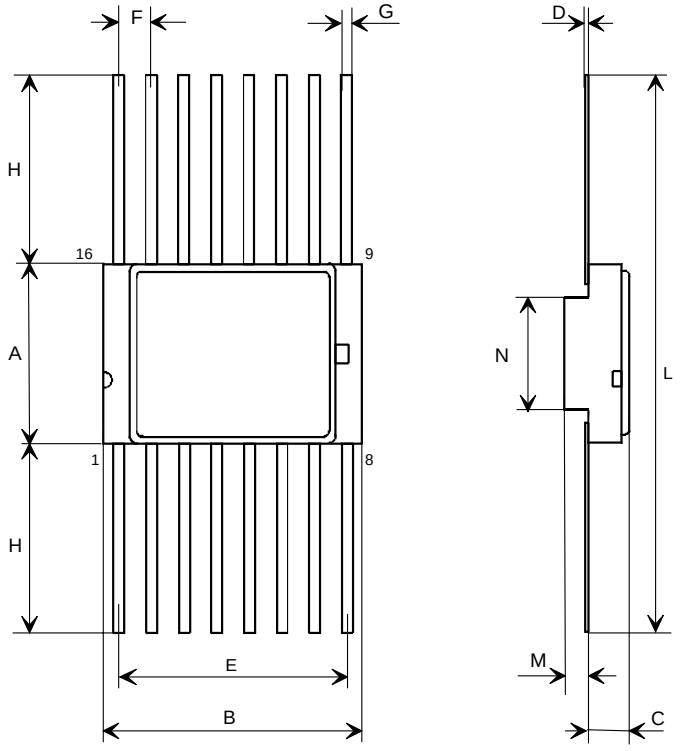
FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	



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