Single Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier

Preliminary Technical Data

AD8223

FEATURES

Gain set with 1 resistor per amplifier
- **Gain = 5 to 1000**

Inputs
- **Voltage range to 150 mV below negative rail**
- **25 nA maximum input bias current**
- **30 nV/√Hz, RTI noise @ 1 kHz**

Power supplies
- **Dual supply: ±2.5V to ±12.5**
- **Single supply: 3V to 25V**
- **600 μA maximum supply current**

APPLICATIONS

Low power medical instrumentation
Transducer interface
Thermocouple amplifiers
Industrial process controls
Difference amplifiers
Low power data acquisition

CONNECTION DIAGRAM

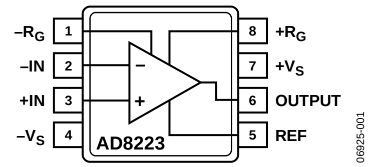

Figure 1. 8-Lead SOIC (R) and 8-Lead MSOP SOIC (RM) Packages

GENERAL DESCRIPTION

The AD8223 is an integrated single-supply instrumentation amplifier that delivers rail-to-rail output swing on a single supply (+3.0 V to +25 V supplies). The AD8223 offers superior user flexibility by allowing single-gain set resistor programming, and conforming to the 8-lead industry standard pinout configuration.

With no external resistor, the AD8223 is configured for G = 5 and with an external resistor, the AD8223 can be programmed for gains up to 1000.

The AD8223 holds errors to a minimum by providing superior ac CMRR that increases with increasing gain. Line noise, as well as line harmonics, is rejected because the CMRR remains constant up to 200 Hz. The AD8223 has a wide input common-mode range and can amplify signals that have a common-mode voltage 150 mV below ground. Although the design of the AD8223 is optimized to operate from a single supply, the AD8223 still provides superior performance when operated from a dual voltage supply (±2.5 V to ±12.5 V).

Low power consumption (1.5 mW at 3 V), wide supply voltage range, and rail-to-rail output swing make the AD8223 ideal for battery-powered applications. The rail-to-rail output stage maximizes the dynamic range when operating from low supply voltages. The AD8223 replaces discrete instrumentation amplifier designs and offers superior linearity, temperature stability and reliability in a minimum of space.

Rev. PrA

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REVISION HISTORY

SPECIFICATIONS

SINGLE SUPPLY

T_A = 25°C, single supply, V_S = +5 V, and R_L = 10 kΩ, unless otherwise noted.

Table 1

Parameter	Conditions	AD8223A Min	AD8223A Typ	AD8223A Max	AD8223B Min	AD8223B Typ	AD8223B Max	Unit
COMMON MODE REJECTION RATIO								
DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to 3 V							
G = 5		74			86			dB
G = 10		80			92			dB
G = 100		88			100			dB
G = 1000		88			100			dB
NOISE								
Voltage Noise, 1 kHz								
G = 5			50			50		nV/√Hz
G = 1000			30			30		nV/√Hz
RTI, 0.1 Hz to 10 Hz								
G = 5			3.0			3.0		µV p-p
G = 1000			1.5			1.5		µV p-p
Current Noise, 1 kHz			100			100		fA/√Hz
0.1 Hz to 10 Hz			1.5			1.5		pA p-p
VOLTAGE OFFSET	Total RTI Error = $V_{OSI} + V_{OSO}/G$							
Input Offset, V_{OSI}				400			200	µV
Average TC				5			3	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Average TC				15			10	µV/°C
Offset Referred to Input vs. Supply (PSR)								
G = 5		80			90			dB
G = 10		86			96			dB
G = 100		90			100			dB
G = 1000		90			100			dB
INPUT CURRENT								
Input Bias Current			17	25		17	25	nA
Over Temperature				27.5			27.5	nA
Average Temperature Coefficient			25			25		pA/°C
Input Offset Current			0.25	2		0.25	2	nA
Over Temperature				2.5			2.5	nA
Average Temperature Coefficient			5			5		pA/°C
DYNAMIC RESPONSE								
Small Signal –3 dB Bandwidth								
G = 5			200			200		kHz
G = 10			190			190		kHz
G = 100			75			75		kHz
G = 1000			8			8		kHz
Slew Rate			0.3			0.3		V/µs

Parameter	Conditions	AD8223A Min	AD8223A Typ	AD8223A Max	AD8223B Min	AD8223B Typ	AD8223B Max	Unit
Settling Time to 0.01%	Step size = 3.5 V							
G = 5								µs
G = 100								µs
G = 1000								µs
GAIN	G = 5 + (80 k/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error[1]	V_{OUT} = 0.05 V to 4.5 V							
G = 5			0.03	0.15		0.03	0.1	%
G = 10			0.10	1		0.10	0.5	%
G = 100			0.10	1		0.10	0.5	%
G = 1000			0.10	1		0.10	0.5	%
Nonlinearity	V_{OUT} = 0.05 V to 4.5 V							
G = 5 to 1000			50			50		ppm
Gain vs. Temperature								
G = 5			5	10		5	10	ppm/°C
G > 5[1]			50			50		ppm/°C
INPUT								
Input Impedance								
Differential			2‖2			2‖2		GΩ‖pF
Common-Mode			2‖2			2‖2		GΩ‖pF
Input Voltage Range[2]		$(-V_S) - 0.15$		$(+V_S) - 1.5$	$(-V_S) - 0.15$		$(+V_S) - 1.5$	V
OUTPUT								
Output Swing	R_L = 10 kΩ to ground	+0.01		$(+V_S) - 0.5$	+0.01		$(+V_S) - 0.5$	V
	R_L = 100 kΩ to ground	+0.01		$(+V_S) - 0.2$	+0.01		$(+V_S) - 0.2$	V
REFERENCE INPUT								
R_{IN}			60	±20%		60	±20%	kΩ
I_{IN}	$V_{IN}+$, V_{REF} = 0		+50	+60		+50	+60	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0002			1 ± 0.0002		V
POWER SUPPLY								
Operating Range		+3.0		+25	+3.0		+25	V
Quiescent Current				550			550	µA
TEMPERATURE RANGE								
For Specified Performance		-40		+85	−40		+85	°C

[1] Does not include effects of external resistor RG.
[2] One input grounded. G = 1.

DUAL SUPPLY

T_A = 25°C, dual supply, V_S = ±12 V, and R_L = 10 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	AD8223A Min	AD8223A Typ	AD8223A Max	AD8223B Min	AD8223B Typ	AD8223B Max	Unit
COMMON MODE REJECTION RATIO								
DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to 10 V							
G = 5		74			86			dB
G = 10		80			92			dB
G = 100		88			100			dB
G = 1000		88			100			dB
NOISE								
Voltage Noise, 1 kHz								
G = 5			50			50		nV/√Hz
G = 1000			30			30		nV/√Hz
RTI, 0.1 Hz to 10 Hz								
G = 5			3.0			3.0		µV p-p
G = 1000			1.5			1.5		µV p-p
Current Noise, 1 kHz			100			100		fA/√Hz
0.1 Hz to 10 Hz			1.5			1.5		pA p-p
VOLTAGE OFFSET	Total RTI Error = V_{OSI} + V_{OSO}/G							
Input Offset, V_{OSI}				400			200	µV
Average TC				5			3	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Average TC				15			10	µV/°C
Offset Referred to Input vs. Supply (PSR)								
G = 5		80			90			dB
G = 10		86			96			dB
G = 100		90			100			dB
G = 1000		90			100			dB
INPUT CURRENT								
Input Bias Current			17	25		17	25	nA
Over Temperature				27.5			27.5	nA
Average Temperature Coefficient			25			25		pA/°C
Input Offset Current			0.25	2		0.25	2	nA
Over Temperature				2.5			2.5	nA
Average Temperature Coefficient			5			5		pA/°C
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 5			200			200		kHz
G = 10			190			190		kHz
G = 100			75			75		kHz
G = 1000			8			8		kHz
Slew Rate			0.3			0.3		V/µs
Settling Time to 0.01%	Step size = 10 V							
G = 5			30			30		µs
G = 100			30			30		µs
G = 1000			140			140		µs

Parameter	Conditions	AD8223A Min	AD8223A Typ	AD8223A Max	AD8223B Min	AD8223B Typ	AD8223B Max	Unit
GAIN	G = 5 + (80 k/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error[1]	V_{OUT} = −10 V to +10 V							
G = 5			0.03	0.15		0.03	0.1	%
G = 10			0.10	1		0.10	0.5	%
G = 100			0.10	1		0.10	0.5	%
G = 1000			0.10	1		0.10	0.5	%
Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 5 to 1000			50			50		ppm
Gain vs. Temperature								
G = 5			5	10		5	10	ppm/°C
G > 5[1]			50			50		ppm/°C
INPUT								
Input Impedance								
Differential			2‖2			2‖2		GΩ‖pF
Common-Mode			2‖2			2‖2		GΩ‖pF
Input Voltage Range[2]		(−V_S) − 0.15		(+V_S) − 1.5	(−V_S) − 0.15		(+V_S) − 1.5	V
OUTPUT								
Output Swing	R_L = 10 kΩ to ground	(−V_S) + 0.2		(+V_S) − 0.5	(−V_S) + 0.2		(+V_S) − 0.5	V
	R_L = 100 kΩ to ground	(−V_S) + 0.1		(+V_S) − 0.2	(−V_S) + 0.1		(+V_S) − 0.2	V
REFERENCE INPUT								
R_{IN}			60	±20%		60	±20%	kΩ
I_{IN}	V_{IN}+, V_{REF} = 0		+50	+60		+50	+60	µA
Voltage Range		−V_S		+V_S	−V_S		+V_S	V
Gain to Output			1 ± 0.0002			1 ± 0.0002		V
POWER SUPPLY								
Operating Range		±2.5		±12.5	±2.5		±12.5	V
Quiescent Current				600			600	µA
TEMPERATURE RANGE								
For Specified Performance		−40		+85	−40		+85	°C

[1] Does not include effects of external resistor RG.
[2] One input grounded. G = 1.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±12.5 V
Internal Power Dissipation	650 mW
Differential Input Voltage	±6 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range (R, RM)	−65°C to +125°C
Operating Temperature Range (A)	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

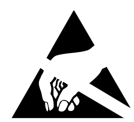
θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Specification is for device in free air.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC	155	°C/W
8-Lead MSOP	200	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C V_S = ±5 V, R_L = 10 kΩ, unless otherwise noted.

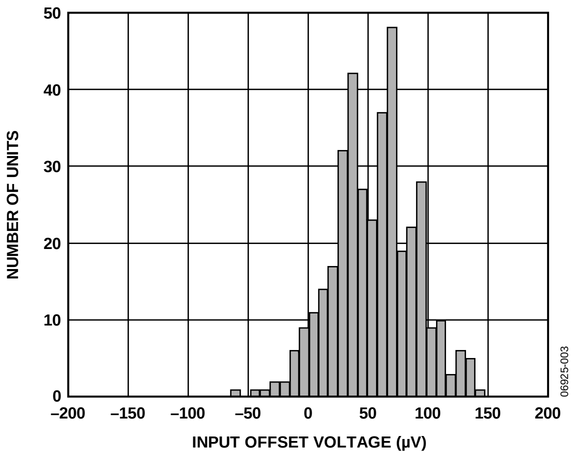


Figure 2. Typical Distribution of Input Offset Voltage

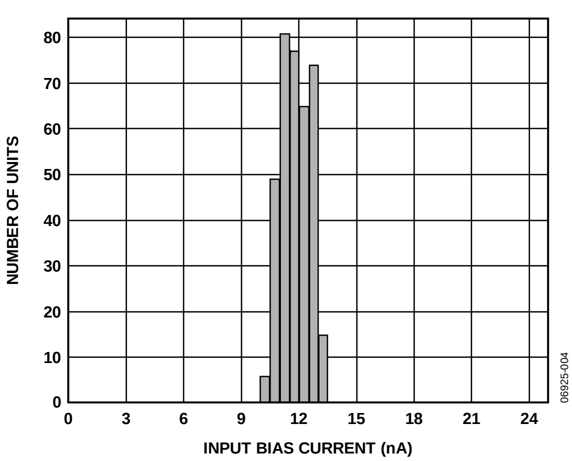


Figure 3. Typical Distribution of Input Bias Current

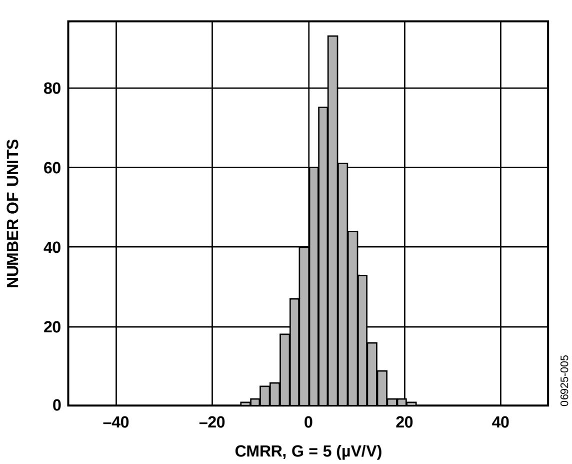


Figure 4. Typical Distribution for CMRR (G = 5)

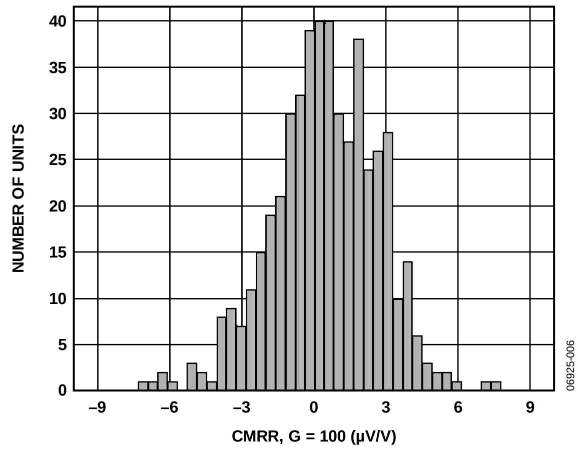


Figure 5. Typical Distribution for CMRR (G = 100)

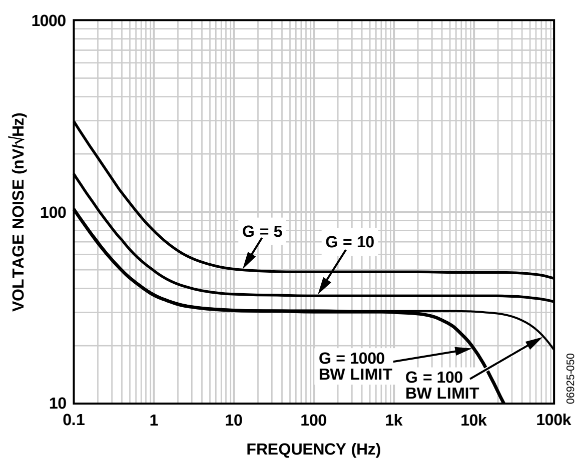


Figure 6. Voltage Noise Spectral Density vs. Frequency

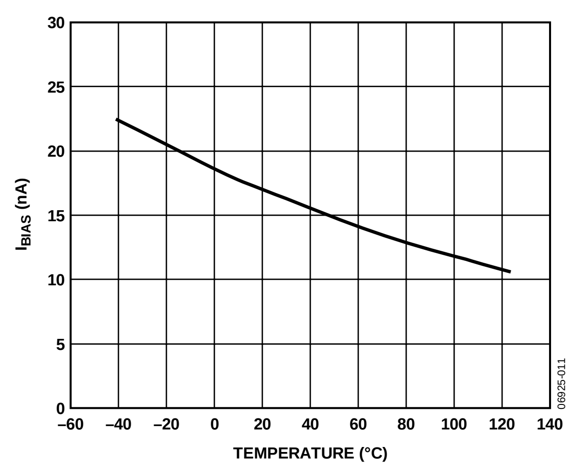


Figure 7. I_{BIAS} vs. Temperature

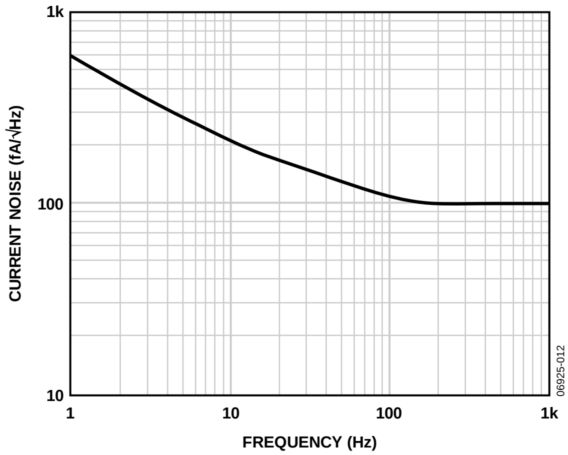


Figure 8. Current Noise Spectral Density vs. Frequency

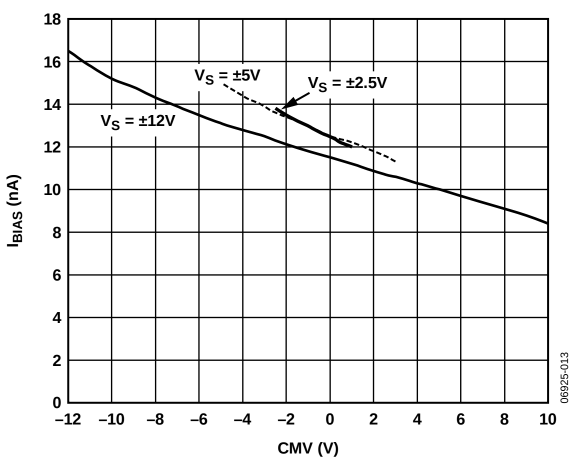


Figure 9. I_{BIAS} vs. CMV

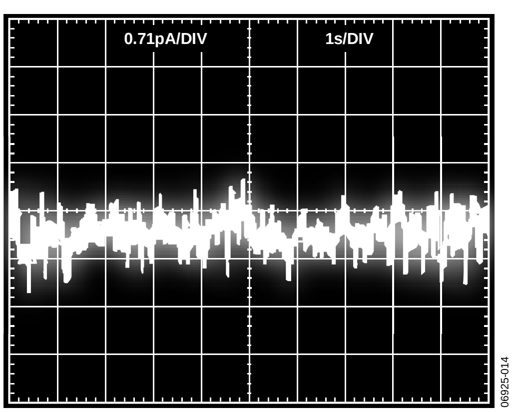


Figure 10. 0.1 Hz to 10 Hz Current Noise (0.71 pA/Div)

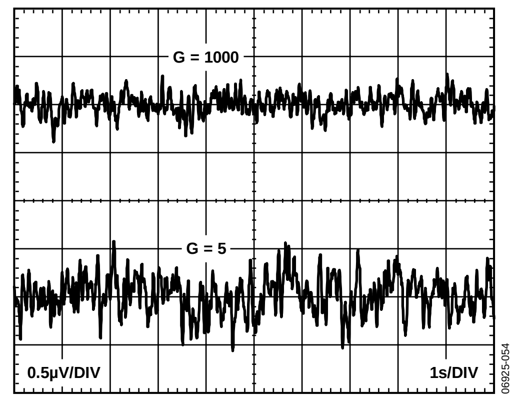


Figure 11. 0.1 Hz to 10 Hz RTI and RTO Voltage Noise

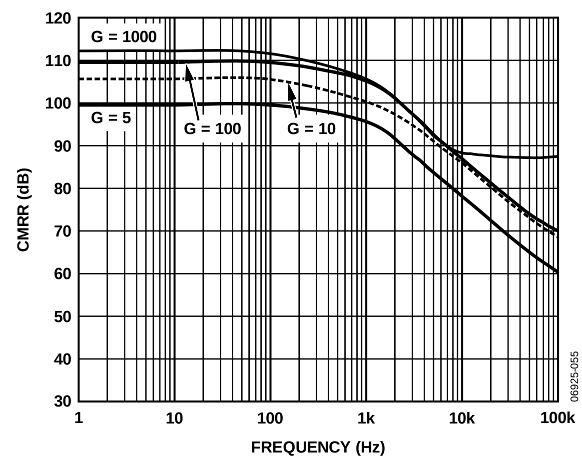


Figure 12. CMRR vs. Frequency, ±12 V_S

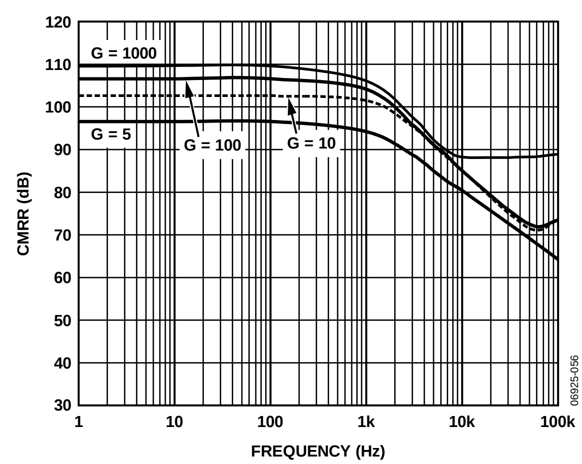


Figure 13. CMRR vs. Frequency, V_S = +5 V

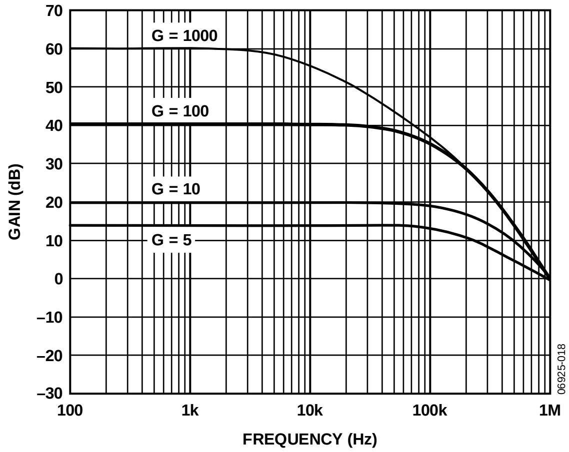


Figure 14. Gain vs. Frequency

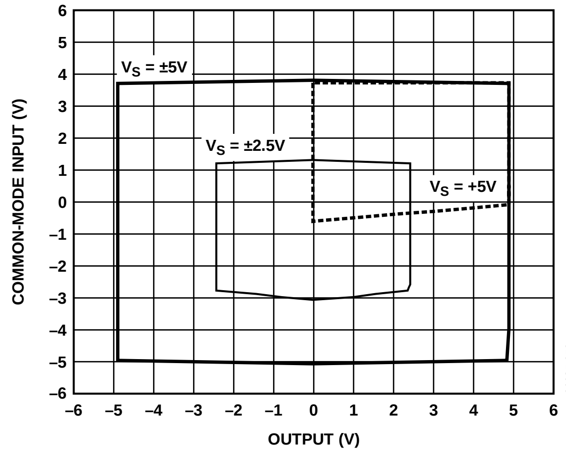


Figure 17. Common-Mode Input vs. Maximum Output Voltage, G = 100, Small Supplies

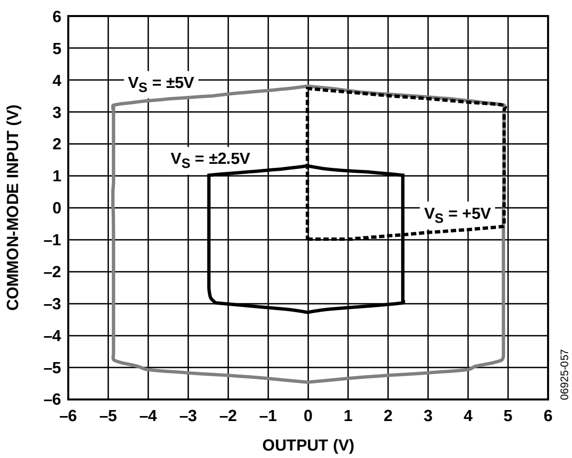


Figure 15. Common-Mode Input vs. Maximum Output Voltage, G = 5, Small Supplies

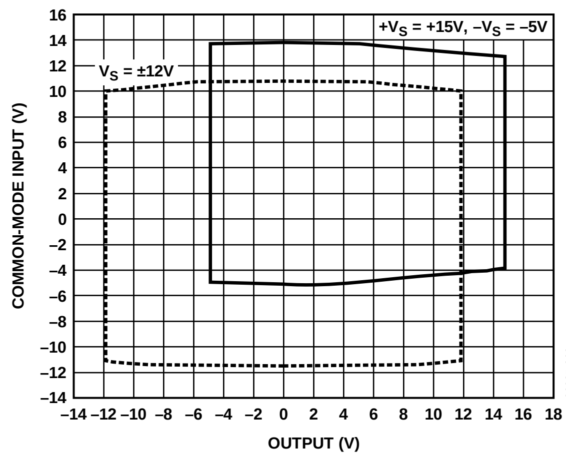


Figure 18. Common-Mode Input vs. Maximum Output Voltage, G = 100, Large Supplies

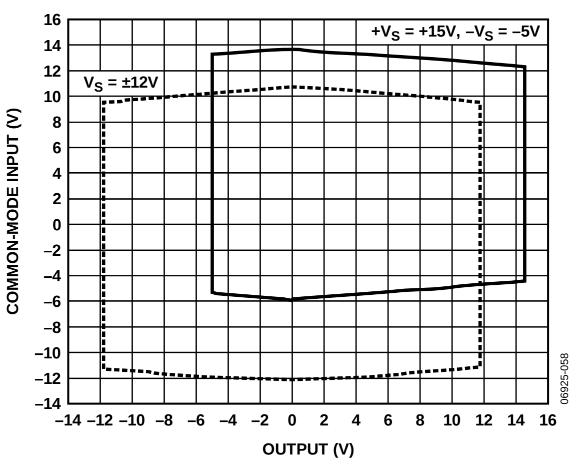


Figure 16. Common-Mode Input vs. Maximum Output Voltage, G = 5, Large Supplies

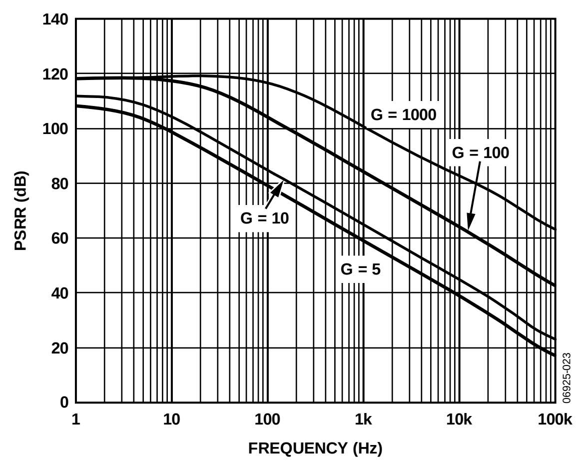


Figure 19. Positive PSRR vs. Frequency, V_S = ±12 V

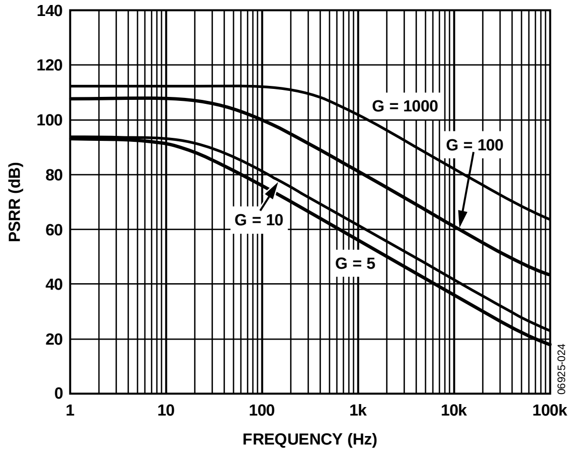


Figure 20. Positive PSRR vs. Frequency, $V_S = 5$ V

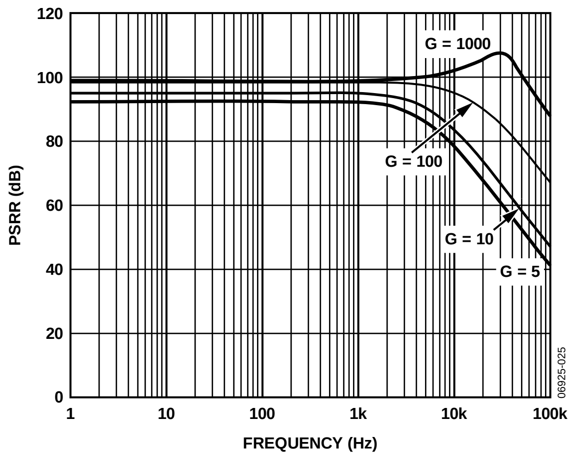


Figure 21. Negative PSRR vs. Frequency, $V_S = \pm12$ V

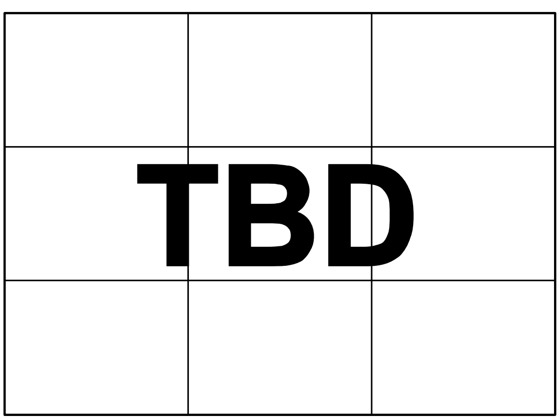


Figure 22. Settling Time to 0.005% vs. Gain, for a 20 V Step at Output, $C_L = 100$ pF, $V_S = \pm12$ V

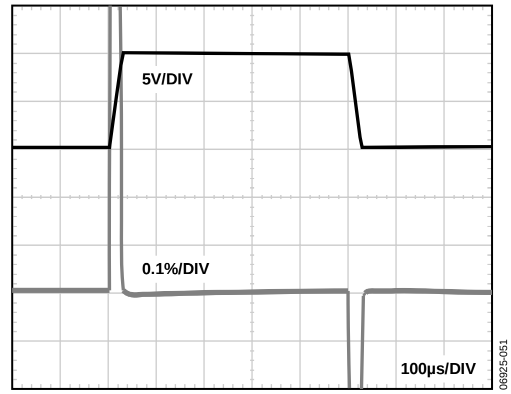


Figure 23. Large Signal Response, G = 5

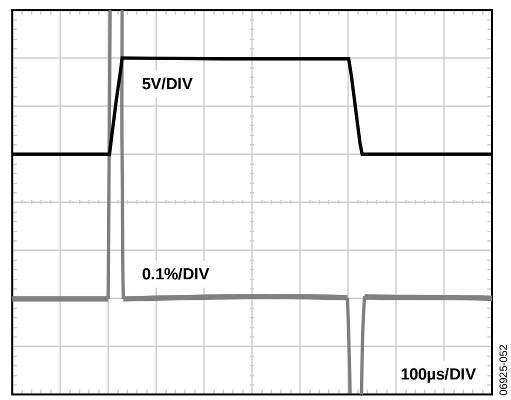


Figure 24. Large Signal Pulse Response, G = 100, $C_L = 100$ pF

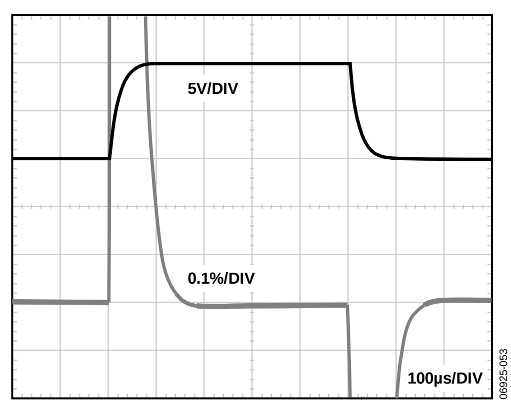


Figure 25. Large Signal Pulse Response, G = 1000, $C_L = 100$ pF

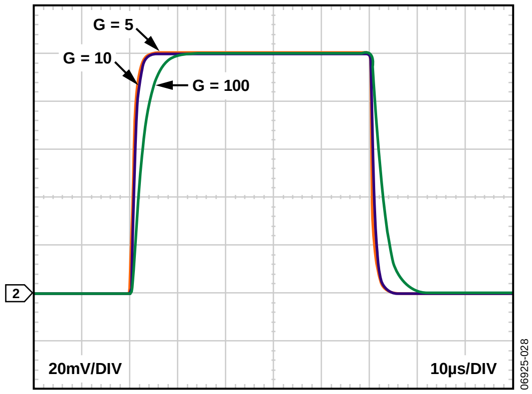


Figure 26. Small Signal Pulse Response, G = 5, 10, 100; R_L = 10 kΩ

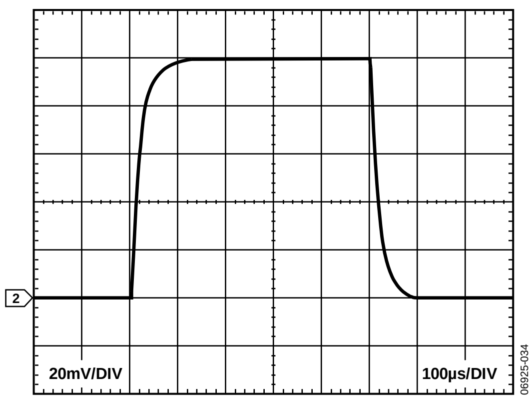


Figure 27. Small Signal Pulse Response, G = 1000, R_L = 25 kΩ, C_L = 100 pF

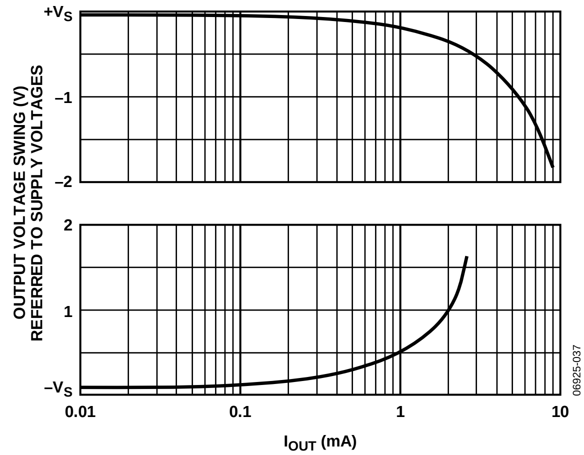


Figure 28. Output Voltage Swing vs. Output Current

THEORY OF OPERATION

AMPLIFIER ARCHITECTURE

The AD8223 is an instrumentation amplifier based on a classic 3-op amp approach, modified to assure operation even at common-mode voltages at the negative supply rail. The architecture allows lower voltage offsets, better CMRR, and higher gain accuracy than competing instrumentation amplifiers in its class.

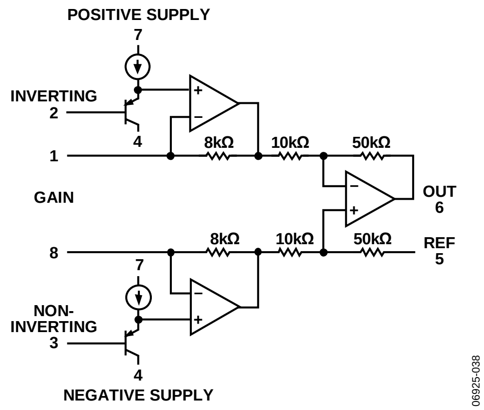


Figure 29. Simplified Schematic

Figure 29 shows a simplified schematic of the AD8223. The AD8223 has three stages. In the first stage, the input signal is applied to PNP transistors. These PNP transistors act as voltage buffers and allow input voltages below ground. The second stage consists of a pair of 8 kΩ resistors, the R_G resistor, and a pair of amplifiers. This stage allows the amplification of the AD8223 to be set with a single external resistor. The third stage is a differential amplifier composed of an op amp, two 10 kΩ resistors, and two 50 kΩ resistors. This stage removes the common mode signal and applies an additional gain of 5.

The transfer function of the AD8223 is

$$V_{OUT} = G(V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 5 + \frac{80\ \text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8223, which can be calculated by referring to Table 5 or by using the following gain equation:

$$R_G = \frac{80\ \text{k}\Omega}{G - 5}$$

Table 5. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Desired Gain	Calculated Gain
26.7k	8	7.99
15.8k	10	10.1
5.36k	20	19.9
2.26k	40	40.4
1.78k	50	49.9
845	100	99.7
412	200	199
162	500	499
80.6	1000	998

The AD8223 defaults to G = 5 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the specifications of the AD8223 to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are kept to a minimum.

INPUT VOLTAGE RANGE

The 3-op amp architecture of the AD8223 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8223 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. To determine whether the signal can be limited, refer to Figure 15 through Figure 18. Alternatively, use the parameters in the Specifications section to verify that the input and output are not limited and then use the following formula to make sure the internal nodes are not limited:

To check if it is limited by the internal nodes,

$$-V_S + 0.01\ \text{V} < 0.6 + V_{CM} \pm \frac{|V_{DIFF}| \times Gain}{10} < +V_S - 0.1\ \text{V}$$

If more common-mode range is required, a solution is to apply less gain in the instrumentation amplifier and more in a later stage.

REFERENCE TERMINAL

The output voltage of the AD8223 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8223 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept below 5 Ω. As shown in Figure 29, the reference terminal, REF, is at one end of a 50 kΩ resistor. Additional impedance at the REF terminal adds to this resistor and results in poorer CMRR performance.

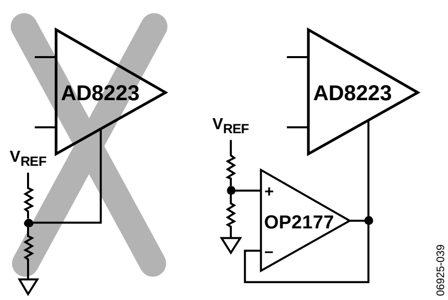


Figure 30. Driving the Reference Pin

INPUT PROTECTION

Internal supply referenced clamping diodes allow the input, reference, output, and gain terminals of the AD8223 to safely withstand overvoltages of 0.3 V above or below the supplies. This is true for all gains, and for power-on and power-off. This last case is particularly important because the signal source and amplifier may be powered separately.

If the overvoltage is expected to exceed this value, the current through these diodes should be limited to about 10 mA using external current limiting resistors. This is shown in Figure 31. The size of this resistor is defined by the supply voltage and the required overvoltage protection.

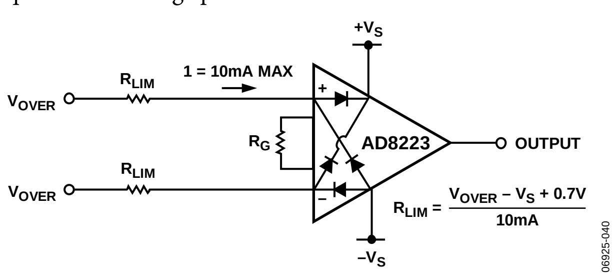


Figure 31. Input Protection

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass, R-C network placed at the input of the instrumentation amplifier, as shown in Figure 32. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{Diff} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

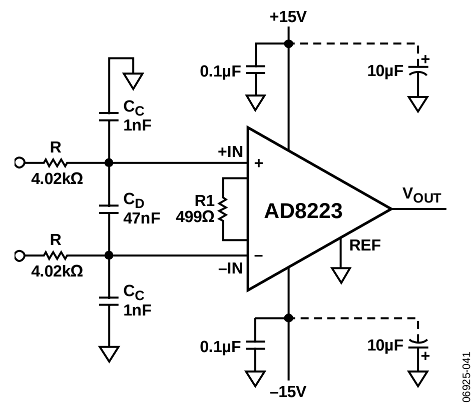


Figure 32. RFI Suppression

Figure 32 shows an example where the differential filter frequency is approximately 400 Hz, and the common-mode filter frequency is approximately 40 kHz. The typical dc offset shift over frequency is less than 1.5 µV and the circuit's RF signal rejection is better than 71 dB.

The resistors were selected to be large enough to isolate the circuit's input from the capacitors, but not large enough to significantly increase the circuit's noise. Values of R and C_C should be chosen to minimize RFI. Mismatch between the $R \times C_C$ at the positive input and the $R \times C_C$ at negative input degrades the CMRR of the AD8223. Because of their higher accuracy and stability, COG/NPO type ceramic capacitors are recommended for the C_C capacitors. The dielectric for the C_D capacitor is not as critical.

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those dc currents that must flow to bias the input transistors of an amplifier. These are usually transistor base currents. When amplifying floating input sources such as transformers or ac-coupled sources, there must be a direct dc path into each input so that the bias current can flow. Figure 33 shows how a bias current path can be provided for the cases of transformer coupling, capacitive ac-coupling and for a thermocouple application.

In dc-coupled resistive bridge applications, providing this path is generally not necessary as the bias current simply flows from the bridge supply through the bridge and into the amplifier. However, if the impedances that the two inputs see are large and differ by a large amount (>10 kΩ), the offset current of the input stage causes dc errors proportional with the input offset voltage of the amplifier.

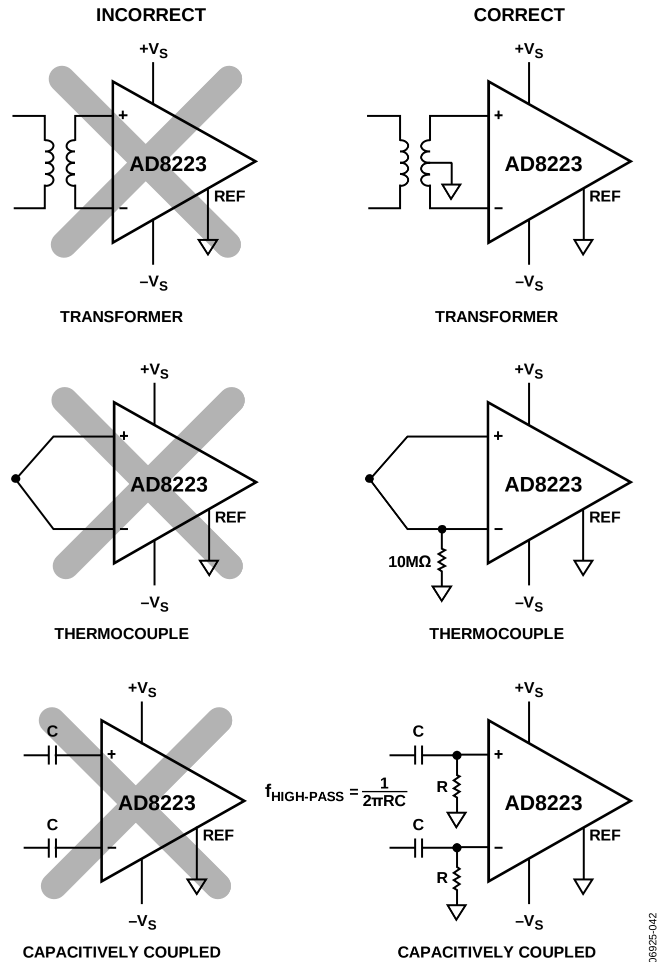


Figure 33. Creating an I_{BIAS} Path

APPLICATIONS INFORMATION

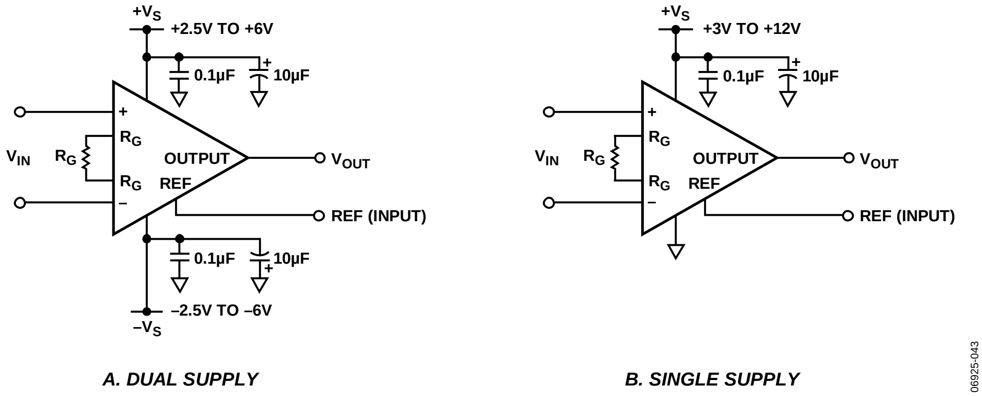


Figure 34. Basic Connections

BASIC CONNECTION

Figure 34 shows the basic connection circuit for the AD8223. The $+V_S$ and $−V_S$ terminals are connected to the power supply. The supply can be either bipolar (V_S = ±2.5 V to ±12.5 V) or single supply ($−V_S$ = 0 V, $+V_S$ = +3.0 V to +25 V). Power supplies should be capacitively decoupled close to the device's power pins. For best results, use surface-mount 0.1 µF ceramic chip capacitors and 10 µF electrolytic tantalum capacitors.

The input voltage, which can be either single-ended (tie either −IN or +IN to ground) or differential, is amplified by the programmed gain. The output signal appears as the voltage difference between the output pin and the externally applied voltage on the REF input.

DIFFERENTIAL OUTPUT

Figure 35 shows how to create a differential output in-amp. A OP1177 op amp creates the inverted output. Because the op amp drives the AD8223 reference pin, the AD8223 can still ensure that the differential voltage is correct. Errors from the op amp or mismatched resistors are common to both outputs and are thus common mode. These common-mode errors should be rejected by the next device in the signal chain.

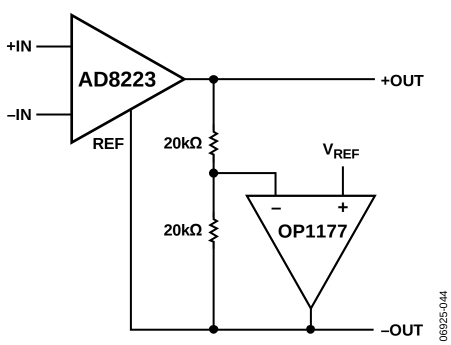


Figure 35. Differential Output Using Op Amp

OUTPUT BUFFERING

The AD8223 is designed to drive loads of 10 kΩ or greater. If the load is less than this value, the AD8223 output should be buffered with a precision single-supply op amp such as the OP113. This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω.

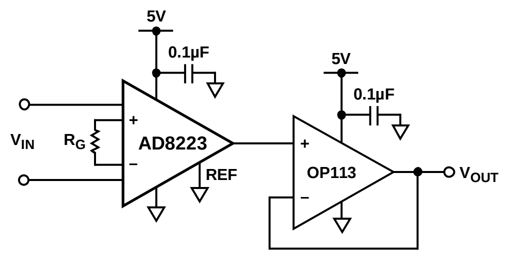


Figure 36. Output Buffering

CABLES

Receiving from a Cable

In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield should be properly driven. Figure 37 shows an active guard drive that is configured to improve ac common-mode rejection by bootstrapping the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

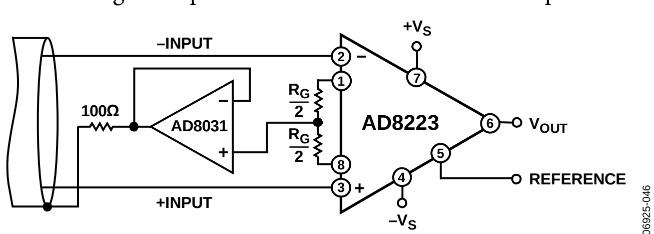


Figure 37. Common-Mode Shield Driver

Driving a Cable

All cables have a certain capacitance per unit length, which varies widely with cable type. The capacitive load from the cable may cause peaking in the AD8223's output response. To reduce the peaking, use a resistor between the AD8223 and the cable. Because cable capacitance and desired output response vary widely, this resistor is best determined empirically. A good starting point is 50 Ω.

The AD8232 operates at a low enough frequency that transmission line effects are rarely an issue; therefore, the resistor need not match the characteristic impedance of the cable.

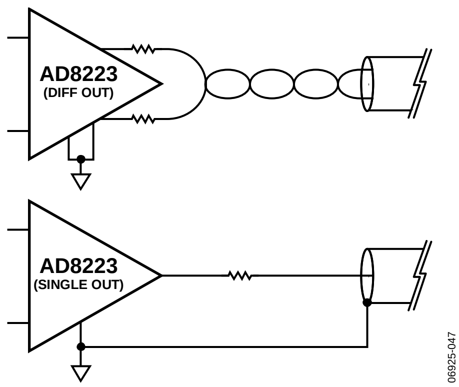


Figure 38. Driving a Cable

A SINGLE-SUPPLY DATA ACQUISITION SYSTEM

Interfacing bipolar signals to single-supply analog-to-digital converters (ADCs) presents a challenge. The bipolar signal must be mapped into the input range of the ADC. Figure 39 shows how this translation can be achieved.

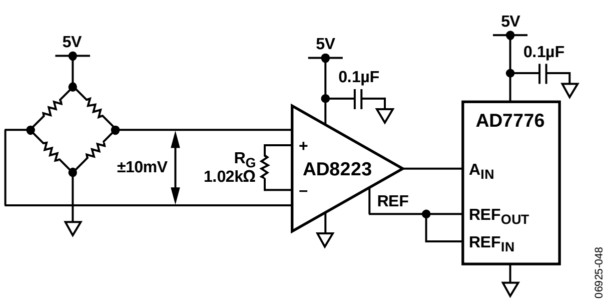


Figure 39. A Single Supply Data Acquisition System

The bridge circuit is excited by a +5 V supply. The full-scale output voltage from the bridge (±10 mV) therefore has a common-mode level of 2.5 V. The AD8223 removes the common-mode component and amplifies the input signal by a factor of 100 (R_{GAIN} = 1.02 kΩ). This results in an output signal of ±1 V. To prevent this signal from running into the AD8223 ground rail, the voltage on the REF pin has to be raised to at least 1 V. In this example, the 2 V reference voltage from the AD7776 ADC is used to bias the AD8223 output voltage to 2 V ± 1 V. This corresponds to the input range of the ADC.

AMPLIFYING SIGNALS WITH LOW COMMON-MODE VOLTAGE

Because the common-mode input range of the AD8223 extends 0.1 V below ground, it is possible to measure small differential signals that have low, or no, common-mode components. Figure 40 shows a thermocouple application where one side of the J-type thermocouple is grounded.

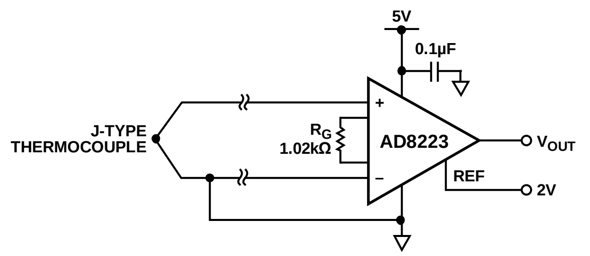
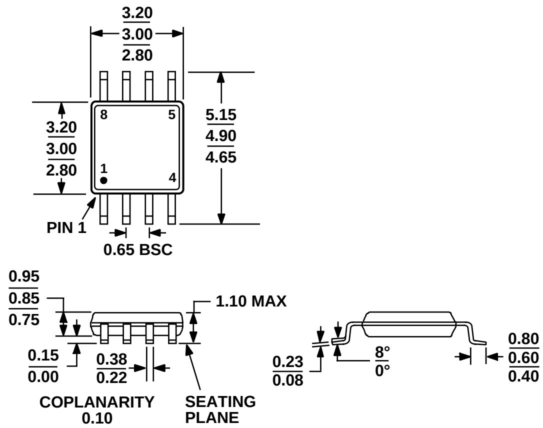


Figure 40. Amplifying Bipolar Signals with Low Common-Mode Voltage

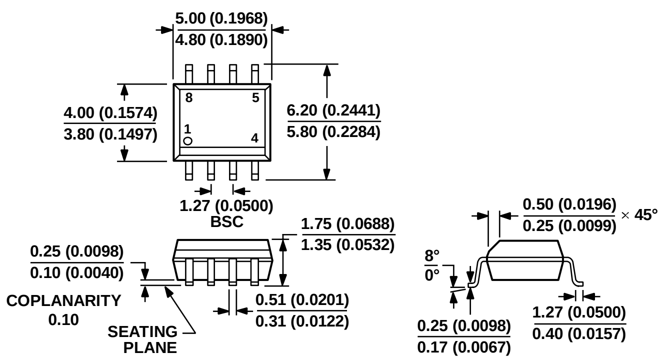
Over a temperature range from −200°C to +200°C, the J-type thermocouple delivers a voltage ranging from −7.890 mV to 10.777 mV. A programmed gain on the AD8223 of 100 (R_G = 845) and a voltage on the AD8223 REF pin of 2 V results in the AD8223 output voltage ranging from 1.110 V to 3.077 V relative to ground.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 41. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 42. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8223AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8223AR-RL	−40°C to +85°C	8-Lead SOIC_N,13" Tape and Reel	R-8	
AD8223AR-R7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8223ARM	−40°C to +85°C	8-Lead MSOP	RM-8	Y0U
AD8223ARM-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y0U
AD8223ARM-R7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y0U
AD8223ARMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	Y0Q
AD8223ARMZ-RL[1]	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y0Q
AD8223ARMZ-R7[1]	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y0Q
AD8223ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8223ARZ-RL[1]	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8223ARZ-R7[1]	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8223BR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8223BR-RL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8223BR-R7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8223BRM	−40°C to +85°C	8-Lead MSOP	RM-8	Y0V
AD8223BRM-RL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y0V
AD8223BRM-R7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y0V
AD8223BRMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	Y0R
AD8223BRMZ-RL[1]	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y0R
AD8223BRMZ-R7[1]	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y0R
AD8223BRZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8223BRZ-RL[1]	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8223BRZ-R7[1]	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	

[1] Z = RoHS Compliant Part.

NOTES