



The Infinite Bandwidth Company™

# MIC2590B

## Dual-Slot PCI Hot Plug Controller

### Final Information

### General Description

The MIC2590B is a power controller supporting power distribution requirements for Peripheral Component Interconnect (PCI) hot plug compliant systems incorporating the Intelligent Platform Management Interface (IPMI). The MIC2590B provides complete power control support for two PCI slots including the 3.3V<sub>AUX</sub> defined by the PCI 2.2 specification. Support for +5V, +3.3V, +12V and -12V supplies is provided including programmable constant-current inrush limiting, voltage supervision, programmable current limit, fault reporting and circuit breaker functions which provide fault isolation. The MIC2590B also incorporates a SMBus interface in which complete status and control of power within each slot is provided. Data such as voltage and current from each supply of each slot can be obtained for IPMI sensor records in addition to power status of each slot.

### Features

- Supports two independent PCI 2.2 slots
- SMBus interface for slot power control and status
- +5V, +3.3V, +12V, -12V, +3.3V<sub>AUX</sub> supplies supported per PCI specification 2.2
- Programmable inrush current-limiting
- Active current regulation controls inrush current
- Electronic circuit breaker
- Dual level fault detection for quick fault response without nuisance tripping
- Thermal isolation between circuitry for slot A and slot B

### Applications

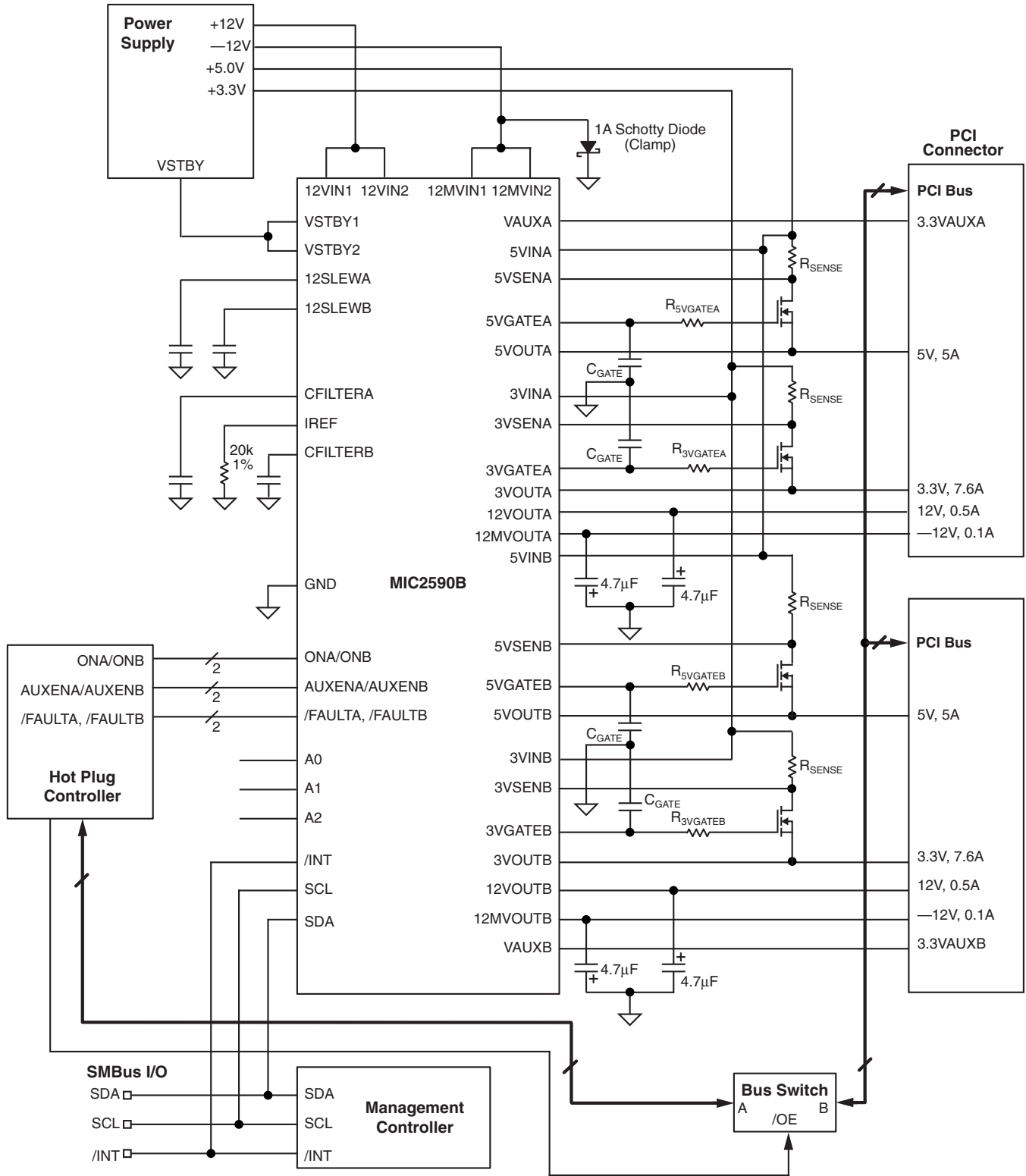
- PCI hot-plug power distribution

### Ordering Information

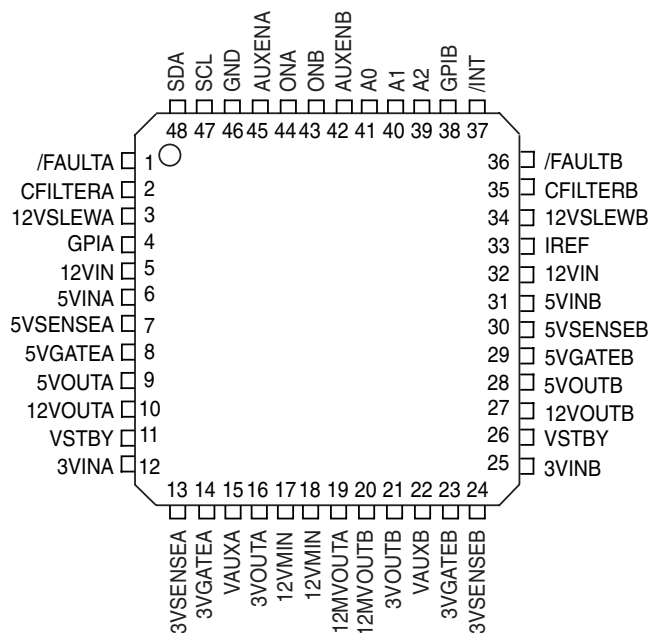
| Part Number   | 5V & 3V Fast-trip Threshold | +12V & -12V Fast-trip Threshold | Operating Temp. Range | Package     |
|---------------|-----------------------------|---------------------------------|-----------------------|-------------|
| MIC2590B-2BTQ | 100mV                       | 1.5A/0.4A                       | 0°C to +70°C          | 48-Pin TQFP |
| MIC2590B-5BTQ | Disabled*                   | 1.5A/0.4A                       | 0°C to +70°C          | 48-Pin TQFP |

\*Contact factory for availability.

# Typical Application



# Pin Configuration



**48-Pin TQFP (BTQ)**

## Pin Description

| Pin Number | Pin Name           | Pin Function   |
|------------|--------------------|--|
| 6, 31      | 5VINA, 5VINB       | 5V Supply Power and Sense Inputs [A/B]: Two pins are provided for Kelvin connection (one for each slot). Pin 6 is the Kelvin sense connection to the supply side of the sense resistor for 5V Slot A. Pin 31 is the Kelvin sense connection to the supply side of the sense resistor for 5V Slot B. These two pins must ultimately connect to each other within 10cm. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.    |
| 12, 25     | 3VINA, 3VINB       | 3.3V Supply Power and Sense Inputs [A/B]: Two pins are provided for Kelvin connection (one for each slot). Pin 12 is the Kelvin sense connection to the supply side of the sense resistor for 3V Slot A. Pin 25 is the Kelvin sense connection to the supply side of the sense resistor for 3V Slot B. These two pins must ultimately connect to each other within 10cm. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold. |
| 5, 32      | 12VIN – 2 pins     | +12V Supply Input: An undervoltage lockout circuit prevents the switches from turning on while this input is less than its lockout threshold. Both pins must be tied together at the chip.   |
| 17, 18     | 12VMIN – 2 pins    | -12V Supply Input: An undervoltage lockout circuit prevents the switches from turning on while this input is less than its lockout threshold. Both pins must be tied together at the chip.   |
| 10, 27     | 12VOUTA, 12VOUTB   | 12V output [A/B]   |
| 19, 20     | 12MVOUTA, 12MVOUTB | -12V output [A/B]  |
| 3, 34      | 12VSLEWA, 12VSLEWB | 12V Slew Rate Control [A/B]: Connect capacitors between these pins and ground to set output slew rates of the +12V and -12V supplies.  |
| 45, 42     | AUXENA, AUXENB     | AUX Enable Inputs [A/B]: Rising-edge sensitive enable inputs for VAUXA and VAUXB outputs. Taking AUXENA/AUXENB low after a fault resets the respective slot's Aux Output Fault Latch. Tie these pins to ground if using SMBus-mode power control.  |
| 16, 21     | 3VOUTA, 3VOUTB     | 3.3V Power-Good Sense Inputs: Connect to 3.3V[A/B] outputs. Used to monitor the 3.3V output voltages for Power-Good status.  |
| 9, 28      | 5VOUTA, 5VOUTB     | 5V Power-Good Sense Inputs: Connect to 5V[A/B] outputs. Used to monitor the 5V output voltages for Power-Good status.  |
| 33         | IREF               | A resistor connected between this pin and ground sets the ADC current measurement gain. This resistor must be $20k\Omega \pm 1\%$ .  |
| 7, 30      | 5VSENSEA, 5VSENSEB | 5V Circuit Breaker Sense Input [A/B]: The current-limit thresholds are set by connecting sense resistors between these pins and 5VIN[A/B]. When the current-limit threshold of $I_R = 50mV$ is reached, the 5VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for $t_{FLT}$ , the circuit breaker is tripped and the GATE pin for the affected slot is immediately pulled low.       |
| 13, 24     | 3VSENSEA, 3VSENSEB | 3V Circuit Breaker Sense Input [A/B]: The current limit thresholds are set by connecting sense resistors between these pins and 3VIN[A/B]. When the current limit threshold of $I_R = 50mV$ is reached, the 3VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for $t_{FLT}$ , the circuit breaker is tripped and the GATE pin for the affected slot is immediately pulled low.       |

## Pin Description

| Pin Number | Pin Name           | Pin Function  |
|------------|--------------------|---|
| 8, 29      | 5VGATEA, 5VGATEB   | <p>5V Gate Drive Outputs [A/B]: Each connects to the gate of an external N-Channel MOSFET. During power-up the <math>C_{GATE}</math> and the gate of the MOSFETs are charged by a 20<math>\mu</math>A current source. This controls the value of <math>dv/dt</math> seen at the source of the MOSFETs, and hence the current flowing into the load capacitance.</p> <p>During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of <math>t_{FLT}</math>. Whenever an overcurrent, thermal shutdown or input undervoltage fault condition occurs the GATE pin for the affected slot is immediately brought low.</p> <p>During power-down these pins are discharged by an internal current source.</p> |
| 14, 23     | 3VGATEA, 3VGATEB   | <p>3V Gate Drive Outputs [A/B]: Each connects to the gate of an external N-Channel MOSFET. During power-up the <math>C_{GATE}</math> and the gate of the MOSFETs are charged by a 20<math>\mu</math>A current source. This controls the value of <math>dv/dt</math> seen at the source of the MOSFETs, and hence the current flowing into the load capacitance.</p> <p>During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of <math>t_{FLT}</math>. Whenever an overcurrent, thermal shutdown or input undervoltage fault condition occurs the GATE pin for the affected slot is immediately brought low.</p> <p>During power-down these pins are discharged by an internal current source.</p> |
| 11, 26     | VSTBY – 2 pins     | 3.3V Standby input voltage required to support PCI 2.2 VAUX input: SMBus, internal registers and A/D converter run off of VSTBY to ensure chip access during standby modes. A UVLO circuit prevents turn-on of this supply until VSTBY rises above its UVLO threshold. Both pins must be tied together at the chip.   |
| 15, 22     | VAUXA, VAUXB       | $V_{AUX}$ [A/B] output voltages to PCI card slots: These outputs connect the VAUX pin of the PCI 2.2 Connectors VSTBY via internal 400m $\Omega$ MOSFETs which are current-limited and protected against short circuit faults.  |
| 44, 43     | ONA, ONB           | Enable input for MAIN outputs: Rising-edge sensitive. Used to enable or disable MAIN (5V, 3.3V, +12V, –12V) outputs. Taking ONA/ONB low after a fault resets the respective slot's Main Output Fault Latch. Tie these pins to ground if using SMBus-mode power control.   |
| 1, 36      | /FAULTA, /FAULTB   | <p>Open Drain, Active-Low: Asserted whenever the circuit breaker trips due to a fault condition.</p> <p>/FAULT[A/B] is reset by bringing the faulted slot's ON pin low if /FAULT was asserted in response to a fault condition on one of the slot's MAIN outputs (+12V, +5V, +3.3V, or –12V).</p> <p>/FAULT[A/B] is reset by bringing the faulted slot's AUXEN pin low if /FAULT was asserted in response to a fault condition on the slot's VAUX output.</p> <p>If a fault condition occurred on both the MAIN and AUX outputs of the same slot, then both ON and AUXEN must be brought low to de-assert the /FAULT output.</p>  |
| 2, 35      | CFILTERA, CFILTERB | Filter Capacitor [A/B]: Capacitors connected between these pins and ground set the duration of $t_{FLT}$ . $t_{FLT}$ is the amount of time for which a slot remains in current-limit before its circuit breaker is tripped.   |
| 37         | /INT               | Interrupt Output: Open Drain, Active-low. Asserted whenever a power fault is detected. Cleared by writing a logic 1 to the respective active bit into the Status Register.  |

**Pin Description**

| Pin Number | Pin Name   | Pin Function   |
|------------|------------|--|
| 48         | SDA        | SMBus Data: Bidirectional SMBus data line.   |
| 47         | SCL        | SMBus Clock: Input.  |
| 39, 40, 41 | A2, A1, A0 | SMBus Address Select pins: Connect to ground or leave open in order to program device SMBus base address. There is an internal pull-up to VSTBY on each of these inputs. |
| 4, 38      | GPIA, GPIB | General Purpose Inputs: The state of these inputs are available by reading the Common Status Register.   |
| 46         | GND        | Ground.  |

**Absolute Maximum Ratings (Note 1)**

|   |                          |
|---|--------------------------|
| Supply Voltage                                  |                          |
| (12V <sub>IN</sub> ).....                       | +14V                     |
| (12MV <sub>IN</sub> ).....                      | -14V                     |
| (5V <sub>IN</sub> ).....                        | +7V                      |
| (3V <sub>IN</sub> ), (V <sub>STBY</sub> ) ..... | +7V                      |
| Any Logic Output Voltage .....                  | -0.5 (min.)/+5.5V (max.) |
| Any Logic Input Voltage .....                   | -0.5 (min.)/+5.5V (max.) |
| Output Current (FAULT[A/B]#, /INT, SDA).....    | 10mA                     |
| Lead Temperature                                |                          |
| IR Reflow, Peak Temperature .....               | 235 +5/-0°C              |
| Storage Temperature (T <sub>S</sub> ) .....     | -65°C to +150°C          |
| ESD Rating, <b>Note 3</b> .....                 | 2kV                      |

**Operating Ratings (Note 2)**

|  |                   |
|--|-------------------|
| Supply Voltage                               |                   |
| (12V <sub>IN</sub> ).....                    | +11.65V to +12.6V |
| (12MV <sub>IN</sub> ).....                   | -11.0V to -13.2V  |
| (5V <sub>IN</sub> ).....                     | +4.85V to +5.25V  |
| (3V <sub>IN</sub> ).....                     | +3.1V to +3.6V    |
| (V <sub>STBY</sub> ) .....                   | +3.15V to +3.6V   |
| Ambient Temperature (T <sub>A</sub> ) .....  | 0°C to +70°C      |
| Junction Temperature (T <sub>J</sub> ) ..... | 125°C             |
| Package Thermal Resistance                   |                   |
| TQFP (θ <sub>JA</sub> ) .....                | 56.5°C/W          |

**Electrical Characteristics**

12V<sub>IN</sub> = 12V; 12MV<sub>IN</sub> = -12V; 5V<sub>IN</sub> = 5V; 3V<sub>IN</sub> = 3.3V; V<sub>STBY</sub> = 3.3V; T<sub>A</sub> = 0°C to 70°C; unless noted.

**Power Control and Logic Sections**

| Symbol                    | Parameter   | Condition  | Min                                      | Typ             | Max               | Units |
|---------------------------|---|--|--|-----------------|-------------------|-------|
| I <sub>CC12</sub>         | Supply Current  |  |  | 0.6             | 2.0               | mA    |
| I <sub>CC5</sub>          |   |  |  | 1.2             | 2.0               | mA    |
| I <sub>CC33</sub>         |   |  |  | 0.5             | 0.7               | mA    |
| I <sub>CC12M</sub>        |   |  |  | -1.0            | -2.0              | mA    |
| I <sub>CCVSBY</sub>       |   |  |  | 2.5             | 5.0               | mA    |
| V <sub>UVLO</sub>         | Under Voltage Lockout   | 12V <sub>IN</sub> increasing   | 8  | 9               | 10                | V     |
|                           |   | 3V <sub>IN</sub> increasing  | 2.2                                      | 2.5             | 2.75              | V     |
|                           |   | 5V <sub>IN</sub> increasing  | 3.7                                      | 4.0             | 4.3               | V     |
|                           |   | 12MV <sub>IN</sub> decreasing  | -10                                      | -9              | -8                | V     |
|                           |   | V <sub>STBY</sub> increasing   | 2.8                                      | 2.9             | 3.0               | V     |
| V <sub>HYSUV</sub>        | Under Voltage Lockout Hysteresis - 12V <sub>IN</sub> , 12MV <sub>IN</sub> , 5V <sub>IN</sub> , 3V <sub>IN</sub> |  |  | 180             |                   | mV    |
| V <sub>HYSSTBY</sub>      | Under-voltage Lockout Hysteresis - V <sub>STBY</sub>  |  |  | 50              |                   | mV    |
| V <sub>UVTH</sub>         | Power Good Under-Voltage Thresholds   |  |  |                 |                   |       |
| V <sub>UVTH(12V)</sub>    |   | 12V <sub>OUT</sub> [A/B] decreasing  | 10.2                                     | 10.5            | 10.8              | V     |
| V <sub>UVTH(12MV)</sub>   |   | 12MV <sub>OUT</sub> [A/B] increasing   | -10.8                                    | -10.6           | -10.2             | V     |
| V <sub>UVTH(3V)</sub>     |   | 3V <sub>OUT</sub> [A/B] decreasing   | 2.7                                      | 2.8             | 2.9               | V     |
| V <sub>UVTH(5V)</sub>     |   | 5V <sub>OUT</sub> [A/B] decreasing   | 4.4                                      | 4.5             | 4.7               | V     |
| V <sub>UVTH(VAUX)</sub>   |   | V <sub>AUX</sub> [A/B] decreasing  | 2.7                                      | 2.8             | 2.9               | V     |
| V <sub>HYS PG</sub>       | Power-Good Detect Hysteresis  |  |  | 30              |                   | mV    |
| V <sub>GATE</sub>         | 5V <sub>GATE</sub> /3V <sub>GATE</sub> Voltage  |  | 12V <sub>IN</sub> -1.5                   |                 | 12V <sub>IN</sub> | V     |
| I <sub>GATE(SOURCE)</sub> | 5V <sub>GATE</sub> /3V <sub>GATE</sub> Output Source Current  | start cycle  | 15                                       | 25              | 35                | μA    |
| I <sub>GATE(SINK)</sub>   | 5V <sub>GATE</sub> /3V <sub>GATE</sub> Output Sink Fault Current  | any fault condition, V <sub>GATE</sub> = 5V  |  | 70              |                   | mA    |
| V <sub>FILTER</sub>       | C <sub>FILTER</sub> Threshold Voltage   |  | 1.20                                     | 1.25            | 1.30              | V     |
| I <sub>FILTER</sub>       | C <sub>FILTER</sub> [A/B] Charge Current  | V <sub>[5/3]</sub> V <sub>IN</sub> - V <sub>[5/3]</sub> V <sub>SENSE</sub> > V <sub>THILIMIT</sub> | 1.80                                     | 2.5             | 5.0               | μA    |
| I <sub>SLEW</sub>         | 12V <sub>SLEW</sub> [A/B] Charge Current  | During turn-on only  | 13                                       | 22              | 35                | μA    |
| V <sub>THILIMIT</sub>     | Current Limit Threshold Voltages  |  |  |                 |                   |       |
|                           |   | 5V[A/B] Supplies   | V <sub>5VIN</sub> - V <sub>5VSENSE</sub> | 35              | 50                | 65    |
|                           | 3.3V[A/B] Supplies  | V <sub>3VIN</sub> - V <sub>3VSENSE</sub>   | 35                                       | 50              | 65                | mV    |
| V <sub>THFAST</sub>       | 5V <sub>OUT</sub> [A/B] and 3V <sub>OUT</sub> [A/B] Fast-Trip Thresholds  | MIC2590B-2<br>MIC2590B-5   | 90                                       | 113<br>Disabled | 135               | mV    |

| Symbol  | Parameter   | Condition  | Min           | Typ                              | Max   | Units                 |
|---|---|--|---------------|----------------------------------|---|-----------------------|
| V <sub>IL</sub>   | LOW-Level Input Voltage<br>(SCL, SDA, ON[A/B], A[0-2], GPI[A/B])  |  |               |                                  | 0.8   | V                     |
| V <sub>OL</sub>   | Output LOW Voltage<br>/FAULT[A/B], /INT, SDA  | I <sub>OL</sub> = 3mA  |               |                                  | 0.4   | V                     |
| V <sub>IH</sub>   | HIGH-Level Input Voltage<br>SCL, SDA, ON[A/B], A[0-2],<br>AUXEN[A/B], GPI[A/B])   |  | 2.1           |                                  |   | V                     |
| R <sub>PULL-UP</sub>  | Internal Pullups from A[0-2] to V <sub>STBY</sub>   |  |               | 40                               |   | kΩ                    |
| I <sub>IL</sub>   | Input Leakage Current<br>SCL, ON[A/B], AUXEN[A/B], GP[A/B])   |  |               |                                  | ±5  | μA                    |
| I <sub>LKG(OFF)</sub>   | Off-State Leakage Current<br>SDA, /FAULT[A/B], /INT   |  |               |                                  | ±5  | μA                    |
| T <sub>OV</sub>   | Overtemperature Shutdown & Reset<br>Thresholds, with overcurrent on slot  | T <sub>J</sub> Increasing, each slot, <b>Note 5</b><br>T <sub>J</sub> Decreasing, each slot, <b>Note 5</b>   |               | 140<br>130                       |   | °C<br>°C              |
|   | Overtemperature Shutdown & Reset<br>Thresholds, all other conditions<br>(all outputs will latch OFF)  | T <sub>J</sub> Increasing, both slots, <b>Note 5</b><br>T <sub>J</sub> Decreasing, both slots, <b>Note 5</b>   |               | 160<br>150                       |   | °C<br>°C              |
| R <sub>OUT(ON)</sub><br>R <sub>DS(12V)</sub><br>R <sub>DS(12VM)</sub><br>R <sub>DS(AUX)</sub>                                     | Output MOSFET Resistance<br>12V MOSFET<br>-12V MOSFET<br>V <sub>AUX</sub> MOSFET  | I <sub>DS</sub> = 500mA, T <sub>J</sub> = 125°C<br>I <sub>DS</sub> = 100mA, T <sub>J</sub> = 125°C<br>I <sub>DS</sub> = 375mA, T <sub>J</sub> = 125°C                        |               |                                  | 500<br>2<br>400   | mΩ<br>Ω<br>mΩ         |
| V <sub>OFF</sub><br>V <sub>OFF(+12V)</sub><br>V <sub>OFF(-12V)</sub><br>V <sub>OFF(VAUX)</sub>                                    | Off-State Output Offset Voltage<br>12V <sub>OUT</sub> [A/B]<br>12MV <sub>OUT</sub> [A/B]<br>V <sub>AUX</sub> [A/B]  | 12V <sub>OUT</sub> [A/B] = Off, T <sub>J</sub> = 125°C<br>12MV <sub>OUT</sub> [A/B] = Off, T <sub>J</sub> = 125°C<br>V <sub>AUX</sub> [A/B] = Off, T <sub>J</sub> = 125°C    | -50           |                                  | 50<br>50  | mV<br>mV<br>mV        |
| I <sub>THSLOW</sub><br>I <sub>LIM(12)</sub><br>I <sub>LIM(12M)</sub>  | Current Limit Threshold<br>12V MOSFET<br>-12V MOSFET  | 12V <sub>OUT</sub> [A/B] = 0V<br>12MV <sub>OUT</sub> [A/B] = 0V  | 0.52<br>-0.11 | 1.0<br>-0.2                      | 1.5<br>-0.3   | A<br>A                |
| I <sub>THFAST</sub>   | Fast-Trip Thresholds  | 12V <sub>OUT</sub> [A/B] (MIC2590B-2)<br>12MV <sub>OUT</sub> [A/B] (MIC2590B-2)  | 1.0<br>-0.20  | 2.15<br>-0.45                    | 3.0<br>-0.6   | A<br>A                |
| I <sub>AUX(THRESH)</sub>  | Auxiliary Output Current Limit Threshold<br><b>Figure 4</b>   | Current which must be drawn from V <sub>AUX</sub><br>to register as a fault  |               | 0.84                             |   | A                     |
| I <sub>SC(TRAN)</sub>   | Maximum Transient Short Circuit Current   | V <sub>AUX</sub> Enabled, then Grounded  |               |                                  | I <sub>MAX</sub> = V <sub>STBY</sub> / R <sub>DS(AUX)</sub> | A                     |
| I <sub>LIM(AUX)</sub>   | Regulated Current after Transient   | From end of I <sub>SC(TRAN)</sub> to C <sub>FILTER</sub> Time Out  | 0.375         | 0.7                              | 1.35  | A                     |
| R <sub>DISCH</sub><br>R <sub>(12V)</sub><br>R <sub>(12MV)</sub><br>R <sub>(3V)</sub><br>R <sub>(5V)</sub><br>R <sub>(3VAUX)</sub> | Output Discharge Resistance<br>12V <sub>OUT</sub> [A/B]<br>12MV <sub>OUT</sub> [A/B]<br>3V <sub>OUT</sub> [A/B]<br>5V <sub>OUT</sub> [A/B]<br>3V <sub>AUX</sub> [A/B] | 12V <sub>OUT</sub> [A/B] = 6.0V<br>12MV <sub>OUT</sub> [A/B] = -6.0V<br>3V <sub>OUT</sub> [A/B] = 1.65V<br>5V <sub>OUT</sub> [A/B] = 2.5V<br>5V <sub>OUT</sub> [A/B] = 1.65V |               | 1600<br>600<br>150<br>150<br>430 |   | Ω<br>Ω<br>Ω<br>Ω<br>Ω |
| t <sub>OFF(3)</sub><br>t <sub>OFF(5)</sub>  | Current Limit Response Time<br>for 3.3V and 5V Outputs, <b>Figure 2</b>   | MIC2590B-2 with C <sub>GATE</sub> = 10nF,<br>V <sub>IN</sub> - V <sub>SENSE</sub> = 200mV  |               | 1                                |   | μs                    |
| T <sub>SC(TRAN)</sub>   | V <sub>AUX</sub> Current Limiter Response Time<br><b>Figure 5</b>   | V <sub>AUX</sub> [A/B] = 0V, <b>Note 5</b>   |               | 33                               |   | μs                    |
| t <sub>OFF(12)</sub>  | 12V Current Limit Response<br><b>Figure 3</b>   | 12V <sub>OUT</sub> [A/B] = 0V, <b>Note 5</b>   |               | 1                                |   | μs                    |
| t <sub>OFF(12M)</sub>   | -12V Current Limit Response<br><b>Figure 3</b>  | 12MV <sub>OUT</sub> [A/B] = 0V, <b>Note 5</b>  |               | 1                                |   | μs                    |



| Symbol              | Parameter   | Condition   | Min | Typ | Max | Units   |
|---------------------|---|---|-----|-----|-----|---------|
| $T_{PROP(3VFAULT)}$ | Delay from 3V[A/B] overcurrent-limit to FAULT Output        | MIC2590B-2, $V_{SENSE} - V_{THLIMIT} = 200mV$ , $C_{FILTER} = open$ |     | 1   |     | $\mu s$ |
| $T_{PROP(5VFAULT)}$ | Delay from 5V[A/B] overcurrent-limit to FAULT Output        | MIC2590B-2, $V_{SENSE} - V_{THLIMIT} = 200mV$ , $C_{FILTER} = open$ |     | 1   |     | $\mu s$ |
| $t_W$               | ON[A/B], AUXEN[A/B] Pulse Width                             | <b>Note 5</b>   |     | 100 |     | ns      |
| $t_{POR}$           | MIC2590B Power-On Reset Time after $V_{STBY}$ becomes valid | <b>Note 5</b>   |     |     | 500 | $\mu s$ |

**8-Bit Analog to Digital Converter**

| Symbol                         | Parameter   | Condition   | Min      | Typ                           | Max      | Units               |
|--------------------------------|---|---|----------|-------------------------------|----------|---------------------|
|                                | Total Unadjusted Error Voltage, All Outputs<br>Current, $3V_{OUT[A/B]}/5V_{OUT[A/B]}$<br>Current, $V_{AUX[A/B]}$ , $12V_{OUT[A/B]}$ , $12MV_{OUT[A/B]}$ | Measured as voltage across corresponding external $R_{SENSE}$ | -3<br>-3 | <br>$\pm 3$                   | +3<br>+3 | %<br>%<br>%         |
| $t_{CONV}$                     | Conversion Time   |   |          | 60                            | 100      | ms                  |
| $V_{AUXA}$<br>$V_{AUXB}$       | <b>Resolution Specifications:</b><br>Full Scale Voltage<br>LSB of Voltage<br>Full Scale Current<br>LSB of Current                                       |   |          | 3.85<br>15.1<br>375<br>1.47   |          | V<br>mV<br>mA<br>mA |
| $3V_{OUTA}$<br>$3V_{OUTB}$     | Full Scale Voltage<br>LSB of Voltage<br>Full Scale Current<br>LSB of Current  | External $R_{SENSE} = 6.00m\Omega$                            |          | 3.85<br>15.1<br>11.6<br>45.5  |          | V<br>mV<br>A<br>mA  |
| $5V_{OUTA}$<br>$5V_{OUTB}$     | Full Scale Voltage<br>LSB of Voltage<br>Full Scale Current<br>LSB of Current  | External $R_{SENSE} = 10.0m\Omega$                            |          | 5.89<br>23.1<br>6.96<br>27.3  |          | V<br>mV<br>A<br>mA  |
| $12V_{OUTA}$<br>$12V_{OUTB}$   | Full Scale Voltage<br>LSB of Voltage<br>Full Scale Current<br>LSB of Current  |   |          | 13.8<br>54.1<br>500<br>1.96   |          | V<br>mV<br>mA<br>mA |
| $12MV_{OUTA}$<br>$12MV_{OUTB}$ | Full Scale Voltage<br>LSB of Voltage<br>Full Scale Current<br>LSB of Current  |   |          | -13.6<br>53.5<br>100<br>0.392 |          | V<br>mV<br>mA<br>mA |

**SMBus Timing, Note 5**

| Symbol | Parameter                          | Condition                        | Min | Typ | Max | Units   |
|--------|------------------------------------|----------------------------------|-----|-----|-----|---------|
| $t_1$  | SCL (Clock) Period                 | <b>Figure 1</b>                  | 2.5 |     |     | $\mu s$ |
| $t_2$  | Data In Set-Up Time to SCL HIGH    | <b>Figure 1</b>                  | 100 |     |     | ns      |
| $t_3$  | Data Out Stable after SCL LOW      | <b>Figure 1</b>                  | 300 |     |     | ns      |
| $t_4$  | Data LOW Set-Up Time to SCL LOW    | Start Condition, <b>Figure 1</b> | 100 |     |     | ns      |
| $t_5$  | Data HIGH Hold Time after SCL HIGH | Stop Condition, <b>Figure 1</b>  | 100 |     |     | ns      |

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating ratings.

**Note 3.** Devices are ESD sensitive. Employ proper handling precautions. Human body model, 1.5k $\Omega$  in series with 100pF.

**Note 4.** See the Applications Section.

**Note 5.** Parameters guaranteed by design. Not 100% production tested.

# Timing Diagrams

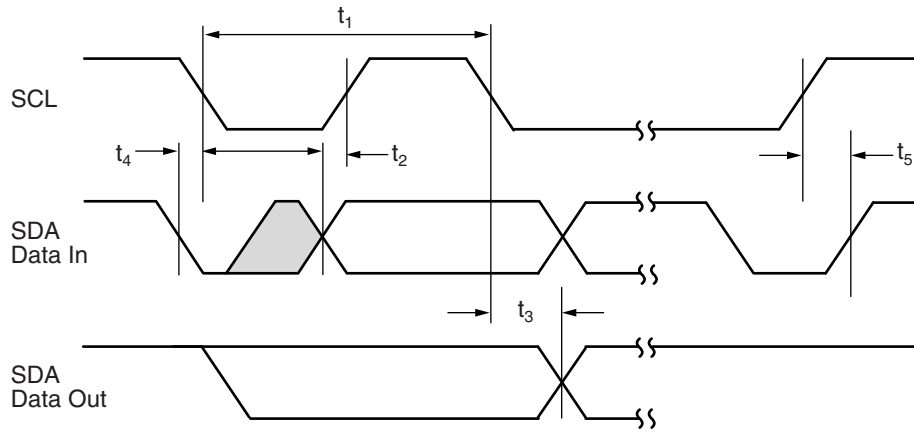


Figure 1. SMBus Timing

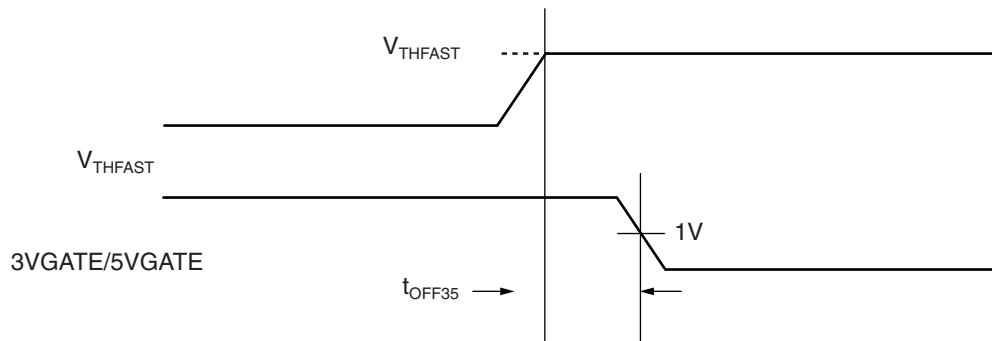


Figure 2. 3V/5V Current Limit Response Timing

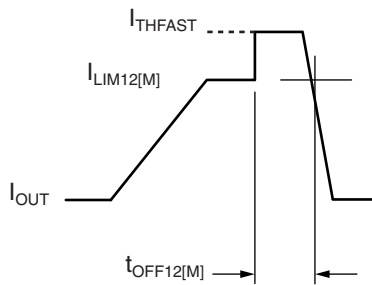


Figure 3. +12V/-12V Current Limit Response Timing

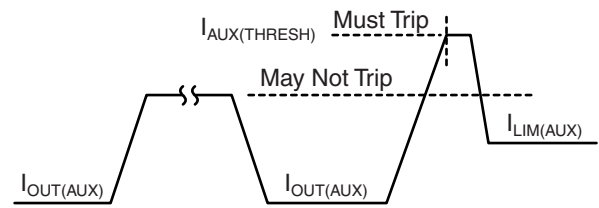


Figure 4. VAUX Current Limit Threshold

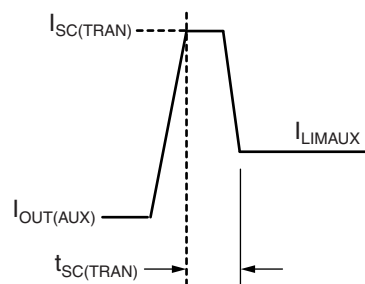


Figure 5. VAUX Current Limit Response Timing

## Functional Description

### Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages (“hot plugged”), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board’s supply pins. This transient inrush current can cause the system’s supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot plug event may cause permanent damage to connectors or on-board components.

The MIC2590B addresses these issues by limiting the inrush currents to the load (PCI Board), and thereby controlling the rate at which the load’s circuits turn on. In addition, the MIC2590B offers input and output voltage supervisory functions and current-limiting to provide robust protection for both the host system and the PCI board.

### System Interfaces

The MIC2590B employs two system interfaces. One is the hot plug Interface (HPI) which includes ON[A/B], AUXEN[A/B], and /FAULT[A/B]. The other is the System Management Interface (SMI) consisting of SDA, SCL and /INT, (whose signals conform to the specifications and format of Intel’s SMBus standard). The MIC2590B can be operated exclusively from the SMI, or can employ the HPI for power control while continuing to use the SMI for access to all but the power control registers.

In addition to the basic power control features of the MIC2590B accessible by the HPI, the SMI also gives the host access to the following information from the part:

1. Output voltage from each supply.
2. Output current from each supply.
3. Fault conditions occurring on each supply.

When using the System Management Interface for power control, do not use the hot plug Interface. Conversely, when using the HPI for power control, do not execute power control commands over the SMI bus (all other register accesses via the SMI bus remain permissible while in the HPI control mode). Note that if power control is performed via the SMI bus, the AUXENA, AUXENB, ONA and ONB pins should be tied to ground.

### Power-On Reset and Power Cycling

The MIC2590B utilizes VSTBY as the main supply input source. It is required for proper operation of the MIC2590B SMBus, registers and ADC and must be applied at all times. A Power-On Reset (POR) cycle is initiated after VSTBY rises above its UVLO threshold and remains valid at that voltage for 500µs. All internal registers except RESULT are cleared after POR. If VSTBY is recycled the MIC2590B enters a new power-on reset cycle. VSTBY must be the first supply input applied. Following the POR interval, the MAIN supply inputs of 12V<sub>IN</sub>, 12MV<sub>IN</sub>, 5V<sub>IN</sub> and 3V<sub>IN</sub> may be applied in any order. The SMBus is ready for access at the end of the POR interval. During t<sub>POR</sub> all outputs are off.

### Power-Up Cycle (See Typical Application Circuit)

When a slot is off, the 5VGATE and 3VGATE pins are held low with an internal pull-down current source. When a slot’s main outputs are enabled, and all input voltages are above their respective undervoltage lockout thresholds, all four main supplies execute a controlled turn on. At this time, the GATE voltages of the 5V and 3.3V MOSFETs are ramped at a controlled rate from 0V to approximately 11.5V. This is sufficient to fully enhance the external MOSFETs for lowest possible DC losses. The ramp rate is controlled by 25µA(typ.) current sources from the GATE pins charging each C<sub>GATE</sub>. The magnitude and slew rate of the output current is proportional to the value of C<sub>GATE</sub> and the load capacitance. The minimum value of C<sub>GATE</sub> is selected to ensure that during start-up the load current does not exceed the current-limit threshold. The following equation is used to determine the value of C<sub>GATE</sub>(min):

$$C_{GATE}(\text{min}) = \frac{I_{GATE}}{I_{LIM}} \times C_{LOAD}$$

Where C<sub>LOAD</sub> is the load capacitance connected to the 3.3V and 5V outputs and I<sub>LIM</sub> and I<sub>GATE</sub> are respectively the current-limit and gate charge current specifications as given in the Electrical Characteristics table. The output slew rate dv/dt is computed by:

$$dv / dt (\text{load}) = \frac{I_{GATE}}{C_{GATE} \times 10^6}$$

| I <sub>SLEW</sub> = 25µA |              |
|--------------------------|--------------|
| C <sub>GATE</sub>        | dv/dt (load) |
| 0.001µF                  | 25000V/s     |
| 0.01µF                   | 2500V/s      |
| 0.1µF                    | 250V/s       |
| 1µF                      | 25V/s        |

**Table 1. 3.3V/5V Output Slew Rate Selection**

For the +12V and –12V supplies, the output slew rate is controlled by capacitors connected to the 12VSLEWA and 12VSLEWB pins. To determine the minimum value of the slew rate capacitor, (C<sub>SLEW</sub>), connected to 12VSLEW[A/B], the following equation is used:

$$C_{SLEW}(\text{min}) = \frac{I_{SLEW}}{I_{LIM}} \times C_{LOAD}$$

where C<sub>LOAD</sub> is the load capacitance connected to the +12V and –12V outputs, and I<sub>LIM</sub> and I<sub>SLEW</sub> are respectively the current-limit and slew rate charge current values found in the Electrical Characteristics table. The equation above computes the minimum value to guarantee the device does not enter into current limit. The slew rate dv/dt is computed by:

$$dv / dt \text{ at load} = \frac{I_{SLEW}}{C_{SLEW} \times 10^6}$$

By appropriate selection of the value of C<sub>SLEW</sub>, it can be ensured that the magnitude of the inrush current never exceeds the current limit for a given load capacitance. Since

one capacitor fixes the slew rate for both +12V and -12V, the capacitor value should be chosen to provide the slower slew rate of the two. Table 2 depicts the output slew rate for various values of  $C_{SLEW}$ .

| $I_{SLEW} = 22\mu A$ |              |
|----------------------|--------------|
| $C_{GATE}$           | dv/dt (load) |
| 0.001 $\mu F$        | 22000V/s     |
| 0.01 $\mu F$         | 2200V/s      |
| 0.1 $\mu F$          | 220V/s       |
| 1 $\mu F$            | 22V/s        |

**Table 2.  $\pm 12V$  Output Slew Rate Selection**

### Power Down Cycle

When a slot is turned off, internal switches are connected to each of the outputs to discharge the PCI board's bypass capacitors to ground.

### Standby Mode

Standby mode is entered when any one (or more) enabled MAIN supply input(s) (12VIN, 12MVIN, 5VIN and 3VIN) drops below its respective UVLO threshold. The MIC2590B supplies two 3.3V auxiliary outputs, VAUX[A/B], satisfying PCI 2.2 specifications. These outputs are fed via the VSTBY input, and controlled by the AUXEN[A/B] inputs or via their SMI bus Control Registers. These outputs are independent of the MAIN outputs: should one or more of the MAIN supply inputs move below its UVLO thresholds, VAUX[A/B] still function as long as VSTBY is present. Prior to entering standby mode, ONA and ONB (or the MAINA and MAINB bits in the Control Registers) inputs should be de-asserted. If this is not done, the MIC2590B will assert /FAULT, and also /INT if interrupts are enabled, when the MIC2590B detects an undervoltage condition on a supply input.

### Circuit Breaker Functions

The MIC2590B provides an electronic circuit breaker function that protects against excessive loads such as short circuits at each supply. When the current from one or more of a slot's MAIN outputs exceeds the current limit threshold ( $50mV/R_{SENSE}$  for 3.3V and 5V, 1.0A for +12V, and/or 0.2A for -12V) for a duration greater than  $t_{FLT}$ , the circuit breaker is tripped and all MAIN supplies (all outputs except VAUX[A/B]) are shut off. Should the load current exceed  $I_{THFAST}$  (+12V and -12V), or cause a MAIN output's  $V_{SENSE}$  to exceed  $V_{THFAST}$  (+3.3V and +5V), the outputs are shut off with no delay. Undervoltage conditions on the MAIN supply inputs also trip the circuit breaker, but only when the MAIN outputs are enabled (to signal a supply input brown-out condition).

The VAUX[A/B] outputs have their own separate circuit breaker functions. VAUX[A/B] do not incorporate a fast-trip threshold, but instead regulate the output current into a fault to avoid exceeding their operating current limit. The circuit breaker will trip due to overcurrents on VAUX[A/B] when the fault timer expires. This use of the  $t_{FLT}$  timer prevents the circuit breaker from tripping prematurely due to brief current transients.

Following a fault condition, the outputs can be turned on again via the ON inputs (if the fault occurred on one of the MAIN outputs), via the AUXEN inputs (if the fault occurred on the AUX outputs), or by cycling both ON and AUXEN (if faults occurred on both the MAIN and AUX outputs). A fault condition can alternatively be cleared under SMI control of the ENABLE bits in the CNTRL[A/B] registers. When the circuit breaker trips, /FAULT[A/B] will be asserted if the outputs were enabled through the hot plug Interface (non-SMI mode) inputs. At the same time, /INT will be asserted (unless interrupts are masked). Note that /INT is de-asserted by writing a logic 1 back into the respective fault bit position(s) in the STAT[A/B] register or the Common Status Register.

$t_{FLT}$  is set by external capacitors,  $C_{FIL[A/B]}$ , connected to the CFILTER[A/B] pins. The equation below can be used to determine the capacitor value for a given duration of  $t_{FLT}$ :

$$C_{FIL} \cong 2.0\mu F \times \left( \frac{t_{FLT}}{1 \text{ second}} \right)$$

### Thermal Shutdown

The internal +12V, -12V and VAUX MOSFETs are protected against damage not only by current limiting, but by dual-mode over-temperature protection as well. Each slot controller on the MIC2590B is thermally isolated from the other. Should an overcurrent condition raise the junction temperature of one slot's controller and internal pass elements to 140°C, all of the outputs for that slot (including VAUX) will be shut off, and the slot's /FAULT output will be asserted. The other slot's operation will remain unaffected. However, should the MIC2590B's overall die temperature exceed 160°C, both slots (all outputs, including VAUXA and VAUXB) will be shut off, whether or not a current-limit condition exists. A 160°C overtemperature condition additionally sets the overtemperature bit (OT\_INT) in the Common Status Register.

**A/D Converter**

The MIC2590B has a 20-channel, 8-bit A/D converter capable of monitoring the output voltage and current of each supply. This information is available via the System Management Interface. The information is particularly intended for use by systems that support the IPMI standard, but may be used for any desired purpose.

**Interrupt Generation**

In the MIC2590B, the /INT pin can be asserted (driven low) whenever a fault condition trips the circuit breaker. The MIC2590B can thus operate in either polled mode or interrupt mode. In the polled mode, the Interrupt Mask bit in the Common Status Register should be set, to prevent the /INT pin from being asserted. Upon a circuit breaker fault event the appropriate status bit is also set in the corresponding status registers. In order to clear the status bit the system must write a logic 1 back to same bit in the status register. Upon occurrence of the write the /INT pin will be de-asserted (if interrupts were enabled), if no other interrupts are pending. This method of “echo reset” allows data to be retained in the status registers until such time as the system software is ready to deal with that data, and then to control the earliest time at which the next interrupt might occur.

**System Management Interface (SMI)**

The MIC2590B’s System Management Interface uses the Read\_Byte and Write\_Byte subset of the SMBus protocols to communicate with its host via the System Management Interface bus. Additionally, the /INT output signals the controlling processor that one or more events need attention, if an interrupt-driven architecture is used. Note that the MIC2590B does not participate in the SMBus Alert Response Address (ARA) portion of the SMBus protocol.

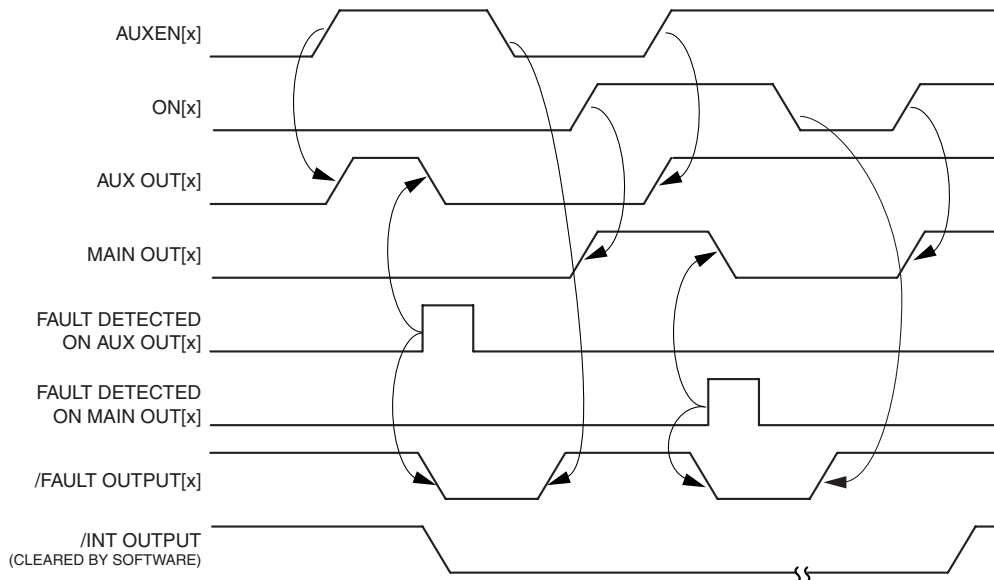
The SMBus Read\_Byte operation consists of sending the device’s slave address, followed by the target register’s internal address, and then clocking out the byte to be read from the target register. Similarly, the Write\_Byte operation consists of sending the device’s slave address, followed by the target register’s internal address, and then clocking in the byte to be written to the target register. The target register addresses for the MIC2590B are given in Table 4.

**MIC2590B SMBus Address Configuration**

The MIC2590B responds to its own unique address which is assigned using A2, A1 and A0. These represent the 3 LSBs of its 7-bit address, as shown in Table 3. These address bits are assigned only during power up of the VSTBY supply input. These three bits allow up to eight MIC2590B devices in a single system. These pins are either grounded or left unconnected to specify a logical 0 or 1 respectively. A pin designated as a logical 1 may also be pulled up to VSTBY.

| Inputs |    |    | MIC2590B Slave Address |                 |
|--------|----|----|------------------------|-----------------|
| A2     | A1 | A0 | Binary                 | Hex             |
| 0      | 0  | 0  | 1000 000 <sub>b</sub>  | 80 <sub>h</sub> |
| 0      | 0  | 1  | 1000 001 <sub>b</sub>  | 82 <sub>h</sub> |
| 0      | 1  | 0  | 1000 010 <sub>b</sub>  | 84 <sub>h</sub> |
| 0      | 1  | 1  | 1000 011 <sub>b</sub>  | 86 <sub>h</sub> |
| 1      | 0  | 0  | 1000 100 <sub>b</sub>  | 88 <sub>h</sub> |
| 1      | 0  | 1  | 1000 101 <sub>b</sub>  | 8A <sub>h</sub> |
| 1      | 1  | 0  | 1000 100 <sub>b</sub>  | 8C <sub>h</sub> |
| 1      | 1  | 1  | 1000 111 <sub>b</sub>  | 8E <sub>h</sub> |

**Table 3. MIC2590B SMBus Addressing**



**Figure 6. Hot Plug Interface Mode Operation**

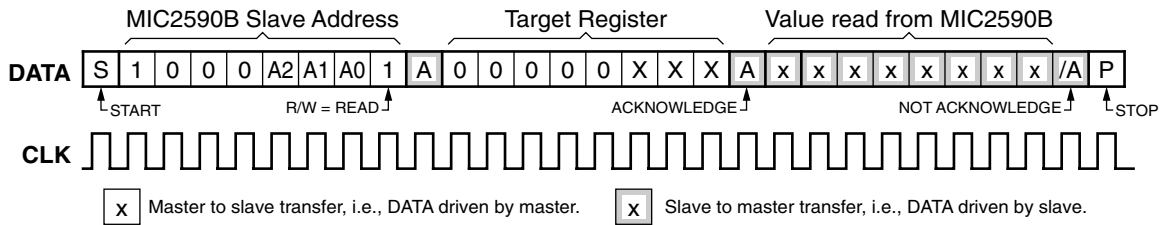


Figure 7. READ\_BYTE Protocol

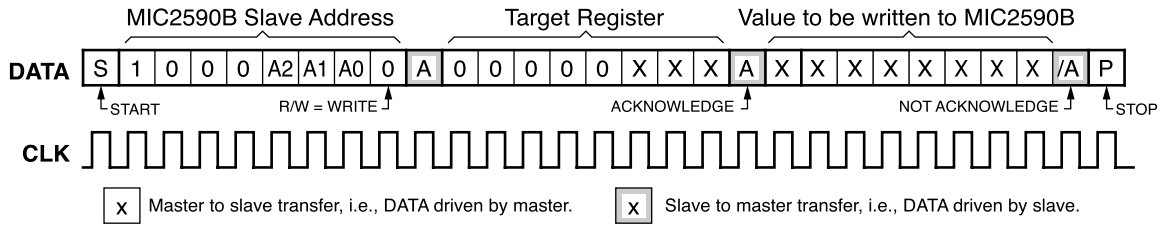


Figure 8. WRITE\_BYTE Protocol

Register Set and Programmer’s Model

| Target Register |                                | Command Byte Value |                 | Power-On Default |
|-----------------|--------------------------------|--------------------|-----------------|------------------|
| Label           | Description                    | Read               | Write           |                  |
| RESULT          | ADC Conversion Result Register | 00 <sub>h</sub>    | n/a             | n/a              |
| ADCNTRL         | ADC Control Register           | 01 <sub>h</sub>    | 01 <sub>h</sub> | 00 <sub>h</sub>  |
| CNTRLA          | Control Register Slot A        | 02 <sub>h</sub>    | 02 <sub>h</sub> | 00 <sub>h</sub>  |
| CNTRLB          | Control Register Slot B        | 03 <sub>h</sub>    | 03 <sub>h</sub> | 00 <sub>h</sub>  |
| STATA           | Slot A Status                  | 04 <sub>h</sub>    | 04 <sub>h</sub> | 00 <sub>h</sub>  |
| STATB           | Slot B Status                  | 05 <sub>h</sub>    | 05 <sub>h</sub> | 00 <sub>h</sub>  |
| STAT            | Common Status Register         | 06 <sub>h</sub>    | 06 <sub>h</sub> | 00 <sub>h</sub>  |

Table 4. MIC2590B Register Addresses

Detailed Register Descriptions below:

| Conversion Result Register (RESULT), 8-Bits Read Only |           |           |           |           |           |           |           |
|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| D[7]  | D[6]      | D[5]      | D[4]      | D[3]      | D[2]      | D[1]      | D[0]      |
| read-only   | read-only | read-only | read-only | read-only | read-only | read-only | read-only |
| Voltage or Current Data from ADC                      |           |           |           |           |           |           |           |

| Bit    | Function               | Operation |
|--------|------------------------|-----------|
| D[7:0] | Measured data from ADC | Read Only |

**Power-Up Default Value:** Undefined following POR

**Read Command Byte:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

| ADC Control Register (ADCNTRL), 8-Bits Read/Write |           |           |            |            |                        |            |            |
|---|-----------|-----------|------------|------------|------------------------|------------|------------|
| D[7]  | D[6]      | D[5]      | D[4]       | D[3]       | D[2]                   | D[1]       | D[0]       |
| read-only   | read-only | read-only | read-write | read-write | read-write             | read-write | read-write |
| BUSY  | Reserved  | Reserved  | SEL        | PAR        | Supply Select SUP[2:0] |            |            |

| Bit(s)   | Function                                 | Operation  |
|----------|--|--|
| BUSY     | ADC Status                               | 0 = ADC Quiescent<br>1 = ADC Busy  |
| D[6]     | Reserved                                 | Always Read As Zero  |
| D[5]     | Reserved                                 | Always Read As Zero  |
| SEL      | A/D Slot Select                          | Specifies Channel for A/D Conversion<br>0 = Slot A, 1 = Slot B   |
| PAR      | Parameter Control Bit for ADC Conversion | 1 = Voltage<br>0 = Current   |
| SUP[2:0] | Supply Select for ADC Conversion         | 000 = No Conversion<br>001 = 3.3V Supply<br>010 = 5.0V Supply<br>011 = +12V Supply<br>100 = -12V Supply<br>101 = VAUX Supply |

**Power-Up Default Value:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

**Command Byte (R/W):** 0000 0001<sub>b</sub> = 01<sub>h</sub>

To operate the ADC the ADCNTRL register must first be initialized by selecting a slot, specifying whether voltage or current is to be measured and then specifying the specific supply that is to be monitored. The software must then wait 100ms, or poll the BUSY bit until it is zero. The RESULT register will then contain the valid result of the conversion.

| Control Register, Slot A (CNTRLA), 8-Bits Read/Write |           |           |           |           |           |            |            |
|--|-----------|-----------|-----------|-----------|-----------|------------|------------|
| D[7]   | D[6]      | D[5]      | D[4]      | D[3]      | D[2]      | D[1]       | D[0]       |
| read-only  | read-only | read-only | read-only | read-only | read-only | read-write | read-write |
| AUXAPG   | MAINAPG   | Reserved  | Reserved  | Reserved  | Reserved  | MAINA      | VAUXA      |

| Bit(s)  | Function                              | Operation  |
|---------|---------------------------------------|--|
| AUXAPG  | AUX Output Power-Good Status, Slot A  | 1 = Power-Good (VAUXA output is above its $V_{UVTH}$ threshold)      |
| MAINAPG | MAIN Output Power-Good Status, Slot A | 1 = Power-Good (MAINA outputs are above their $V_{UVTH}$ thresholds) |
| D[5]    | Reserved                              | Always Read As Zero  |
| D[4]    | Reserved                              | Always Read As Zero  |
| D[3]    | Reserved                              | Always Read As Zero  |
| D[2]    | Reserved                              | Always Read As Zero  |
| MAINA   | MAIN Enable Control, Slot A           | 0 = OFF, 1 = ON  |
| VAUXA   | VAUX Enable Control, Slot A           | 0 = OFF, 1 = ON  |

**Power-Up Default Value:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

**Command Byte (R/W):** 0000 0010<sub>b</sub> = 02<sub>h</sub>

The power-up default value is 00h. Slot A is disabled upon power-up, i.e., all supply outputs are off.

| Control Register, Slot B (CNTRLB), 8-Bits Read/Write |           |           |           |           |           |            |            |
|--|-----------|-----------|-----------|-----------|-----------|------------|------------|
| D[7]   | D[6]      | D[5]      | D[4]      | D[3]      | D[2]      | D[1]       | D[0]       |
| read-only  | read-only | read-only | read-only | read-only | read-only | read-write | read-write |
| AUXBPG   | MAINBPG   | Reserved  | Reserved  | Reserved  | Reserved  | MAINB      | VAUXB      |

| Bit(s)  | Function                              | Operation  |
|---------|---------------------------------------|--|
| AUXBPG  | AUX Output Power-Good Status, Slot B  | 1 = Power-Good (VAUXB output is above its $V_{UVTH}$ threshold)      |
| MAINBPG | MAIN Output Power-Good Status, Slot B | 1 = Power-Good (MAINB outputs are above their $V_{UVTH}$ thresholds) |
| D[5]    | Reserved                              | Always Read As Zero  |
| D[4]    | Reserved                              | Always Read As Zero  |
| D[3]    | Reserved                              | Always Read As Zero  |
| D[2]    | Reserved                              | Always Read As Zero  |
| MAINB   | MAIN Enable Control, Slot B           | 0 = OFF, 1 = ON  |
| VAUXB   | VAUX Enable Control, Slot B           | 0 = OFF, 1 = ON  |

**Power-Up Default Value:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

**Command Byte (R/W):** 0000 0011<sub>b</sub> = 03<sub>h</sub>

The power-up default value is 00h. Slot B is disabled upon power-up, i.e., all supply outputs are off.

| Status Register, Slot A (STATA), 8-Bits Read Only |                   |                   |                    |                    |                    |                    |                    |
|---|-------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| D[7]<br>read-only                                 | D[6]<br>read-only | D[5]<br>read-only | D[4]<br>read-write | D[3]<br>read-write | D[2]<br>read-write | D[1]<br>read-write | D[0]<br>read-write |
| FAULTA  | MAINA             | VAUXA             | VAUXAF             | 12MVAF             | 12VAF              | 5VAF               | 3VAF               |

| Bit(s) | Function                      | Operation  |
|--------|-------------------------------|--|
| FAULTA | FAULT Pin Status, Slot A      | <b>Notes 1 &amp; 2</b>   |
| MAINA  | MAIN Enable Status, Slot A    | Represents actual state (on/off) of the four main power outputs for Slot A. (+12V, +5V, +3.3V and -12V)<br>1 = MAIN Power On<br>0 = MAIN Power Off |
| VAUXA  | VAUX Enable Status Slot A     | Represents actual state (on/off) of the auxiliary power outputs for Slot A.<br>1 = AUX Power On<br>0 = AUX Power Off                               |
| VAUXFA | Overcurrent Fault VAUX Supply | 1 = Fault; 0 = No Fault  |
| 12MVFA | Overcurrent Fault -12V Supply | 1 = Fault; 0 = No Fault  |
| 12VFA  | Overcurrent Fault +12V Supply | 1 = Fault; 0 = No Fault  |
| 5VFA   | Overcurrent Fault 5V Supply   | 1 = Fault; 0 = No Fault  |
| 3VFA   | Overcurrent Fault 3.3V Supply | 1 = Fault; 0 = No Fault  |

**Power-Up Default Value:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

**Read Command Byte (R/W):** 0000 0100<sub>b</sub> = 04<sub>h</sub>

The power-up default value is 00<sub>h</sub>. The slot is disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and de-assert /INT. The status of the /FAULTA pin is not affected by reading the Status Register.

**Note 1.** 1 = /FAULT[A/B] pin asserted, indicating a fault condition (/FAULT is LOW).

0 = /FAULT[A/B] pin is de-asserted (/FAULT is HIGH).

If FAULT[A/B] has been set by an overcurrent condition on one (or more) of the main outputs, the corresponding ON[A/B] must go LOW to reset FAULT. If FAULT[A/B] has been set by an overcurrent on a VAUX output, the corresponding AUXEN[A/B] must go LOW to reset FAULT. If an overcurrent has occurred on both a main output and VAUX output of a slot, both ON[A/B] and AUXEN[A/B] of the corresponding slot must go LOW to reset FAULT.

**Note 2.** The FAULT bits, and the /FAULT pins, are not active when the MIC2590B power paths are controlled by the System Management Interface (SMBus). When using SMI power path control for a slot, the AUXEN and ON pins for that slot must be tied to ground.

| Status Register, Slot B (STATB), 8-Bits Read Only |                   |                   |                    |                    |                    |                    |                    |
|---|-------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| D[7]<br>read-only                                 | D[6]<br>read-only | D[5]<br>read-only | D[4]<br>read-write | D[3]<br>read-write | D[2]<br>read-write | D[1]<br>read-write | D[0]<br>read-write |
| FAULTB  | MAINB             | VAUXB             | VAUXAF             | 12MVAF             | 12VAF              | 5VAF               | 3VAF               |

| Bit(s) | Function                      | Operation  |
|--------|-------------------------------|--|
| FAULTB | FAULT Pin Status, Slot B      | <b>Notes 1 &amp; 2</b>   |
| MAINB  | MAIN Enable Status, Slot B    | Represents actual state (on/off) of the four main power outputs for Slot B. (+12V, +5V, +3.3V and -12V)<br>1 = MAIN Power On<br>0 = MAIN Power Off |
| VAUXB  | VAUX Enable Status Slot B     | Represents actual state (on/off) of the auxiliary power outputs for Slot B.<br>1 = AUX Power On<br>0 = AUX Power Off                               |
| VAUXFB | Overcurrent Fault VAUX Supply | 1 = Fault; 0 = No Fault  |
| 12MVFB | Overcurrent Fault -12V Supply | 1 = Fault; 0 = No Fault  |
| 12VFB  | Overcurrent Fault +12V Supply | 1 = Fault; 0 = No Fault  |
| 5VFB   | Overcurrent Fault 5V Supply   | 1 = Fault; 0 = No Fault  |
| 3VFB   | Overcurrent Fault 3.3V Supply | 1 = Fault; 0 = No Fault  |

**Power-Up Default Value:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

**Read Command Byte (R/W):** 0000 0101<sub>b</sub> = 05<sub>h</sub>

The power-up default value is 00<sub>h</sub>. The slot is disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and de-assert /INT. The status of the /FAULTB pin is not affected by reading the Status Register.



| Common Status Register, (STAT), 8-Bits Read/Write |                   |                   |                   |                    |                    |                    |                   |
|---|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|-------------------|
| D[7]<br>read-only                                 | D[6]<br>read-only | D[5]<br>read-only | D[4]<br>read-only | D[3]<br>read-write | D[2]<br>read-write | D[1]<br>read-write | D[0]<br>read-only |
| Reserved  | Reserved          | GPIB              | GPIA              | INTMSK             | UV_INT             | OT_INT             | Reserved          |

| Bit(s) | Function                      | Operation   |
|--------|-------------------------------|---|
| D[7]   | Reserved                      | Always read as zero   |
| D[6]   | Reserved                      | Always read as zero   |
| GPIB   | General Purpose Input, Slot B | State of GPIB pin   |
| GPIA   | General Purpose Input, Slot A | State of GPIA pin   |
| INTMSK | Interrupt Mask                | 0 = /INT generation is enabled; 1 = /INT generation is disabled. The MIC2590B does not participate in the SMBus Alert Response Address (ARA) Protocol.  |
| UV_INT | Undervoltage Interrupt        | Set whenever a circuit breaker fault condition occurs as a result of an undervoltage lockout condition on one of the main supply inputs. This bit is only set if a UVLO condition occurs while one or both of the ON[A/B] pins are asserted or the MAIN[A/B] enable control bits are set. |
| OT_INT | Overtemperature Interrupt     | Set whenever a circuit breaker fault occurs as a result of an over-temperature condition exceeding 160°C shutting both channels off.  |
| D[0]   | Reserved                      | Read Undefined  |

**Power-Up Default Value:** 0000 0000<sub>b</sub> = 00<sub>h</sub>

**Command Byte (R/W):** 0000 0110<sub>b</sub> = 06<sub>h</sub>

To reset the OT\_INT and UV\_INT fault bits a logical 1 must be written back to these bits.

## Application Information

### Current Sensing

For the three power supplies switched with internal MOSFETs (+12V, -12V, and  $V_{AUX}$ ), the MIC2590B provides all necessary current sensing functions to protect the IC, the load, and the power supply. For the remaining four supplies which the part is designed to control, the high currents at which these supplies typically operate makes sensing the current inside the MIC2590B impractical. Therefore, each of these supplies (3VA, 5VA, 3VB, and 5VB) requires an external current sensing resistor. The  $V_{IN}$  connection to the IC from each supply (e.g., 5VINA) is connected to the positive terminal of the slot's current sense amplifier, and the corresponding SENSE input (in this case, 5VSENSEA) is connected to the negative terminal of the current sense amplifier.

### Sense Resistor Selection

The MIC2590B uses low-value sense resistors to measure the current flowing through the MOSFET switches to the loads. These sense resistors are nominally valued at  $50\text{m}\Omega/I_{LOAD(CONT)}$ . To accommodate worst-case tolerances for both the sense resistor, (allow  $\pm 3\%$  over time and temperature for a resistor with  $\pm 1\%$  initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used.

The current limit threshold voltage (the "trip point") for the MIC2590B may be as low as 35mV, which would equate to a sense resistor value of  $35\text{m}\Omega/I_{LOAD(CONT)}$ . Carrying the numbers through for the case where the value of the sense resistor is 3% high, this yields:

$$R_{SENSE} = \frac{35\text{m}\Omega}{(1.03)(I_{LOAD(CONT)})} = \frac{34\text{m}\Omega}{I_{LOAD(CONT)}}$$

Once the value of  $R_{SENSE}$  has been chosen in this manner, it is good practice to check the maximum  $I_{LOAD(CONT)}$  which the circuit may let through in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum is found using a 65mV trip voltage and a sense resistor which is 3% low in value. The resulting current is:

$$I_{LOAD(CONT, MAX)} = \frac{65\text{mV}}{(0.97)(R_{SENSE(NOM)})} = \frac{67\text{mV}}{R_{SENSE(NOM)}}$$

As an example, if an output must carry a continuous 4.4A without nuisance trips occurring,  $R_{SENSE}$  for that output should be  $34\text{m}\Omega/4.4\text{A} = 7.73\text{m}\Omega$ . The nearest standard value is  $7.5\text{m}\Omega$ , so a  $7.5\text{m}\Omega \pm 1\%$  resistor would be a good choice. At the other set of tolerance extremes,  $I_{LOAD(CONT, MAX)}$  for the output in question is then simply  $67\text{mV}/7.5\text{m}\Omega = 8.93\text{A}$ . Knowing this final datum, we can determine the necessary wattage of the sense resistor, using  $P = I^2R$ . Here  $I$  will be  $I_{LOAD(CONT, MAX)}$ , and  $R$  will be  $(0.97)(R_{SENSE(NOM)})$ . These numbers yield the following:

$$P_{MAX} = (8.93\text{A})^2(7.28\text{m}\Omega) = 0.581\text{W}$$

A 1.0W sense resistor would work well in this application.

### Kelvin Sensing

Because of the low values of the sense resistors, special care must be used to accurately measure the voltage drop across them. Specifically, the voltage across each  $R_{SENSE}$  must employ Kelvin sensing. This is simply a means of making sure that any voltage drops in the power traces connecting to the resistors are not picked up in addition to the voltages across the sense resistors themselves. If accuracy must be paid for, it's worth keeping.

Figure 9 illustrates how Kelvin sensing is performed. As can be seen, all the high current in the circuit (let us say, from +5VINA through  $R_{SENSE}$  and then to the drain of the +5VA output MOSFET) flows directly through the power PCB traces and  $R_{SENSE}$ . The voltage drop resulting across  $R_{SENSE}$  is sampled in such a way that the high currents through the power traces will not introduce any extraneous IR drops.

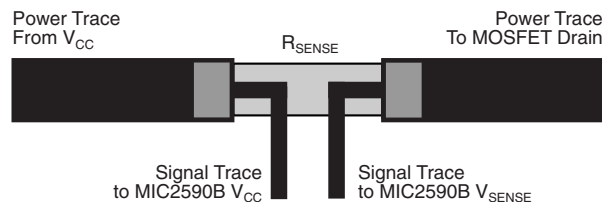


Figure 9. Kelvin Sensing Connections for  $R_{SENSE}$

### MOSFET Selection

Selecting the proper MOSFET for use as current pass and switching element for each of the 3V and 5V slots of the MIC2590B involves four straightforward tasks:

1. Choice of a MOSFET which meets the minimum voltage requirements.
2. Determination of maximum permissible on-state resistance [ $R_{D-S(ON)}$ ].
3. Selection of a device to handle the maximum continuous current (steady-state thermal issues).
4. Verification of the selected part's ability to withstand current peaks (transient thermal issues).

### MOSFET Voltage Requirements

The first voltage requirement for each MOSFET is easily stated: the drain-source breakdown voltage of the MOSFET must be greater than  $V_{IN(MAX)}$  for the slot in question. For instance, the 5V input may reasonably be expected to see high-frequency transients as high as 5.5V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 6V.

The second breakdown voltage criteria which must be met is a bit subtler than simple drain-source breakdown voltage, but is not hard to meet. Low-voltage MOSFETs generally have low breakdown voltage ratings from gate to source as well. In MIC2590B applications, the gates of the external MOSFETs are driven from the +12V input to the IC. That supply may well be at  $12\text{V} + (5\% \times 12\text{V}) = 12.6\text{V}$ . At the same time, if the output of the MOSFET (its source) is suddenly shorted to ground, the gate-source voltage will go to  $(12.6\text{V} - 0\text{V}) = 12.6\text{V}$ . This

means that the external MOSFETs must be chosen to have a gate-source breakdown voltage in excess of 13V; after 12V absolute maximum the next commonly available voltage class has a permissible gate-source voltage of 20V maximum. This is a very suitable class of device. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source breakdown rating or higher. As a general tip, look to surface mount devices with a drain-source rating of 30V as a starting point.

### MOSFET Maximum On-State Resistance

The MOSFETs in the +3.3V and +5V MAIN power paths will have a finite voltage drop, which must be taken into account during component selection. A suitable MOSFET's data sheet will almost always give a value of on resistance for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on resistance of the device with 7 Volts of enhancement (keep this in mind; we'll use it in the following Thermal Issues sections). The resulting value is conservative, but close enough. Call this value  $R_{ON}$ . Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that is required to calculate the voltage drop across the MOSFET is to multiply the maximum current times the MOSFET's  $R_{ON}$ . The one addendum to this is that MOSFETs have a slight increase in  $R_{ON}$  with increasing die temperature. A good approximation for this value is 0.5% increase in  $R_{ON}$  per °C rise in junction temperature above the point at which  $R_{ON}$  was initially specified by the manufacturer. For instance, the Vishay (Siliconix) Si4430DY, which is a commonly used part in this type of application, has a specified  $R_{DS(ON)}$  of 8.0mΩ max. at  $V_{G-S} = 4.5V$ , and  $R_{DS(ON)}$  of 4.7mΩ max. at  $V_{G-S} = 10V$ . Then  $R_{ON}$  is calculated as:

$$R_{ON} = \frac{(4.7m\Omega + 8.0m\Omega)}{2} = 6.35m\Omega$$

at 25°C  $T_J$ . If the actual junction temperature is estimated to be 110°C, a reasonable approximation of  $R_{ON}$  for the Si4430DY at temperature is:

$$6.35m\Omega \left[ 1 + (110^\circ - 25^\circ) \left( \frac{0.5\%}{^\circ C} \right) \right] = 6.35m\Omega \left[ 1 + (85^\circ) \left( \frac{0.5\%}{^\circ C} \right) \right] \cong 9.05m\Omega$$

Note that this is not a closed-form equation; if more precision were required, several iterations of the calculation might be necessary. This is demonstrated in the section "MOSFET Transient Thermal Issues."

For the given case, if Si4430DY is operated at an  $I_{DRAIN}$  of 7.6A, the voltage drop across the part will be approximately  $(7.6A)(9.05m\Omega) = 69mV$ .

### MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of  $I_{LOAD(CONT, MAX)}$  for the output in question (see Sense Resistor Selection).
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., Can heat be dissipated into the ground plane or power plane, if using a surface mount part? Is any airflow available?).

Now it gets easy: steady-state power dissipation is found by calculating  $I^2R$ . As noted in "MOSFET Maximum On-State Resistance," above, the one further concern is the MOSFET's increase in  $R_{ON}$  with increasing die temperature. Again, use the Si4430DY MOSFET as an example, and assume that the actual junction temperature ends up at 110°C. Then  $R_{ON}$  at temperature is again approximately 9.05mΩ. Again, allow a maximum  $I_{DRAIN}$  of 7.6A:

$$\text{Power dissipation} \cong I_{DRAIN}^2 \times R_{ON} = (7.6A)^2 \times 9.05m\Omega \cong 0.523W$$

The next step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Formally put, the steady-state electrical model of power dissipated at the MOSFET junction is analogous to a current source, and anything in the path of that power being dissipated as heat into the environment is analogous to a resistor. It's therefore necessary to verify that the thermal resistance from the junction to the ambient is equal to or lower than that value of thermal resistance (often referred to as  $R_{\theta(JA)}$ ) for which the operation of the part is guaranteed. As an applications issue, surface mount MOSFETs are often less than ideally specified in this regard—it's become common practice simply to state that the thermal data for the part is specified under the conditions "Surface mounted on FR-4 board,  $t \leq 10$ seconds," or something equally mystifying. So here are a few practical tips:

1. The heat from a surface mount device such as an SO-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more of copper the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.
2. Since the rating for the part is given as "for 10 seconds," derate the maximum junction temperature by 35°C. This is the standard good practice derating of 25°C, plus another 10°C to allow for the time element of the specification.
3. Airflow, if available, works wonders. This is not the place for a dissertation on how to perform airflow calculations, but even a few LFM (linear feet per minute) of air will cool a MOSFET down

dramatically. If you can position the MOSFET(s) in question near the inlet of a power supply's fan, or the outlet of a processor's cooling fan, that's always a good free ride.

- Although it seems a rather unsatisfactory statement, the best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. The ideal evaluation is in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or in infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

### MOSFET Transient Thermal Issues

Having chosen a MOSFET that will withstand the imposed voltage stresses, and be able to handle the worst-case continuous  $I^2R$  power dissipation which it will see, it remains only to verify the MOSFET's ability to handle short-term overload power dissipation without overheating. Here, nature and physics work in our favor: a MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, semiconductor devices (silicon die, lead frames, etc.) have thermal inertia. This is easily understood by all of us who have stood waiting for a pot of water to boil.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance." Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve, which is a handy tool for making sure that you can safely get by with a less expensive MOSFET than you thought you might need. For example, take the case where  $t_{FLT}$  for the 5V supply has been set to 50ms,  $I_{LOAD(CONT, MAX)}$  is 5.0A, the slow-trip threshold is 50mV nominal, and the fast-trip threshold is 100mV. If the output is connected to a 0.60Ω load, the output current from the MOSFET for the slot in question will be regulated to 5.0A for 50ms before the part's circuit breaker trips. During that time, the dissipation in the MOSFET is given by:

$$P = E \times I \quad E_{MOSFET} = [5V - 5A(0.6\Omega)] = 2V$$

$$P_{MOSFET} = (2V \times 5A) = 10W \text{ for } 50ms$$

Wow! Looks like we need a really hefty MOSFET to withstand just this unlikely—but plausible enough to protect against—fault condition. Or do we? This is where the transient thermal impedance curves become very useful. Figure 10 shows those curves for the Vishay (Siliconix) Si4430DY, a commonly used SO-8 power MOSFET.

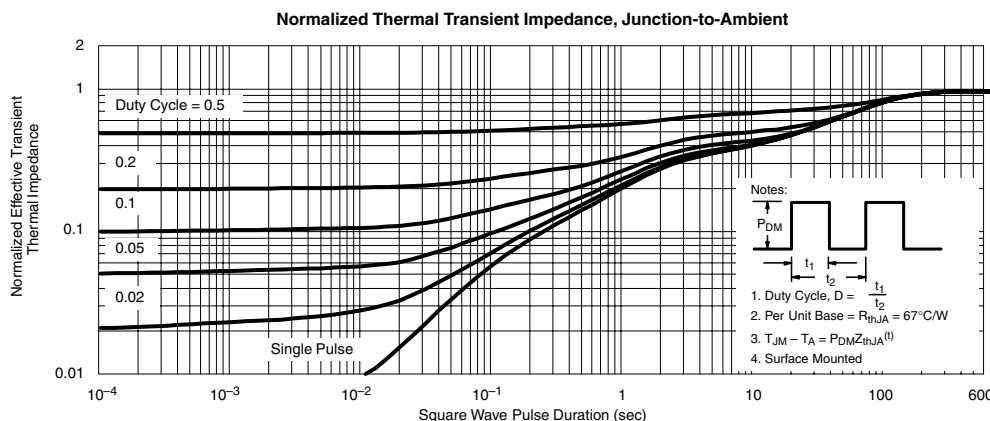


Figure 10. Si4430DY MOSFET Transient Thermal Impedance Curve

Using this graph is not nearly as daunting as it may at first appear. Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be a long time, 10 minutes or more, before the fault is isolated and the slot is reset. In such a case, we can approximate this as a "single pulse" event, that is to say, there's no significant duty cycle. Then, reading up from the X-axis at the point where "Square Wave Pulse Duration" is equal to 0.1sec (=100ms), we see that the effective thermal impedance of this MOSFET

to a single pulse event of this duration is only 6% of its continuous  $R_{\theta(JA)}$ .

This particular part is specified as having an  $R_{\theta(JA)}$  of 50°C/W for intervals of 10 seconds or less. So, some further math, just to get things ready for the finale:

Assume  $T_A = 55^\circ\text{C}$  maximum, 1 square inch of copper at the drain leads, no airflow.

Assume the MOSFET has been carrying just about 5A for some time.

Then the starting (steady-state)  $T_J$  is:

$$T_J \cong 55^\circ\text{C} + (7.3\text{m}\Omega)(5\text{A})^2(30^\circ\text{C}/\text{W})$$

$$T_J \cong 60.5^\circ\text{C}$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with  $T_J$  equal to the already calculated value of  $67^\circ\text{C}$ :

$$R_{\text{ON}} \text{ at } T_J = 60.5^\circ\text{C} = [1 + (60.5^\circ\text{C} - 25^\circ)(0.5\%/^\circ\text{C})] \times 6.35\text{m}\Omega$$

$$R_{\text{ON}} \text{ at } T_J = 60.5^\circ\text{C} \cong 7.48\text{m}\Omega$$

$$T_J \cong 55^\circ\text{C} + (7.3\text{m}\Omega)(5\text{A})^2(30^\circ\text{C}/\text{W})$$

$$T_J \cong 60.6^\circ\text{C}$$

At this point, the simplest thing to do is to approximate  $T_J$  as  $61^\circ\text{C}$ , which will be close enough for all practical purposes.

Finally, add  $(10\text{W})(67^\circ\text{C}/\text{W})(0.03) = 21^\circ\text{C}$  to the steady-state  $T_J$  to get  $T_{J(\text{TRANSIENT MAX})} = 82^\circ\text{C}$ . The Si4430DY can easily handle this value of  $T_{J(\text{MAX})}$ .

A second illustration of the use of the transient thermal impedance curves: assume that the system will attempt multiple retries on a slot showing a fault, with a one second interval between retry attempts. This frequency of restarts will significantly increase the dissipation in the Si4430DY MOSFET. Will

the MOSFET be able to handle the increased dissipation? We get the following:

The same part is operating into a persistent fault, so it is cycling in a square-wave fashion (no steady-state load) with a duty cycle of (50msec/second = 0.05).

On the Transient Thermal Impedance Curves, read up from the X-axis to the line showing Duty Cycle equaling 0.05. The effective  $R_{\theta(\text{JA})} = (0.7 \times 67^\circ\text{C}/\text{W}) = 4.7^\circ\text{C}/\text{W}$ .

Calculating the peak junction temperature:

$$T_{J(\text{PEAK MAX})} = [(10\text{W})(4.7^\circ\text{C}/\text{W}) + 55^\circ\text{C}] = 102^\circ\text{C}$$

And finally, checking the RMS power dissipation just to be complete:

$$P_{\text{RMS}} = (5\text{A})^2(7.47\text{m}\Omega)\sqrt{0.05} = 0.042\text{W}$$

which will result in a negligible temperature rise.

The Si4430DY is electrically and thermally suitable for this application.

### MOSFET and Sense Resistor Selection Guide

Listed below, by Manufacturer and Type Number, are some of the more popular MOSFET and resistor types used in PCI hot plug applications. Although far from comprehensive, this information will constitute a good starting point for most designs.

| MOSFET Vendors          | Key MOSFET Type(s)   | Web Address           |
|-------------------------|--|-----------------------|
| Vishay (Siliconix)      | Si4430DY ("LittleFoot" Series)<br>Si4420DY ("LittleFoot" Series)                           | www.siliconix.com     |
| International Rectifier | IRF7413A (SO-8 package part)<br>Si4420DY (second source to Vishay)                         | www.irf.com           |
| Fairchild Semiconductor | FDS6644 (SO-8 package part)<br>FDS6670A (SO-8 package part)<br>FDS6688 (SO-8 package part) | www.fairchildsemi.com |

| Resistor Vendors | Sense Resistors  | Web Address   |
|------------------|--|---|
| Vishay (Dale)    | "WSL" Series   | www.vishay.com/docs/wsl_30100.pdf                           |
| IRC              | "OARS" Series<br>"LR" Series<br>(second source to "WSL") | irctt.com/pdf_files/OARS.pdf<br>irctt.com/pdf_files/LRC.pdf |

### Power Supply Decoupling

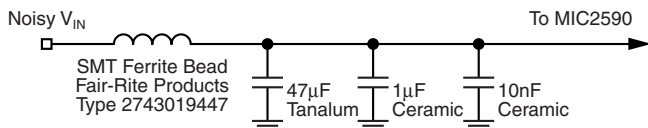
In general, prudent system design requires that power supplies used for logic functions should have less than 100mV of noise at frequencies of 100kHz and above. This is especially true given the speeds of modern logic families, such as the 1.2 micron CMOS used in the MIC2590B. In particular, the  $-12\text{V}$  supply should have less than 100mV of peak-to-peak noise at frequencies of 1MHz or higher. This is because the  $-12\text{V}$  supply is the most negative potential applied to the IC, and is therefore connected to the device's substrate. All of the subcircuits integrated onto the silicon chip are hence subjected by capacitances coupling to any HF noise on the  $-12\text{V}$  supply. While individual capacitances are quite low, the amount of injected energy required to cause a "glitch" can

also be quite low at the internal nodes of high speed logic circuits.

Less obviously, but equally important, is the fact that the internal charge pump for the 3.3VAUX supplies is somewhat susceptible to noise on the  $+12\text{V}$  input when that input is at or near zero volts. The  $+12\text{V}$  supply should not carry HF noise in excess of 200mV peak-to-peak with respect to chip ground when it is in the "off" state.

If either the  $-12\text{V}$  input, the  $+12\text{V}$  input, or both supplies do carry significant HF noise (as can happen when they are locally derived by a switching converter), the solution is both small and inexpensive. An LC filter made of a ferrite bead between the noisy power supply input and the MIC2590B,

followed by a "composite capacitor" from the affected MIC2590B input pin to ground will suffice for almost any situation. A good composite capacitor for this purpose is the parallel combination of a 47 $\mu$ F tantalum bulk decoupling capacitor, and one each 1 $\mu$ F and 0.01 $\mu$ F ceramic capacitors for high-frequency bypass. A suggested ferrite bead for such use is Fair-Rite Products Corporation part number 2743019447 (this is a surface-mountable part). Similar parts from other vendors will also work well, or a 0.27 $\mu$ H, air-core coil can be used.



**Figure 11. Filter Circuit for Noisy Supplies (+3.3V and/or -12V)**

It is theoretically possible that high-amplitude, HF noise reflected back into one or both of the MIC2590B's -12V outputs could interfere with proper device operation, although such noisy loads are unlikely to occur in the real world. If this becomes an application-specific concern, a pair of filters similar to that in Figure 11 will provide the required HF bypassing. The capacitors would be connected to the MIC2590B's -12V output pins, and the ferrite beads would be placed between the -12V output pins and the loads.

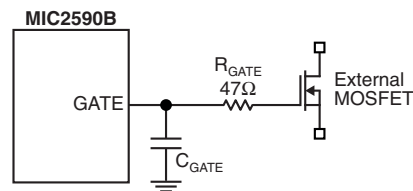
#### -12V Input Clamp Diode

The -12V input to the MIC2590B is the most negative potential on the part, and is therefore connected to the chip's substrate (as described in "Power Supply Decoupling," above). Although no particular sequencing of the -12V supply relative to the other MIC2590B supplies is required for normal operation, this substrate connection does mean that the -12V input must never exceed the voltage on the GROUND pin of the IC by more than 0.3 volts. In some systems, even though the -12V supply will discharge towards ground potential when it is turned OFF, the possibility exists that power supply output ringing or  $L(di/dt)$  effects in the wiring and on the PCB itself will cause brief transient voltages in excess of +0.3V to appear at the -12V input. The simplest way to deal

with such a transient is to clamp it with a Schottky diode. The diode's anode should be physically placed directly at the -12V input to the MIC2590B, and its cathode should have as short a path as possible back to the part's ground. A good SMT part for this application is ON Semiconductor's type MBRS140T3 (1A, 40V). Although the 40V rating of this part is a bit gratuitous, it is an inexpensive industry-standard part with many second sources. Unless it is absolutely known in advance that the voltage on the "-12V" inputs will never exceed 0.0V at the IC's -12V input pins, it's wise to at least leave a position for this diode in the board layout and then remove it later. This final determination should be made by observations of the voltage at the -12V input with a fast storage oscilloscope, under turn-on and turn-off conditions.

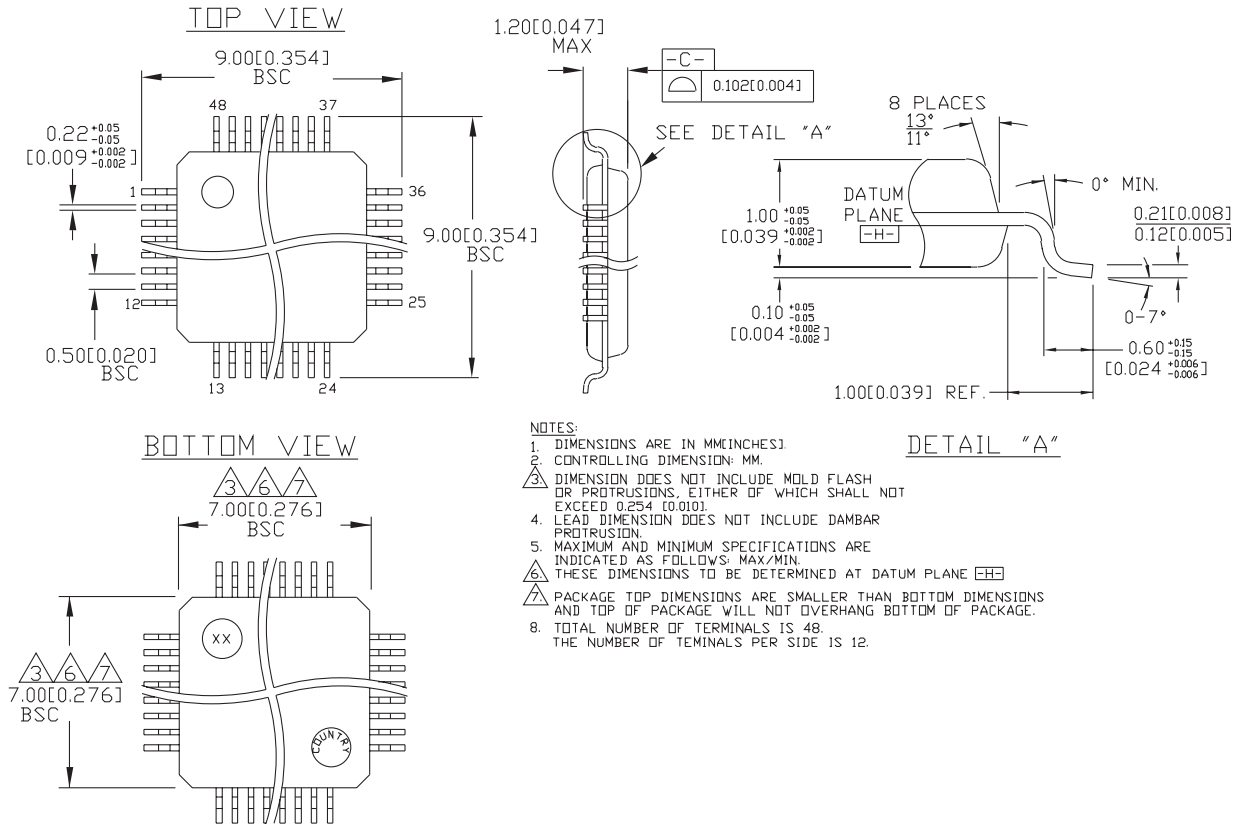
#### Gate Resistor Guidelines

The MIC2590B controls four external power MOSFETs, which handle the high currents for each of the two 3.3V and 5V outputs. A capacitor ( $C_{GATE}$ ) is connected in the application circuit from each GATE pin of the MIC2590B to ground. Each  $C_{GATE}$  controls the ramp-up rate of its respective power output (e.g., 5VOUTB). These capacitors, which are typically in the 10nF range, cause the GATE outputs of the MIC2590B to have very low AC impedances to ground at any significant frequency. It is therefore necessary to place a modest value of gate damping resistance ( $R_{GATE}$ ) between each  $C_{GATE}$  and the gate of its associated MOSFET. These resistances prevent high-frequency MOSFET source-follower oscillations from occurring. The exact value of the resistors used is not critical; 47 $\Omega$  is usually a good choice. Each  $R_{GATE}$  should be physically located directly adjacent to the MOSFET gate lead to which it connects.



**Figure 12. Proper Connection of  $C_{GATE}$  and  $R_{GATE}$**

Package Information



48-Pin TQFP (BTQ)

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