

### FEATURES

#### Four inputs, one output DVI/HDMI links:

- Four TMDS channels per link
- Supports 250Mbps to 1.65Gbps data rates
- Supports 25MHz to 165MHz pixel clocks
- Equalized inputs for operation with long HDMI cables (20 meters at 1080p)
- Fully buffered unidirectional inputs/outputs
- Globally-switchable 50Ω on-chip terminations
- Pre-emphasized outputs
- Low added jitter
- Single-supply operation (3.3V)
- Four auxiliary channels per link
- Bidirectional unbuffered I/Os
- Flexible supply operation (3.3V to 5V)
- HDCP standard compatible
- Allows switching of DDC bus and two other signals

#### Multiple channel bundling modes

- 1x(4:1) DVI/HDMI link switch (default)
- 2x(8:1) TMDS channel switch
- 1x(16:1) TMDS channel switch

#### Output disable feature

- Reduced power dissipation
- Allows building of larger arrays

#### Two AD8191 support DVI/HDMI dual-link

- Standards compatible: DVI, HDMI, HDCP
- Serial (I<sup>2</sup>C slave) and parallel control interface
- 100-pin 14mm x 14mm LQFP Pb-free package

### APPLICATIONS

#### Multi-input displays and projectors

#### A/V receivers

#### Set-top boxes

#### Advanced television (HDTV)

### GENERAL DESCRIPTION

The AD8191 is a DVI/HDMI switch featuring equalized TMDS inputs and pre-emphasized TMDS outputs, ideal for systems with long cable runs. Outputs can be set to a high impedance state to reduce the power dissipation and/or allow the construction of larger arrays using the wire-OR technique. Flexible channel bundling modes allow the AD8191 to be configured as a 4:1 single DVI/HDMI link switch, a dual 8:1 TMDS channel switch, or a single 16:1 TMDS channel switch.

#### Rev. PrJ

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### FUNCTIONAL BLOCK DIAGRAM

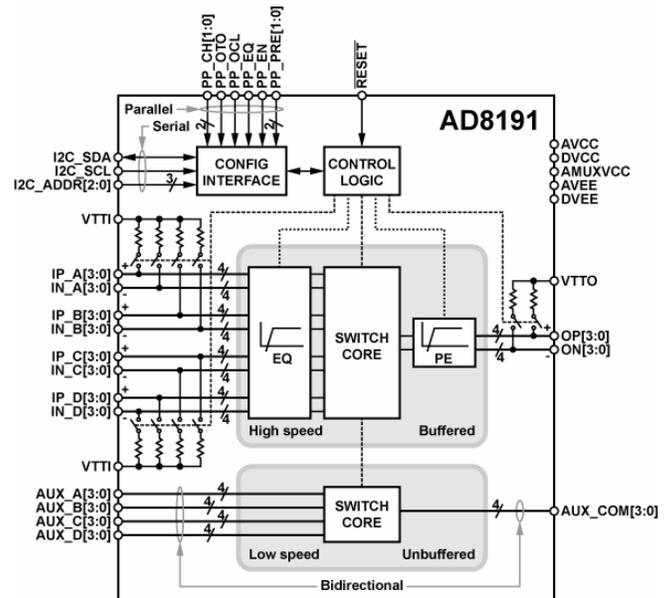


Figure 1. AD8191, 100-lead LQFP

### TYPICAL APPLICATION

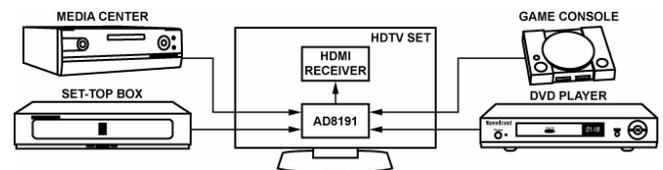


Figure 2. Typical AD8191 HDTV application

The AD8191 is provided in a 100-lead LQFP lead-free package specified to operate over the 0°C to 70°C temperature range.

### PRODUCT HIGHLIGHTS

1. Supports data rates up to 1.65Gbps, enabling UXGA (1600x1200) DVI resolutions and 1080p HDMI formats.
2. Input cable equalizer enables use of long cables at the input (more than 20 meters of 24 AWG cable at 1080p).
3. Auxiliary switch allows routing of DDC signals for a single-chip, fully HDMI 1.2a receive-compliant solution.

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## SPECIFICATIONS

$T_A = 27^\circ\text{C}$ ,  $AVCC = 3.3\text{ V}$ ,  $V_{TTI} = 3.3\text{ V}$ ,  $V_{TTO} = 3.3\text{ V}$ ,  $DVCC = 3.3\text{ V}$ ,  $AMUXVCC = 5\text{ V}$ ,  $AVEE = 0\text{ V}$ ,  $DVEE = 0\text{ V}$ , differential input swing = 1000 mV, TMDS outputs terminated with external  $50\ \Omega$  resistors to 3.3 V unless otherwise noted.

**Table 1.**

Parameter	Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
Maximum Data Rate (DR) per Channel	NRZ	1.65			Gbps
Bit Error Rate (BER)	PRBS $2^{23} - 1$			$10^{-9}$	
Added Deterministic Jitter	$DR \leq 1.65\text{ Gbps}$ , PRBS $2^{23} - 1$		40		ps (p-p)
Added Random Jitter			1		ps (rms)
Differential Intrapair Skew	At output		1		ps
Differential Interpair Skew <sup>1</sup>	At output		40		ps
<b>EQUALIZATION PERFORMANCE</b>					
Receiver (Highest Setting) <sup>2</sup>	Boost frequency = 825 MHz		12		dB
Transmitter (Highest Setting) <sup>3</sup>	Boost frequency = 825 MHz		6		dB
<b>INPUT CHARACTERISTICS</b>					
Input Voltage Swing	Differential	150		1200	mV
Input Common-Mode Voltage ( $V_{ICM}$ )		$AVCC - 800$		$AVCC$	mV
<b>OUTPUT CHARACTERISTICS</b>					
High Voltage Level	Single-ended high speed channel	$AVCC - 10$		$AVCC + 10$	mV
Low Voltage Level	Single-ended high speed channel	$AVCC - 600$		$AVCC - 400$	mV
Rise/Fall Time (20% to 80%)		75		242	ps
<b>INPUT TERMINATION</b>					
Resistance	Single-ended		50		$\Omega$
<b>AUXILIARY CHANNELS</b>					
On Resistance, $R_{AUX}$			100		$\Omega$
On Capacitance, $C_{AUX}$	DC bias = 2.5 V, ac voltage = 3.5 V, f = 100 kHz		8		pF
Input/Output Voltage Range		$DVEE$		$AMUXVCC$	V
<b>POWER SUPPLY</b>					
$AVCC$	Operating range	3	3.3	3.6	V
<b>QUIESCENT CURRENT</b>					
$AVCC$	Outputs disabled		40		mA
	Outputs enabled, no pre-emphasis		60		mA
	Outputs enabled, maximum pre-emphasis		108		mA
$V_{TTI}$	Input termination on <sup>4</sup>		40		mA
$V_{TTO}$	Output termination on, no pre-emphasis		40		mA
	Output termination on, maximum pre-emphasis		80		mA
$DVCC$			7		mA
$AMUXVCC$			0.01		mA
<b>POWER DISSIPATION</b>					
	Outputs disabled		271		mW
	Outputs enabled, no pre-emphasis		574		mW
	Outputs enabled, maximum pre-emphasis		936		mW
<b>TIMING CHARACTERISTICS</b>					
Switching/Update Delay				200	ms
	High speed switching register: HS_CH			1.5	$\mu\text{s}$
	All other configuration registers				ns
$\overline{\text{RESET}}$ Pulse Width		50			ns
<b>SERIAL CONTROL INTERFACE</b>					
Input High Voltage, $V_{IH}$		2			V
Input Low Voltage, $V_{IL}$				0.8	V

Parameter	Conditions/Comments	Min	Typ	Max	Unit
SERIAL CONTROL INTERFACE <sup>5</sup>					
Output High Voltage, $V_{OH}$		2.4			V
Output Low Voltage, $V_{OL}$				0.4	V

<sup>1</sup> Differential interpair skew is measured between the TMDS pairs of a single link.

<sup>2</sup> AD8191 output meets the transmitter eye diagram as defined in the DVI Standard Revision 1.0 and the HDMI Standard Revision 1.2a.

<sup>3</sup> Cable output meets the receiver eye diagram mask as defined in the DVI Standard Revision 1.0 and the HDMI Standard Revision 1.2a.

<sup>4</sup> Typical value assumes only the selected HDMI/DVI link is active with nominal signal swings and that the unselected HDMI/DVI link is deactivated. Minimum and maximum limits are measured at the respective extremes of input termination resistance and input voltage swing.

<sup>5</sup> The AD8191 is an I<sup>2</sup>C slave and its serial control interface is based on the 3.3 V I<sup>2</sup>C bus specification.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVCC to AVEE	3.7 V
DVCC to DVEE	3.7 V
DVEE to AVEE	±0.3 V
VTTI	AVCC + 0.6 V
VTTO	AVCC + 0.6 V
AMUXVCC	5.5 V
Internal Power Dissipation	TBD
High Speed Input Voltage	$AVCC - 1.4 V < V_{IN} < AVCC + 0.6 V$
High Speed Differential Input Voltage	2.0 V
Low-speed Input Voltage	$DVEE - 0.3 V < V_{IN} < AMUXVCC + 0.6 V$
I <sup>2</sup> C Logic Input Voltage	$DVEE - 0.3 V < V_{IN} < DVCC + 0.6 V$
Storage Temperature Range	-65°C to +125°C
Operating Temperature Range	0°C to +70°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions: a device soldered in a 4-layer JEDEC circuit board for surface-mount packages.  $\theta_{JC}$  is specified for the exposed pad soldered to the circuit board with no airflow.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
100-Lead LQFP	56	19	°C/W

### MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8191 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power rating as determined by the coefficients in Table 3.

**PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS**

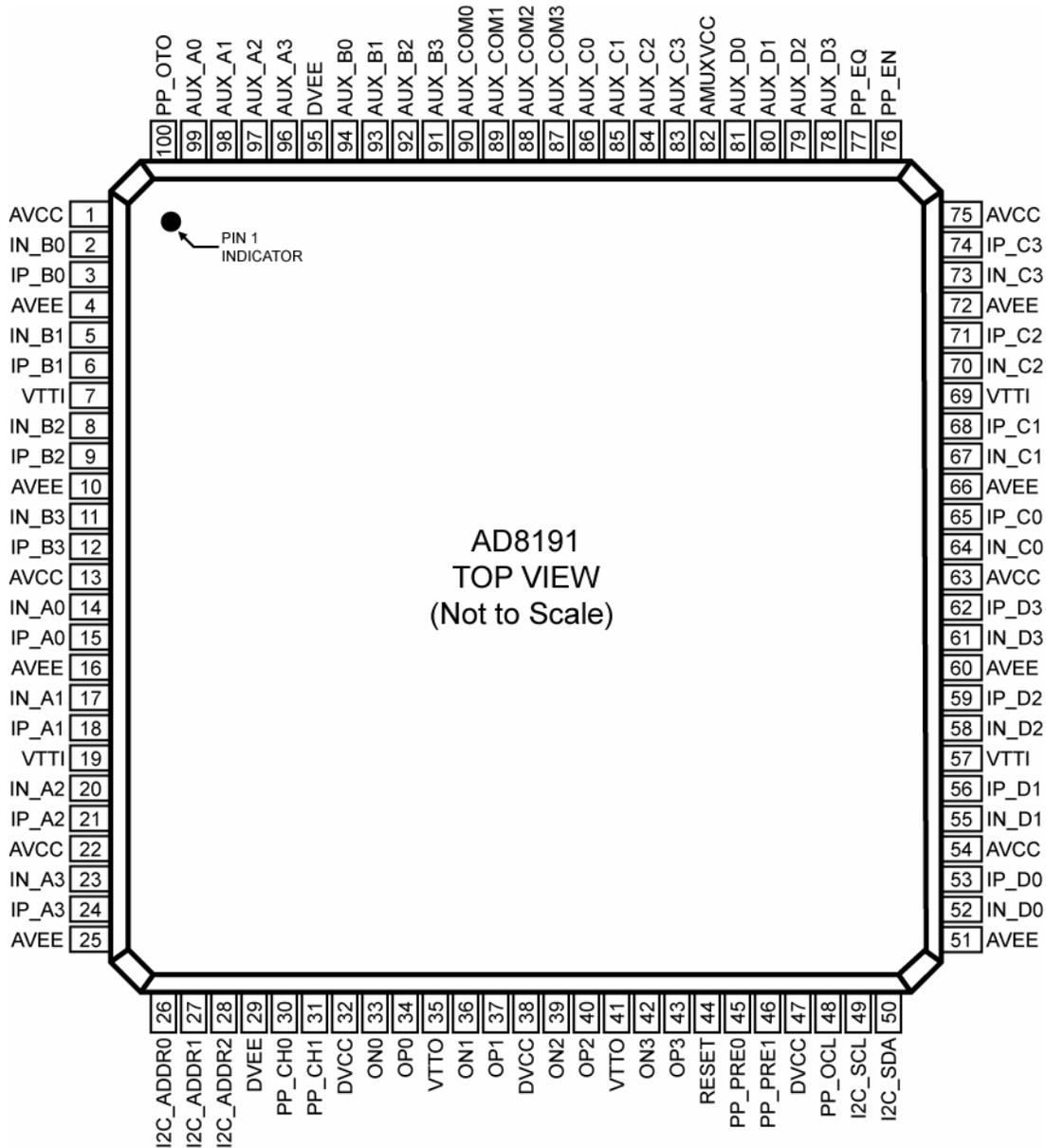


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 13, 22, 54, 63, 75	AVCC	Power	Positive Analog Supply (+3.3V Nominal).
2	IN_B0	HS <sup>1</sup> I	High Speed Input Complement.
3	IP_B0	HS I	High Speed Input.
4, 10, 16, 25, 51, 60, 66, 72	AVEE	Power	Negative Analog Supply (0V Nominal).
5	IN_B1	HS I	High Speed Input Complement.
6	IP_B1	HS I	High Speed Input.

<sup>1</sup> High-speed, TMDS.

7, 19, 57, 69	VTTI	Power	Input Termination Supply (Nominally Connected to AVCC).
8	IN_B2	HS I	High Speed Input Complement.
9	IP_B2	HS I	High Speed Input.
11	IN_B3	HS I	High Speed Input Complement.
12	IP_B3	HS I	High Speed Input.
14	IN_A0	HS I	High Speed Input Complement.
15	IP_A0	HS I	High Speed Input.
17	IN_A1	HS I	High Speed Input Complement.
18	IP_A1	HS I	High Speed Input.
20	IN_A2	HS I	High Speed Input Complement.
21	IP_A2	HS I	High Speed Input.
23	IN_A3	HS I	High Speed Input Complement.
24	IP_A3	HS I	High Speed Input.
26	I2C_ADDR0	Control	I <sup>2</sup> C Address 1 <sup>st</sup> LSB.
27	I2C_ADDR1	Control	I <sup>2</sup> C Address 2 <sup>nd</sup> LSB.
28	I2C_ADDR2	Control	I <sup>2</sup> C Address 3 <sup>rd</sup> LSB.
29, 95	DVEE	Power	Negative Digital and Auxiliary Multiplexer Power Supply (0V Nominal).
30	PP_CH0	Control	Quad Switching Mode High Speed Source Selection Parallel Interface LSB.
31	PP_CH1	Control	Quad Switching Mode High Speed Source Selection Parallel Interface MSB.
32, 38, 47	DVCC	Power	Positive Digital Power Supply (+3.3V Nominal).
33	ON0	HS O	High Speed Output Complement.
34	OP0	HS O	High Speed Output.
35, 41	V TTO	Power	Output Termination Supply (Nominally Connected to AVCC).
36	ON1	HS O	High Speed Output Complement.
37	OP1	HS O	High Speed Output.
39	ON2	HS O	High Speed Output Complement.
40	OP2	HS O	High Speed Output.
42	ON3	HS O	High Speed Output Complement.
43	OP3	HS O	High Speed Output.
44	$\overline{\text{RESET}}$	Control	Configuration Registers Reset (Normally pulled up to AVCC).
45	PP_PRE0	Control	High Speed Pre-emphasis Selection Parallel Interface LSB.
46	PP_PRE1	Control	High Speed Pre-emphasis Selection Parallel Interface MSB.
48	PP_OCL	Control	High Speed Output Current Level Parallel Interface.
49	I2C_SCL	Control	I <sup>2</sup> C Clock
50	I2C_SDA	Control	I <sup>2</sup> C Data
52	IN_D0	HS I	High Speed Input Complement.
53	IP_D0	HS I	High Speed Input.
55	IN_D1	HS I	High Speed Input Complement.
56	IP_D1	HS I	High Speed Input.
58	IN_D2	HS I	High Speed Input Complement.
59	IP_D2	HS I	High Speed Input.
61	IN_D3	HS I	High Speed Input Complement.
62	IP_D3	HS I	High Speed Input.
64	IN_C0	HS I	High Speed Input Complement.
65	IP_C0	HS I	High Speed Input.
67	IN_C1	HS I	High Speed Input Complement.
68	IP_C1	HS I	High Speed Input.

70	IN_C2	HS I	High Speed Input Complement.
71	IP_C2	HS I	High Speed Input.
73	IN_C3	HS I	High Speed Input Complement.
74	IP_C3	HS I	High Speed Input.
76	PP_EN	Control	High Speed Output Enable Parallel Interface.
77	PP_EQ	Control	High Speed Equalization Selection Parallel Interface.
78	AUX_D3	LS <sup>1</sup> I/O	Low Speed Input/Output.
79	AUX_D2	LS I/O	Low Speed Input/Output.
80	AUX_D1	LS I/O	Low Speed Input/Output.
81	AUX_D0	LS I/O	Low Speed Input/Output.
82	AMUXVCC	Power	Positive Auxiliary Multiplexer Supply (+5V Typical).
83	AUX_C3	LS I/O	Low Speed Input/Output.
84	AUX_C2	LS I/O	Low Speed Input/Output.
85	AUX_C1	LS I/O	Low Speed Input/Output.
86	AUX_C0	LS I/O	Low Speed Input/Output.
87	AUX_COM3	LS I/O	Low Speed Common Input/Output.
88	AUX_COM2	LS I/O	Low Speed Common Input/Output.
89	AUX_COM1	LS I/O	Low Speed Common Input/Output.
90	AUX_COM0	LS I/O	Low Speed Common Input/Output.
91	AUX_B3	LS I/O	Low Speed Input/Output.
92	AUX_B2	LS I/O	Low Speed Input/Output.
93	AUX_B1	LS I/O	Low Speed Input/Output.
94	AUX_B0	LS I/O	Low Speed Input/Output.
96	AUX_A3	LS I/O	Low Speed Input/Output.
97	AUX_A2	LS I/O	Low Speed Input/Output.
98	AUX_A1	LS I/O	Low Speed Input/Output.
99	AUX_A0	LS I/O	Low Speed Input/Output.
100	PP_OTO	Control	High Speed Output Termination Selection Parallel Interface.

<sup>1</sup> Low Speed, auxiliary.

## SERIAL INTERFACE CONFIGURATION REGISTERS

The serial interface configuration registers can be read and written using the I<sup>2</sup>C serial interface, pins I2C\_SDA and I2C\_SCL. The least significant bits of the AD8191 I<sup>2</sup>C part address can be set with the pins I2C\_ADDR2, I2C\_ADDR1 and I2C\_ADDR0.

**Table 5. Serial (I<sup>2</sup>C) Interface Register Map**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr.	Default
High-Speed Device Modes		High-speed switch enable HS_EN	High-speed switching mode select HS_SM[1]	HS_SM[0]	High-speed source select HS_CH[3]   HS_CH[2]   HS_CH[1]   HS_CH[0]				00h	40h
Auxiliary Device Modes		Auxiliary switch enable AUX_EN	Auxiliary switching mode select AUX_SM[1]	AUX_SM[0]	Auxiliary switch source select AUX_CH[3]   AUX_CH[2]   AUX_CH[1]   AUX_CH[0]				01h	40h
Receiver Settings								Input term. on/off select RX_TO	10h	01h
Input Term. Pulse 1	Sources A and B input termination pulse-on-source-switch select (disconnect termination for a short period of time) RX_PT[7]   RX_PT[6]   RX_PT[5]   RX_PT[4]   RX_PT[3]   RX_PT[2]   RX_PT[1]   RX_PT[0]								11h	00h
Input Term. Pulse 2	Sources C and D input termination pulse-on-source-switch select (disconnect termination for a short period of time) RX_PT[15]   RX_PT[14]   RX_PT[13]   RX_PT[12]   RX_PT[11]   RX_PT[10]   RX_PT[9]   RX_PT[8]								12h	00h
Receive Equalizer 1	Sources A and B input equalization level select RX_EQ[7]   RX_EQ[6]   RX_EQ[5]   RX_EQ[4]   RX_EQ[3]   RX_EQ[2]   RX_EQ[1]   RX_EQ[0]								13h	00h
Receive Equalizer 2	Sources C and D input equalization level select RX_EQ[15]   RX_EQ[14]   RX_EQ[13]   RX_EQ[12]   RX_EQ[11]   RX_EQ[10]   RX_EQ[9]   RX_EQ[8]								14h	00h
Transmitter Settings					Output pre-emphasis level select TX_PE[1]   TX_PE[0]		Output term. on/off select TX_PTO	Output current level select TX_OCL	20h	03h

### HIGH-SPEED DEVICE MODES REGISTER

HS\_EN: High-speed (TMDS) channels enable bit

**Table 6. HS\_EN Description**

HS_EN	Description
0b	High-speed channels off, low power/standby mode
1b	High-speed channels on

HS\_SM[1:0]: High-speed (TMDS) switching mode select bus

**Table 7. HS\_SM Description**

HS_SM[1:0]	Description
00b	Quad mode 4x(4:1)
01b	Dual mode 2x(8:1)
10b	Single mode 1x(16:1)
11b	Illegal value, previous HS_SM[1:0] kept

HS\_CH[3:0]: High-speed (TMDS) switch source select bus

**Table 8. Quad High-speed Switch Mode Mapping**

HS_CH[3:0]	O[3:0]	Description
xx00b	A[3:0]	High-speed source A switched to output
xx01b	B[3:0]	High-speed source B switched to output
xx10b	C[3:0]	High-speed source C switched to output
xx11b	D[3:0]	High-speed source D switched to output

**Table 9. Dual High-speed Switch Mode Mapping**

HS_CH[3:0]	O[3:2]	O[1:0]	Description
x000b	A1	A0	High-speed channels A0 and A1 switched to output
x001b	A3	A2	High-speed channels A2 and A3 switched to output
x010b	B1	B0	High-speed channels B0 and B1 switched to output
x011b	B3	B2	High-speed channels B2 and B3 switched to output
x100b	C1	C0	High-speed channels C0 and C1 switched to output
x101b	C3	C2	High-speed channels C2 and C3 switched to output
x110b	D1	D0	High-speed channels D0 and D1 switched to output
x111b	D3	D2	High-speed channels D2 and D3 switched to output

**Table 10. Single High-speed Switch Mode Mapping**

HS_CH[3:0]	O[3:0]	Description
0000b	A0	High-speed channel A0 switched to output
0001b	A1	High-speed channel A1 switched to output
0010b	A2	High-speed channel A2 switched to output
0011b	A3	High-speed channel A3 switched to output
0100b	B0	High-speed channel B0 switched to output
0101b	B1	High-speed channel B1 switched to output
0110b	B2	High-speed channels B2 switched to output
0111b	B3	High-speed channels B3 switched to output
1000b	C0	High-speed channels C0 switched to output
1001b	C1	High-speed channels C1 switched to output
1010b	C2	High-speed channels C2 switched to output
1011b	C3	High-speed channels C3 switched to output
1100b	D0	High-speed channels D0 switched to output
1101b	D1	High-speed channels D1 switched to output
1110b	D2	High-speed channels D2 switched to output
1111b	D3	High-speed channels D3 switched to output

**AUXILIARY DEVICE MODES REGISTER**

AUX\_EN: Auxiliary (low-speed) switch enable bit

**Table 11. AUX\_EN Description**

AUX_EN	Description
0b	Auxiliary switch off, no low speed input/output to low speed common input/output connection
1b	Auxiliary switch on

AUX\_SM[1:0]: Auxiliary (low-speed) switching mode select bus

**Table 12. AUX\_SM[1:0] Description**

AUX_SM[1:0]	Description
00b	Quad mode 4x(4:1)
01b	Dual mode 2x(8:1)
10b	Single mode 1x(16:1)
11b	Illegal value, previous AUX_SM[1:0] kept

AUX\_CH[3:0]: Auxiliary (low-speed) switch source select bus

**Table 13. Quad Auxiliary Switch Mode Mapping**

AUX_CH[3:0]	AUX_COM[3:0]	Description
xx00b	AUX_A[3:0]	Auxiliary source A switched to output
xx01b	AUX_B[3:0]0	Auxiliary source B switched to output
xx10b	AUX_C[3:0]	Auxiliary source C switched to output
xx11b	AUX_D[3:0]	Auxiliary source D switched to output

**Table 14. Dual Auxiliary Switch Mode Mapping**

AUX_CH[3:0]	AUX_COM[3:2]	AUX_COM[1:0]	Description
x000b	AUX_C0	AUX_A0	High-speed channels A0 and A1 switched to output
x001b	AUX_C1	AUX_A1	High-speed channels A2 and A3 switched to output
x010b	AUX_C2	AUX_A2	High-speed channels B0 and B1 switched to output
x011b	AUX_C3	AUX_A3	High-speed channels B2 and B3 switched to output
x100b	AUX_D0	AUX_B0	High-speed channels C0 and C1 switched to output
x101b	AUX_D1	AUX_B1	High-speed channels C2 and C3 switched to output
x110b	AUX_D2	AUX_B2	High-speed channels D0 and D1 switched to output
x111b	AUX_D3	AUX_B3	High-speed channels D2 and D3 switched to output

**Table 15. Single Auxiliary Switch Mode Mapping**

AUX_CH[3:0]	AUX_COM[3:0]	Description
0000b	AUX_A0	Auxiliary channel A0 switched to output
0001b	AUX_A1	Auxiliary channel A1 switched to output
0010b	AUX_A2	Auxiliary channel A2 switched to output
0011b	AUX_A3	Auxiliary channel A3 switched to output
0100b	AUX_B0	Auxiliary channel B0 switched to output
0101b	AUX_B1	Auxiliary channel B1 switched to output
0110b	AUX_B2	Auxiliary channels B2 switched to output
0111b	AUX_B3	Auxiliary channels B3 switched to output
1000b	AUX_C0	Auxiliary channels C0 switched to output
1001b	AUX_C1	Auxiliary channels C1 switched to output
1010b	AUX_C2	Auxiliary channels C2 switched to output
1011b	AUX_C3	Auxiliary channels C3 switched to output
1100b	AUX_D0	Auxiliary channels D0 switched to output
1101b	AUX_D1	Auxiliary channels D1 switched to output
1110b	AUX_D2	Auxiliary channels D2 switched to output
1111b	AUX_D3	Auxiliary channels D3 switched to output

**RECEIVER SETTINGS REGISTER**

RX\_TO: High-speed (TMDS) channels input termination on/off select bit

**Table 16. RX\_TO Description**

RX_TO	Description
0b	Input termination off
1b	Input termination on (can be pulsed on and off according to settings in the Input Termination Pulse Register)

**INPUT TERMINATION PULSE REGISTERS 1 AND 2**

RX\_PT[X]: High-speed (TMDS) input channel “X” pulse-on-source switch select bit

**Table 17. RX\_PT[X] Description**

RX_PT[X]	Description
0b	Input termination for TMDS channel “X” always connected when source is switched
1b	Input termination for TMDS channel “X” disconnected for 100msec when source switched

**Table 18. RX\_PT[X] Mapping**

RX_PT[X]	Corresponding Input TMDS Channel
Bit 0	B0
Bit 1	B1
Bit 2	B2
Bit 3	B3
Bit 4	A0
Bit 5	A1
Bit 6	A2
Bit 7	A3
Bit 8	C3
Bit 9	C2
Bit 10	C1
Bit 11	C0
Bit 12	D3
Bit 13	D2
Bit 14	D1
Bit 15	D0

**RECEIVE EQUALIZER REGISTERS 1 AND 2**

RX\_EQ[X]: High-speed (TMDS) input “X” equalization level select bit

**Table 19. RX\_EQ[X] Description**

RX_EQ[X]	Description
0b	Low equalization (6dB)
1b	High equalization (12dB)

**Table 20. RX\_EQ[X] Mapping**

RX_EQ[X]	Corresponding Input TMDS Channel
Bit 0	B0
Bit 1	B1
Bit 2	B2
Bit 3	B3
Bit 4	A0
Bit 5	A1
Bit 6	A2
Bit 7	A3
Bit 8	C3
Bit 9	C2
Bit 10	C1
Bit 11	C0
Bit 12	D3
Bit 13	D2
Bit 14	D1

**TRANSMITTER SETTINGS REGISTER**

TX\_PE[1:0]: High-speed (TMDS) output pre-emphasis level select bus (for all TMDS channels)

**Table 21. TX\_PE[1:0] Description**

<b>TX_PE[1:0]</b>	<b>Description</b>
00b	No pre-emphasis (0dB)
01b	Low pre-emphasis (2dB)
10b	Medium pre-emphasis (4dB)
11b	High pre-emphasis (6dB)

TX\_PTO: High-speed (TMDS) output termination on/off select bit (for all channels)

**Table 22. TX\_PTO Description**

<b>TX_PTO</b>	<b>Description</b>
0b	Output termination off
1b	Output termination on

TX\_OCL: High-speed (TMDS) output current level select bit (for all channels)

**Table 23. TX\_OCL Description**

<b>TX_OCL</b>	<b>Description</b>
0b	Output current set to 10mA
1b	Output current set to 20mA

## PARALLEL INTERFACE CONFIGURATION REGISTERS

The parallel interface configuration registers can be directly written using the pins PP\_EN, PP\_CH[1:0], PP\_EQ, PP\_PRE[1:0], PP\_OTO and PP\_OCL.

**Table 24. Parallel Interface Register Map**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High-speed Device Modes		High-speed switch enable PP_EN	High-speed switching mode select (Quad) 0	0	High-speed source select 0   0   PP_CH[1]   PP_CH[0]			
Auxiliary Device Modes		Auxiliary switch enable 1	Auxiliary switching mode select (Quad) 0	0	Auxiliary switch source select 0   0   PP_CH[1]   PP_CH[0]			
Receiver Settings								Input term. on/off select (term. always on) 1
Input Term. Pulse 1	0	0	0	0	0	0	0	0
Input Term. Pulse 2	0	0	0	0	0	0	0	0
Receive Equalizer 1	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ
Receive Equalizer 2	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ
Transmitter Settings					PP_PE[1]	PP_PE[0]	PP_OTO	Output current level select PP_OCL

PP\_CH[1:0]: Auxiliary switch source select bus

### HIGH-SPEED DEVICE MODES REGISTER

The high-speed (TMDS) switching mode is fixed to Quad mode when using the parallel interface.

PP\_EN: High-speed (TMDS) channels enable bit

**Table 25. PP\_EN Description**

PP_EN	Description
0b	High-speed channels off, low power/standby mode
1b	High-speed channels on

PP\_CH[1:0]: High-speed (TMDS) switch source select bus

**Table 26. Quad High-speed Switch Mode Mapping**

PP_CH[1:0]	O[3:0]	Description
00b	A[3:0]	High-speed source A switched to output
01b	B[3:0]	High-speed source B switched to output
10b	C[3:0]	High-speed source C switched to output
11b	D[3:0]	High-speed source D switched to output

### AUXILIARY DEVICE MODES REGISTER

The auxiliary (low-speed) switch is always enabled and the auxiliary switching mode is fixed to Quad mode when using the parallel interface.

**Table 27. Quad Auxiliary Switch Mode Mapping**

PP_CH[1:0]	AUX_COM[3:0]	Description
00b	AUX_A[3:0]	Auxiliary source A switched to output
01b	AUX_B[3:0]	Auxiliary source B switched to output
10b	AUX_C[3:0]	Auxiliary source C switched to output
11b	AUX_D[3:0]	Auxiliary source D switched to output

### RECEIVER SETTINGS REGISTER

High-speed (TMDS) channels input termination is fixed to on when using the parallel interface.

### INPUT TERMINATION PULSE REGISTERS 1 AND 2

High-speed input (TMDS) channels pulse-on-source switching fixed to off when using the parallel interface.

### RECEIVE EQUALIZER REGISTERS 1 AND 2

PP\_EQ: High-speed (TMDS) inputs equalization level select bit. The input equalization cannot be set individually (per channel) when using the parallel interface; one equalization setting affects all input channels.

Table 28. PP\_EQ Description

PP_EQ	Description
0b	Low equalization (6dB)
1b	High equalization (12dB)

**TRANSMITTER SETTINGS REGISTER**

PP\_PE[1:0]: High-speed (TMDS) output pre-emphasis level select bus (for all TMDS channels)

Table 29. PP\_PE[1:0] Description

PP_PE[1:0]	Description
00b	No pre-emphasis (0dB)
01b	Low pre-emphasis (2dB)
10b	Medium pre-emphasis (4dB)
11b	High pre-emphasis (6dB)

PP\_OTO: High-speed (TMDS) output termination on/off select bit (for all channels)

Table 30. PP\_OTO Description

PP_OTO	Description
0b	Output termination off
1b	Output termination on

PP\_OCL: High-speed (TMDS) output current level select bit (for all channels)

Table 31. TX\_OCL Description

PP_OCL	Description
0b	Output current set to 10mA
1b	Output current set to 20mA

### TYPICAL PERFORMANCE CHARACTERISTICS

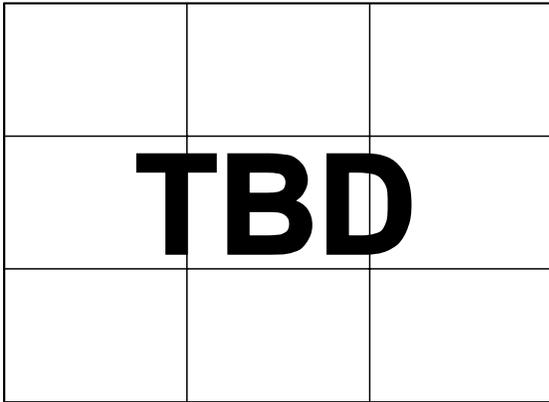


Figure 4.

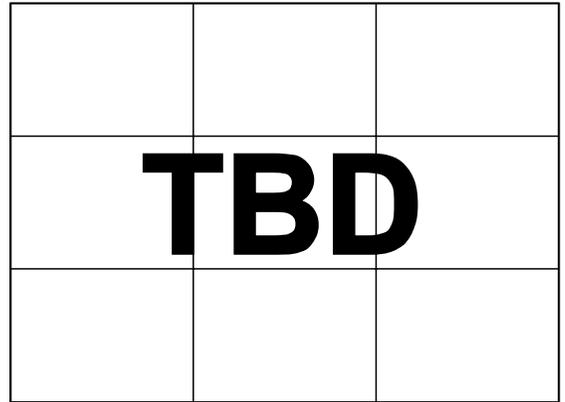


Figure 7.

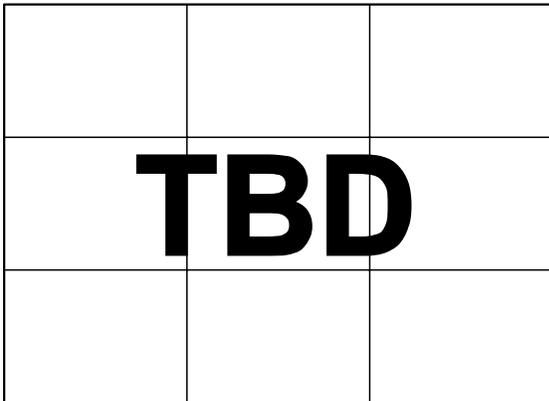


Figure 5.

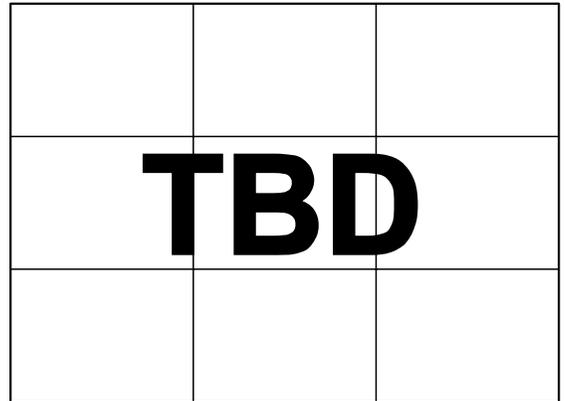


Figure 8.

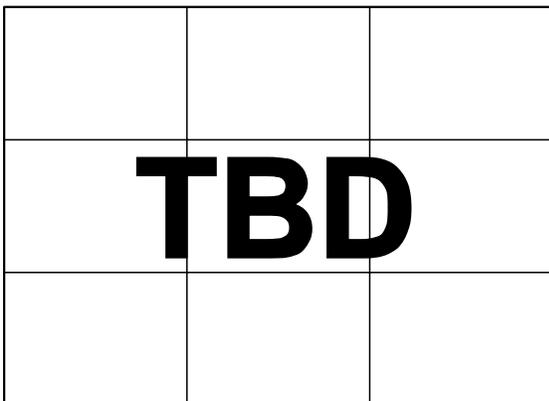


Figure 6.

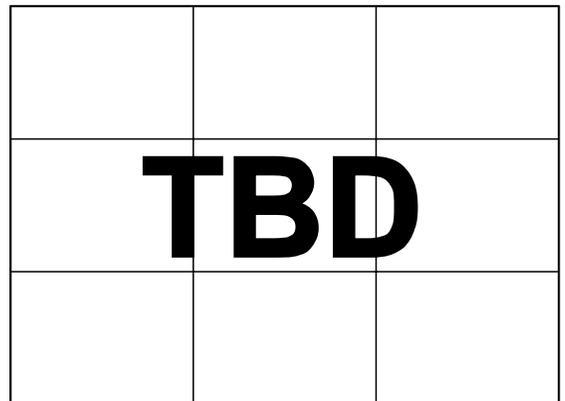


Figure 9.

## THEORY OF OPERATION

### INTRODUCTION

The primary function of the AD8191 is to switch one of four (HDMI or DVI) single-link sources to one output. Each HDMI/DVI link consists of four differential, high speed channels and four auxiliary single-ended, low speed control signals. The high speed channels include a data-word clock and three transition minimized differential signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 1.65 Gbps. The four low speed control signals are 5 V tolerant bidirectional lines that can carry configuration signals, HDCP encryption, and other information; depending upon the specific application.

All four high speed TMDS channels in a given link are identical; that is, the pixel clock can be run on any of the four TMDS channels.

Transmit and receive channel compensation is provided for the high speed channels where the user can (manually) select among a number of fixed settings.

The AD8191 switching logic has three modes: quad (one 4:1 DVI/HDMI link switch), dual (two 8:1 TMDS channel switch) and single (one 16:1 TMDS channel switch).

The AD8191 has dual parallel and I<sup>2</sup>C serial programming with 8 user-programmable I<sup>2</sup>C slave addresses. In all cases serial programming values override any prior parallel programming values.

### INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 10. The input terminations can be optionally disconnected for approximately 100 ms following a source switch. The user can program which of the 16 high speed input channels employs this feature by selectively setting the associated RX\_PT bits in the input termination pulse register. Additionally, all the input terminations can be disconnected by programming the RX\_TO bit in the receiver settings register.

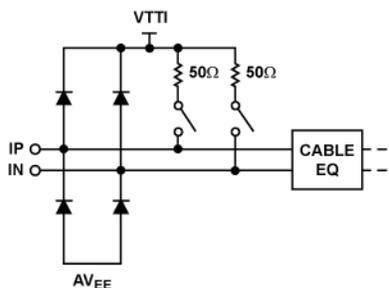


Figure 10. High-speed Input Simplified Schematic

The input equalizer can be manually configured to provide two different levels of high frequency boost: 6 dB or 12 dB. The user can individually program the equalization level of the eight high speed input channels by selectively setting the associated RX\_EQ bits in the receive equalizer register. No specific cable length is suggested for a particular equalization setting because cable performance varies widely between manufacturers; however, in general, the equalization of the AD8191 can be set to 12 dB without degrading the signal integrity, even for short input cables. At the 12 dB setting, the AD8191 can equalize over 20 meters of 24 AWG cable at 1.65 Gbps.

### OUTPUT CHANNELS

Each high-speed output differential pair is terminated to the +3.3V VTTO power supply through a 50Ω on-chip resistor (Figure 11). This termination is user-selectable; it can be turned on or off by programming the TX\_PTO bit of the Transmitter Settings Register.

The output termination resistors of the AD8191 back-terminate the output TMDS transmission lines. These back-terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8191 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

The AD8191 output has a disable feature that places the outputs in a tri-state mode. This mode is enabled by setting the HS\_EN bit of the high speed device modes register. Larger wire-ORed arrays can be constructed using the AD8191 in this mode.

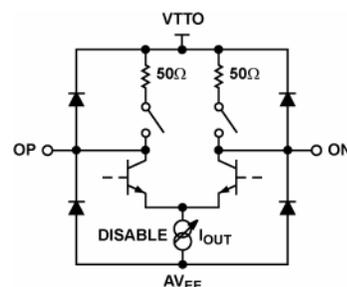


Figure 11. High-speed Output Simplified Schematic

The AD8191 requires output termination resistors when the high speed outputs are enabled. Termination can be internal and/or external. The internal terminations of the AD8191 are enabled by setting the TX\_PTO bit of the transmitter settings register (the default upon reset). External terminations can be provided either by on-board resistors or by the input termination resistors of an HDMI/DVI receiver. If both internal and external terminations are provided, set the output current level to 20 mA by programming the TX\_OCL bit of the transmitter settings register (the default upon reset). If only

external terminations are provided, set the output current level to 10 mA. The high speed outputs must be disabled if there are no output termination resistors present in the system.

The output pre-emphasis can be manually configured to provide one of four different levels of high frequency boost. The specific boost level is selected by programming the TX\_PE bits of the transmitter settings register. No specific cable length is suggested for a particular pre-emphasis setting because cable performance varies widely between manufacturers.

**AD8191 HIGH SPEED SWITCHING MODES**

The AD8191 has three high speed switching modes that can be selected by programming the HS\_SM bits of the high speed modes register.

Single Switching Mode

In this mode the AD8191 behaves as a single 16:1 TMDS channel multiplexer; a single channel, out of a possible 16, is routed to all of the outputs. The input channel that is routed to the outputs can be selected by programming the HS\_CH bits in the high speed modes register.

Dual Switching Mode

In this mode the AD8191 behaves as two locked 8:1 TMDS channel switches. These two locked switches share the channel select input and therefore switch together. The user can select which of the two 8-input groups are routed to outputs by programming the HD\_CH bits of the high speed modes register.

Quad Switching Mode

This is the default mode. In Quad mode the AD8191 behaves like a 4:1 DVI/HDMI link multiplexer, routing groups of 4 input channels to the 4-channel output. The user can select which link is routed to the output by programming the HS\_CH bits of the High Speed Modes Register.

**AUXILIARY SWITCH**

The auxiliary (low speed) lines have no amplification. They are routed using a passive switch that is bandwidth compatible with standard speed I<sup>2</sup>C. The schematic equivalent for this passive connection is shown in Figure 12.

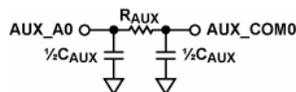


Figure 12. Auxiliary Channel Simplified Schematic. AUX\_A0 to AUX\_COM0 Routing Example Shown.

When turning off the AD8191, care needs to be taken with the AMUXVCC supply to ensure that the auxiliary multiplexer pins are in a high impedance state. A scenario that illustrates this requirement is one where the auxiliary multiplexer is used to switch the display data channel (DDC) bus. In some applica-

tions, additional devices can be connected to the DDC bus (such as an EEPROM with EDID information) upstream of the AD8191. Extended display identification data (EDID) is a VESA standard-defined data format for conveying display configuration information to sources to optimize display use. EDID devices may need to be available via the DDC bus, regardless of the state of the AD8191 and any downstream circuit. For this configuration, the auxiliary inputs of the powered down AD8191 need to be in a high impedance state to avoid pulling down on the DDC lines and preventing these other devices from using the bus.

When the AD8191 is powered from a simple resistor network, as shown in Figure 13, it uses the 5 V supply that is required from any HDMI/DVI source to guarantee high impedance of the auxiliary multiplexer pins. The AMUXVCC supply does not draw any static current; therefore, it is recommended that the resistor network tap the 5 V supplies as close to the connectors as possible to avoid any additional voltage drop.

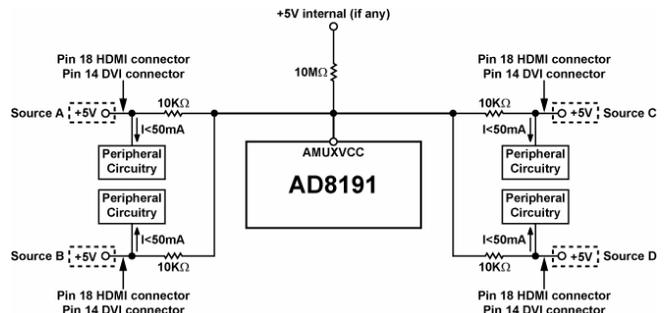


Figure 13: Suggested AMUXVCC Power Scheme.

This precaution does not need to be taken if the DDC peripheral circuitry is connected to the bus downstream of the AD8191.

## SERIAL CONTROL INTERFACE

### RESET

On initial power-up, or at any point in operation, the AD8191 register set can be restored to pre-programmed default values by pulling the RESET pin to low according to the specification in Table 1. During normal operation, however, the RESET pin must be pulled up to 3.3 V. The pre-programmed default values correspond to the state indicated by the parallel control interface pins. Once the AD8191 is reset, the part can be controlled through the parallel control interface until the first serial control event occurs.

### WRITE PROCEDURE

To write data to the AD8191 register set, an I<sup>2</sup>C master (such as a microcontroller) needs to send the appropriate control signals to the AD8191 slave device. The signals are controlled by the I<sup>2</sup>C master unless otherwise specified. For a diagram of the procedure, see Figure 14. The steps for a write procedure are as follows:

1. Send a start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low).
2. Send the AD8191 part address (seven bits). The upper four bits of the AD8191 part address are the static value [1001] and the 3-LSBs are set by the Input Pins I2C\_ADDR2, I2C\_ADDR1 and I2C\_ADDR0 (LSB). This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8191 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8191 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the AD8191 to acknowledge the request.
9. Do one of the following:
  - 9a. Send a stop condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line high) and release control of the bus to end the transaction (shown in Figure 14).
  - 9b. Send a repeated start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low) and continue with Step 2 in this procedure to perform another write.
  - 9c. Send a repeated start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low) and continue with Step 2 of the read procedure (in the Read Procedure section) to perform a read from another address.
  - 9d. Send a repeated start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low) and continue with Step 8 of the read procedure (in the Read Procedure section) to perform a read from the same address set in Step 5.

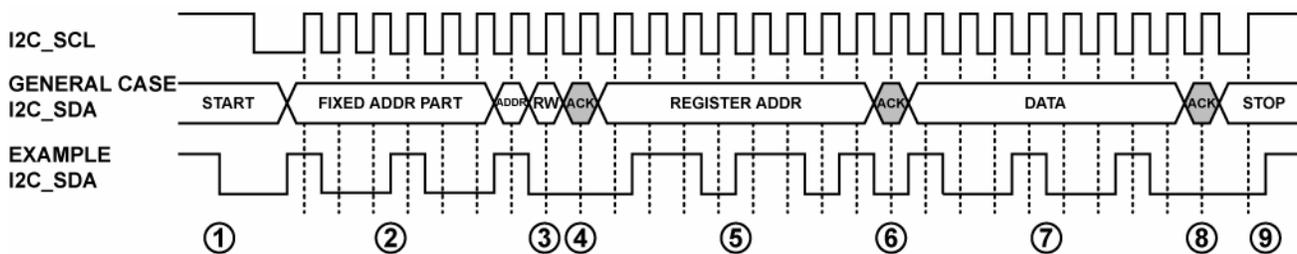


Figure 14. I<sup>2</sup>C Write Diagram

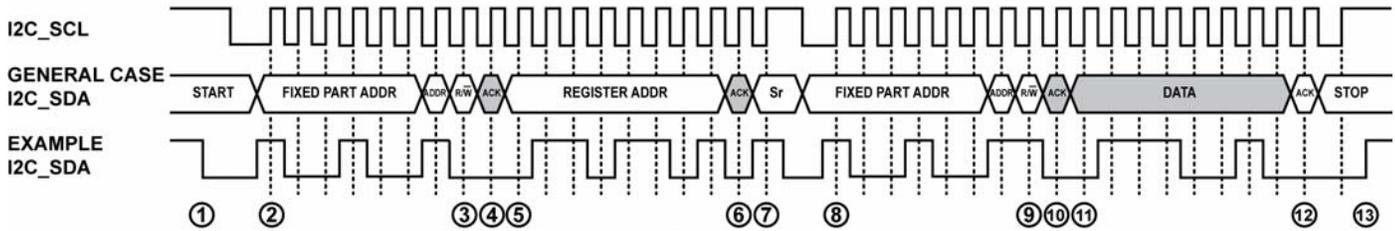


Figure 15. I<sup>2</sup>C Read Diagram

**READ PROCEDURE**

To read data from the AD8191 register set, an I<sup>2</sup>C master (such as a microcontroller) needs to send the appropriate control signals to the AD8191 slave device. The signals are controlled by the I<sup>2</sup>C master unless otherwise specified. For a diagram of the procedure, see Figure 16. The steps for a read procedure are as follows:

1. Send a start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low).
2. Send the AD8191 part address (seven bits). The upper four bits of the AD8191 part address are the static value [1001] and the 3-LSBs are set by the Input Pins I2C\_ADDR2, I2C\_ADDR1 and I2C\_ADDR0 (LSB). This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8191 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first.
6. Wait for the AD8191 to acknowledge the request.
7. Send a repeated start condition (Sr) by holding the I2C\_SCL line high and pulling the I2C\_SDA line low.
8. Resend the AD8191 part address (seven bits) from Step 2. The upper four bits of the AD8191 part address are the static value [1001] and the 3-LSBs are set by the Input Pins I2C\_ADDR2, I2C\_ADDR1 and I2C\_ADDR0 (LSB). This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8191 to acknowledge the request.
11. The AD8191 serially transfers the data (eight bits) held in the register indicated by the address set in Step 5. This data is sent MSB first.
12. Acknowledge the data from the AD8191.
13. Do one of the following:
  - a. Send a stop condition (while holding the I2C\_SCL line high, pull the SDA line high) and release control of the bus to end the transaction (shown in Figure 15).
  - b. Send a repeated start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low) and continue with Step 2 of the write procedure (previous Write Procedure section) to perform a write.
  - c. Send a repeated start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
  - d. Send a repeated start condition (while holding the I2C\_SCL line high, pull the I2C\_SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

## **PARALLEL CONTROL INTERFACE**

The AD8191 can be controlled through the parallel interface using the pins PP\_EN, PP\_CH[1:0], PP\_EQ, PP\_PRE[1:0], PP\_OTO and PP\_OCL. Setting these pins will update the parallel control interface registers, as described in Table 24. If the AD8191 is accessed via the serial control interface, then the parallel control interface is disabled until the part is reset.

## PCB LAYOUT GUIDELINES

The AD8191 is used to switch two distinctly different types of signals, both of which are required for HDMI and DVI video. These signal groups require different treatment when laying out a PC board.

The first group of signals carries the audiovisual data. HDMI/DVI video signals are differential, unidirectional, and high speed (up to 1.65 Gbps). The channels that carry the video data must be controlled impedance, terminated at the receiver, and capable of operating up to at least 1.65 Gbps. It is especially important to note that the differential traces that carry the TMDS signals should be designed with a controlled differential impedance of 100  $\Omega$ . The AD8191 provides single-ended 50  $\Omega$  terminations on-chip for both its inputs and outputs, and both the input and output terminations can be enabled or disabled through the serial interface. Transmitter termination is not fully specified by the HDMI standard but its inclusion improves the overall system signal integrity.

The audiovisual (AV) data carried on these high speed channels is encoded by a technique called transmission minimized differential signaling (TMDS) and in the case of HDMI, is also encrypted according to the high bandwidth digital copy protection (HDCP) standard.

The second group of signals consists of low speed auxiliary control signals used for communication between a source and a sink. Depending upon the application, these signals can include the DDC bus (this is an I<sup>2</sup>C bus used to send EDID information and HDCP encryption keys between the source and the sink), the consumer electronics control (CEC) line, and the hot plug detect (HPD) line. These auxiliary signals are bidirectional, low speed, and transferred over a single-ended transmission line that does not need to have controlled impedance. The primary concern with laying out the auxiliary lines is ensuring that they conform to the I<sup>2</sup>C bus standard and do not have excessive capacitive loading.

### TMDS SIGNALS

In the HDMI/DVI standard, four differential pairs carry the TMDS signals. In DVI, three of these pairs are dedicated to carrying RGB video and sync data. For HDMI, audio data is also interleaved with the video data; the DVI standard does not incorporate audio information. The fourth high speed differential pair is used for the AV data-word clock, and runs at one-tenth the speed of the TMDS data channels.

The four high speed channels of the AD8191 are identical. No concession was made to lower the bandwidth of the fourth channel for the pixel clock, so any channel can be used for any TMDS signal. The user chooses which signal is routed over which channel. Additionally, the TMDS channels are symmetrical; therefore, the p and n of a given differential pair are interchangeable, provided the inversion is consistent across all inputs

and outputs of the AD8191. However, the routing between inputs and outputs through the AD8191 is fixed. For example, Output Channel 0 always switches between Input A0 and Input B0, and so forth.

The AD8191 buffers the TMDS signals and the input traces can be considered electrically independent of the output traces. In most applications, the quality of the signal on the input TMDS traces are more sensitive to the PCB layout. Regardless of the data being carried on a specific TMDS channel, or whether the TMDS line is at the input or the output of the AD8191, all four high speed signals should be routed on a PCB in accordance with the same RF layout guidelines.

### LAYOUT FOR THE TMDS SIGNALS

The TMDS differential pairs can either be microstrip traces, routed on the outer layer of a board, or stripline traces, routed on an internal layer of the board. If microstrip traces are used, there should be a continuous reference plane on the PCB layer directly below the traces. If stripline traces are used, they must be sandwiched between two continuous reference planes in the PCB stack-up. Additionally, the p and n of each differential pair must have a controlled differential impedance of 100  $\Omega$ . The characteristic impedance of a differential pair is a function of several variables including the trace width, the distance separating the two traces, the spacing between the traces and the reference plane, and the dielectric constant of the PC board binder material. Interlayer vias introduce impedance discontinuities that can cause reflections and jitter on the signal path, therefore, it is preferable to route the TMDS lines exclusively on one layer of the board, particularly for the input traces. Additionally, to prevent unwanted signal coupling and interference, route the TMDS signals away from other signals and noise sources on the PCB.

Both traces of a given differential pair must be equal in length to minimize intrapair skew. Maintaining the physical symmetry of a differential pair is integral to ensuring its signal integrity; excessive intrapair skew can introduce jitter through duty cycle distortion (DCD). The p and n of a given differential pair should always be routed together in order to establish the required 100  $\Omega$  differential impedance. Enough space should be left between the differential pairs of a given group so that the n of one pair does not couple to the p of another pair. For example, one technique is to make the interpair distance 4 to 10 times wider than the intrapair spacing.

Any group of four TMDS channels (Input A, Input B, or the output) should have closely matched trace lengths in order to minimize interpair skew. Severe interpair skew can cause the data on the four different channels of a group to arrive out of alignment with one another. A good practice is to match the trace lengths for a given group of four channels to within 0.05 inches on FR4 material.

The length of the TMDS traces should be minimized to reduce overall signal degradation. Commonly used PC board material such as FR4 is lossy at high frequencies, so long traces on the circuit board increase signal attenuation, resulting in decreased signal swing and increased jitter through inter-symbol interference (ISI).

### CONTROLLING THE CHARACTERISTIC IMPEDANCE OF A TMDS DIFFERENTIAL PAIR

The characteristic impedance of a differential pair depends on a number of variables including the trace width, the distance between the two traces, the height of the dielectric material between the trace and the reference plane below it, and the dielectric constant of the PCB binder material. To a lesser extent, the characteristic impedance also depends upon the trace thickness and the presence of solder mask. There are many combinations that can produce the correct characteristic impedance. It is generally required to work with the PC board fabricator to obtain a set of parameters to produce the desired results.

One consideration is how to guarantee a differential pair with a differential impedance of  $100\ \Omega$  over the entire length of the trace. One technique to accomplish this is to change the width of the traces in a differential pair based on how closely one trace is coupled to the other. When the two traces of a differential pair are close and strongly coupled, they should have a width that produces a  $100\ \Omega$  differential impedance. When the traces split apart to go into a connector, for example, and are no longer so strongly coupled, the width of the traces should be increased to yield a differential impedance of  $100\ \Omega$  in the new configuration.

### TMDS TERMINATIONS

The AD8191 provides internal  $50\ \Omega$  single-ended terminations for all of its high speed inputs and outputs. It is not necessary to include external termination resistors for the TMDS differential pairs on the PCB.

The output termination resistors of the AD8191 back-terminate the output TMDS transmission lines. These back-terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8191 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

### AUXILIARY CONTROL SIGNALS

There are four single-ended control signals associated with each source or sink in an HDMI/DVI application. These are hot plug detect (HPD), consumer electronics control (CEC), and two display data channel (DDC) lines. The two signals on the DDC bus are SDA and SCL (serial data and serial clock, respectively). These four signals can be switched through the auxiliary bus of

the AD8191 and do not need to be routed with the same strict considerations as the high speed TMDS signals.

In general, it is sufficient to route each auxiliary signal as a single-ended trace. These signals are not sensitive to impedance discontinuities, do not require a reference plane, and can be routed on multiple layers of the PCB. However, it is best to follow strict layout practices whenever possible to prevent the PCB design from affecting the overall application. The specific routing of the HPD, CEC, and DDC lines depends upon the application in which the AD8191 is being used.

For example, the maximum speed of signals present on the auxiliary lines are  $100\ \text{kHz}$  I<sup>2</sup>C data on the DDC lines, therefore, any layout that enables  $100\ \text{kHz}$  I<sup>2</sup>C to be passed over the DDC bus should suffice. The HDMI 1.2a specification, however, places a strict  $50\ \text{pF}$  limit on the amount of capacitance that can be measured on either SDA or SCL at the HDMI input connector. This  $50\ \text{pF}$  limit includes the HDMI connector, the PCB, and whatever capacitance is seen at the input of the AD8191, or an equivalent receiver. There is a similar limit of  $100\ \text{pF}$  of input capacitance for the CEC line.

The parasitic capacitance of traces on a PCB increases with trace length. To help ensure that a design satisfies the HDMI specification, the length of the CEC and DDC lines on the PCB should be made as short as possible. Additionally, if there is a reference plane in the layer adjacent to the auxiliary traces in the PCB stack-up, relieving or clearing out this reference plane immediately under the auxiliary traces significantly decreases the amount of parasitic trace capacitance. An example of the board stackup is shown in Figure 16.

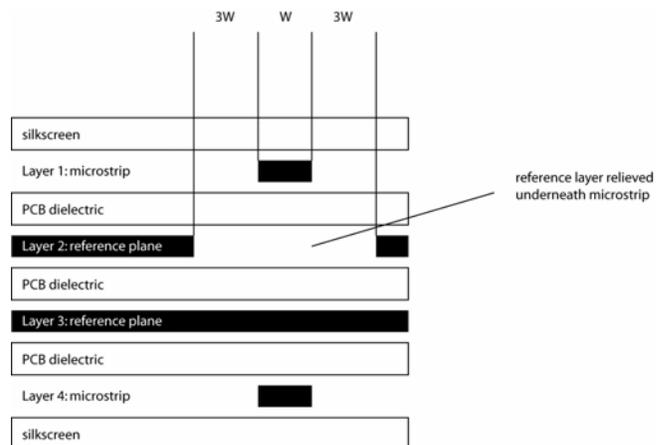


Figure 16. Example Board Stackup

HPD is a dc signal presented by a sink to a source to indicate that the source EDID is available for reading. The placement of this signal is not critical, but it should be routed as directly as possible.

When the AD8191 is powered up, one set of the auxiliary inputs is passively routed to the outputs. In this state, the AD8191 looks like a  $100\ \Omega$  resistor between the selected auxiliary inputs

and the corresponding outputs as illustrated in Figure 12. The AD8191 does not buffer the auxiliary signals, therefore, the input traces, output traces, and the connection through the AD8191 all must be considered when designing a PCB to meet HDMI/DVI specifications. The unselected auxiliary inputs of the AD8191 are placed into a high impedance mode when the device is powered up. To ensure that all of the auxiliary inputs of the AD8191 are in a high impedance mode when the device is powered off, it is necessary to power the AMUXVCC supply as illustrated in Figure 13.

In contrast to the auxiliary signals, the AD8191 buffers the TMDS signals, allowing a PCB designer to layout the TMDS inputs independently of the outputs.

### POWER SUPPLIES

The AD8191 has five separate power supplies referenced to two separate grounds. The supply/ground pairs are: AVCC/AVEE, VTTI/AVEE, VTTO/AVEE, DVCC/DVEE, and AMUXVCC/DVEE.

The AVCC/AVEE (3.3 V) and DVCC/DVEE (3.3 V) supplies power the core of the AD8191. The VTTI/AVEE supply (3.3 V) powers the input termination (see Figure 10). Similarly, the VTTO/AVEE supply (3.3 V) powers the output termination (see Figure 11). The AMUXVCC/DVEE supply (3.3 V to 5 V) powers the auxiliary multiplexer core and determines the maximum allowed voltage on the auxiliary lines. For example,

if the DDC bus is using 5 V I<sup>2</sup>C, then AMUXVCC should be connected to +5 V relative to DVEE.

In a typical application, all pins labeled AVEE or DVEE should be connected directly to ground. All pins labeled AVCC, DVCC, VTTI, or VTTO should be connected to 3.3 V, and Pin AMUXVCC tied to 5 V. The supplies can also be powered individually, but care must be taken to ensure that each stage of the AD8191 is powered correctly.

### POWER SUPPLY BYPASSING

The AD8191 requires minimal supply bypassing. When powering the supplies individually, place a 0.01  $\mu$ F capacitor between each 3.3 V supply pin (AVCC, DVCC, VTTI, and VTTO) and ground to filter out supply noise. Generally, bypass capacitors should be placed near the power pins and should connect directly to the relevant supplies (without long intervening traces). For example, to improve the parasitic inductance of the power supply decoupling capacitors, minimize the trace length between capacitor landing pads and the vias.

In applications where the AD8191 is powered by a single 3.3 V supply, it is recommended to use two reference supply planes and bypass the 3.3 V reference plane to the ground reference plane with one 220 pF, one 1000 pF, two 0.01  $\mu$ F, and one 4.7  $\mu$ F capacitors. The capacitors should via down directly to the supply planes and be placed within a few centimeters of the AD8191. The AMUXVCC supply does not require additional bypassing.

## APPLICATION NOTES

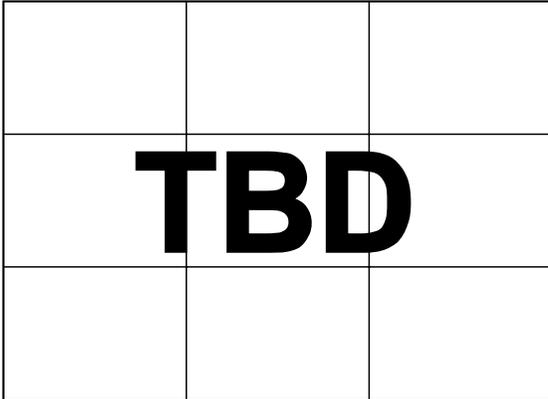


Figure 17. AD8191 Evaluation Board Schematic

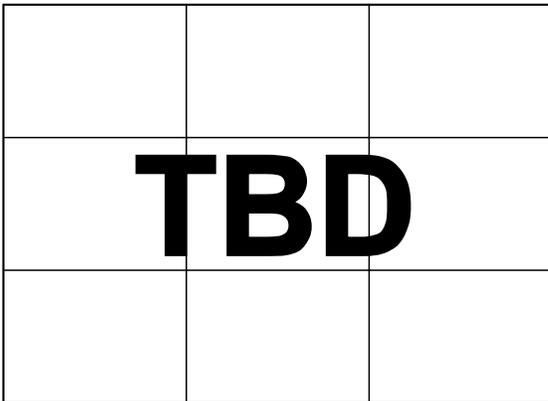


Figure 18. Evaluation Board Layout of the TMDS Traces

The AD8191 is an HDMI/DVI switch featuring equalized TMDS inputs and pre-emphasized TMDS outputs. It is intended for use as a 4:1 switch in systems with long cable runs on both the input and/or the output, and is fully HDMI 1.2a receive compliant.

### PINOUT

The AD8191 was designed to have an HDMI/DVI receiver pinout at its input and a transmitter pinout at its output. This makes the AD8191 ideal for use in AVR-type applications where a designer would route both the inputs and the outputs directly to HDMI/DVI connectors. This type of layout is illustrated in the schematic for the AD8191 evaluation board (Figure 17) and in the layout of the evaluation board (Figure 18). When the AD8191 is used in receiver type applications, it is necessary to change the ordering of the output pins on the PCB to match up with the on-board receiver.

One advantage of the AD8191 in an AVR-type application is that all of the high speed signals can be routed on one side (the topside) of the board, as shown in Figure 17. In addition to 12 dB of input equalization, the AD8191 provides up to 6 dB of output pre-emphasis that boosts the output TMDS signals and allows the AD8191 to precompensate when driving long PCB

traces or output cables. The net effect of the input equalization and output pre-emphasis of the AD8191 is that the AD8191 can compensate for the signal degradation of both input and output cables; it acts to reopen a closed input data eye and transmit a full-swing HDMI signal to an end receiver.

The AD8191 also provides a distinct advantage in receive-type applications because it is a fully buffered HDMI/DVI switch. Although inverting the output pin order of the AD8191 on the PCB requires a designer to place vias in the high speed signal path, the AD8191 fully buffers and electrically decouples the outputs from the inputs. Therefore, the effects of the vias placed on the output signal lines are not seen at the input of the AD8191. The programmable output terminations also improve signal quality at the output of the AD8191. The PCB designer, therefore, has significantly improved flexibility in the placement and routing of the output signal path with the AD8191 over other solutions.

### CABLE LENGTHS AND EQUALIZATION

The AD8191 offers two levels of programmable equalization for the high speed inputs: 6 dB and 12 dB. The equalizer of the AD8191 is optimized for video data rates of 1.65 Gbps. It can equalize up to 20 meters of 24 AWG HDMI cable at data rates corresponding to the video format, 1080p.

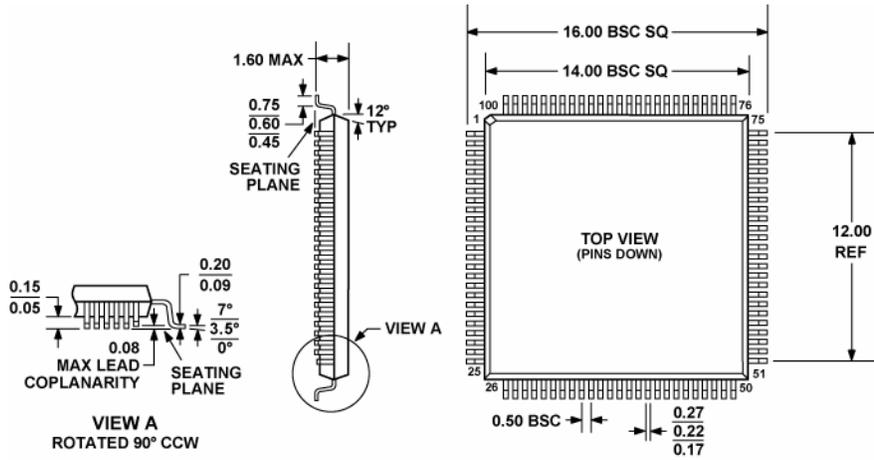
The length of cable that can be used in a typical HDMI/DVI application depends on a large number of factors including:

- Cable quality: the quality of the cable in terms of conductor wire gauge and shielding. Thicker conductors have lower signal degradation per unit length.
- Data rate: the data rate being sent over the cable. The signal degradation of HDMI cables increases with data rate.
- Edge rates: the edge rates of the source input. Slower input edges result in more significant data eye closure at the end of a cable.

- Receiver sensitivity: the sensitivity of the terminating receiver.

As such, specific cable types and lengths are not recommended for use with a particular equalizer setting. In nearly all applications, the AD8191 equalization level can be set to high, or 12 dB, for all input cable configurations at all data rates, without degrading the signal integrity.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026BED  
 THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 OF ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION

Figure 19. 100-Lead Quad Flat Package [LQFP]. Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8191	0°C to +70°C	100-Lead Low-profile Quad Flat Package [LQFP]	TBD

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