# MIC2564A

## Dual Serial PCMCIA/CardBus Power Controller

**Preliminary Information**

## General Description

The MIC2564A is dual-slot PC Card (PCMCIA) and CardBus power controller. It is a sophisticated power switching matrix that controls $V_{CC}$ and $V_{PP}$ voltages to two PC Card slots. The MIC2564A is used in conjunction with a serial-data output logic controller using the standard three-wire serial control data format.

When connected to 3.3V, 5V, and 12V system power supplies, the MIC2564A can switch its $V_{CC}$ outputs between 0V, 3.3V, 5.0V, and high-impedance states and $V_{PP}$ outputs between 0V, 3.3V, 5V, 12V, and high-impedance states. The $V_{CC}$ outputs will supply a minimum of 1A current to the socket and the $V_{PP}$ outputs will supply a minimum of 120mA to the socket. Voltage rise and fall times are well controlled. The MIC2564A also features an efficient standby (sleep) mode at 0.3µA typical quiescent current.

12V and 5V supplies are not required for MIC2564A operation making it possible to omit one or both supplies when they are not needed by the system. An internal charge pump supplies the internal bias voltages required for high-performance switching.

The MIC2564A is protected by overtemperature shutdown, and protects itself and the system with current limiting and cross-conduction lockout.

The MIC2564A is available in 24-pin SSOP and 24-pin TSSOP.

## Features

- Standard 3-wire serial control data input
- Controls two card slots from one surface mount device
- High-efficiency, low-resistance switches
- 12V supply optional (not required by MIC2564A)
- Current limit and overtemperature shutdown
- Ultralow 1µA-typical standby power consumption
- Cross-conduction lockout (no switching transients)
- Break-before-make switching
- 1A minimum $V_{CC}$ output per slot
- Independent $V_{CC}$ and $V_{PP}$ voltage output (MIC2564A-1)
- 120mA minimum $V_{PP}$ output current per slot
- 24-pin surface-mount SSOP and TSSOP packages

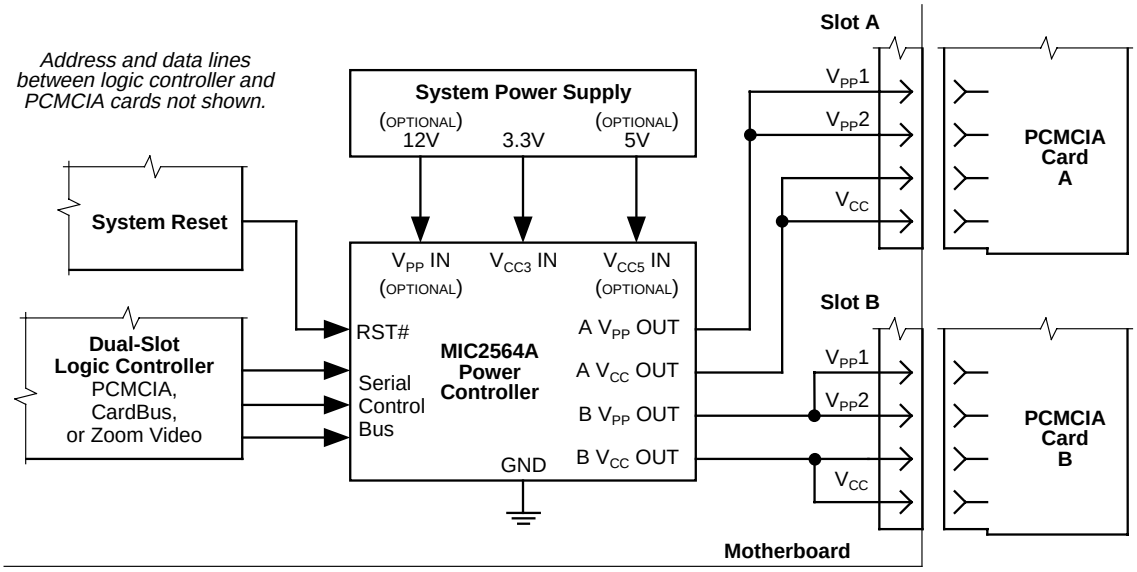
## Applications

- PC Card and CardBus power control
- Zoom Video port power control
- Wireless communications
- Bar code data collection systems
- Docking stations (portable and desktop)
- Power supply management

## Ordering Information

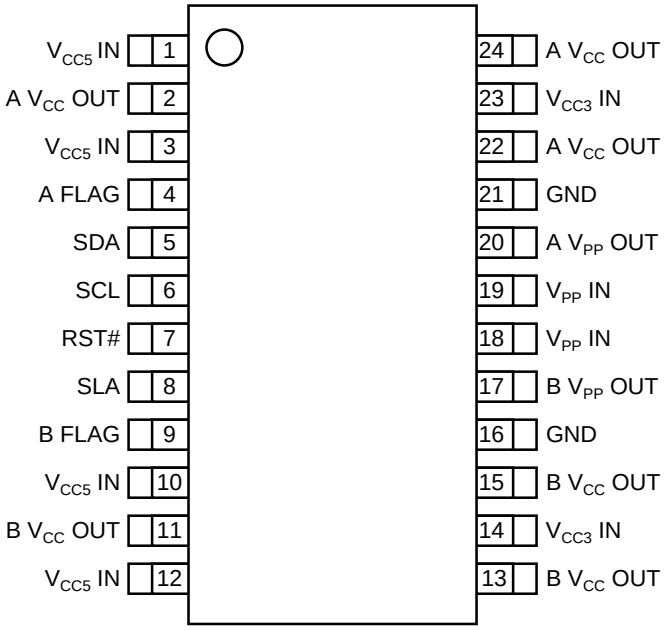
| Part Number | Temperature Range | Package |
|---|---|---|
| MIC2564A-0BSM | –40°C to +85°C | 24-pin SSOP |
| MIC2564A-1BSM | –40°C to +85°C | 24-pin SSOP |
| MIC2564A-0BTS | –40°C to +85°C | 24-pin TSSOP |
| MIC2564A-1BTS | –40°C to +85°C | 24-pin TSSOP |

## Typical Application




**PCMCIA Card Power Management Application**

## Pin Configuration




**24-lead SSOP (SM)**

**24-lead TSSOP (TS)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1,3,10,12 | $V_{CC5}$ IN | 5V Supply Input: Optional system power supply connection. Required only for 5V $V_{CC}$ and $V_{PP}$ output voltage. |
| 2,22,24 | A $V_{CC}$ OUT | Slot A $V_{CC}$ Output: Pins 2, 22, and 24 must be externally connected together. |
| 4 | A FLAG | Channel A $V_{CC}$ and $V_{PP}$ Output Monitor (Output): Low on error condition. |
| 5 | SDA | Serial Data (Input) |
| 6 | SCL | Serial Clock (Input) |
| 7 | RST# | System Reset (Input): Active low signal deactivates the MIC2564A, clearing the serial registers and forcing the four power outputs to 0V (GND). |
| 8 | SLA | Serial Data Latch (Input) |
| 9 | B FLAG | Channel B $V_{CC}$ and $V_{PP}$ Output Monitor (Output): Low on error condition. |
| 11,13,15 | B $V_{CC}$ OUT | Slot B $V_{CC}$ Output: Pins 11, 13, and 15 must be externally connected together. |
| 14,23 | $V_{CC3}$ IN | 3.3V Supply Input: Required system power supply connection. Powers 3.3V $V_{CC}$ and $V_{PP}$ outputs and all internal circuitry. |
| 16,21 | GND | Ground |
| 17 | B $V_{PP}$ OUT | Slot B $V_{PP}$ Output |
| 18,19 | $V_{PP}$ IN | 12V Supply Input: Optional system power supply connection. Required only for 12V $V_{PP}$ output voltage. |
| 20 | A $V_{PP}$ OUT | Slot A $V_{PP}$ Output |

## Absolute Maximum Ratings (Note 1)

$V_{PP}$ IN ..... +13.6V
$V_{CC3}$ IN ..... +6.0V
$V_{CC5}$ IN ..... +6.0V
$V_{SCL}$, $V_{SDA}$, $V_{SLA}$, $V_{RST\#}$ ..... –0.3V to +6.0V
$V_{A\ FLAG}$, $V_{B\ FLAG}$ ..... +6.0V
A or B $V_{PP}$ OUT ..... >120mA, Internally Limited
A or B $V_{CC}$ OUT ..... >1A, Internally Limited
Power Dissipation at $T_A \le 25°C$ ($P_D$) ..... Internally Limited
Storage Temperature ..... –65°C to +150°C
Lead Temperature (5 sec.) ..... +260°C
ESD Rating, **Note 3**

## Operating Ratings (Note 2)

$V_{PP}$ IN ..... 0V to +13.2V
$V_{CC3}$ IN ..... +3.0V to +5.5V
$V_{CC5}$ IN ..... 0V to +5.5V
$V_{SCL}$, $V_{SDA}$, $V_{SLA}$, $V_{RST\#}$ ..... 0V to +5.5V
A or B $V_{PP}$ OUT ..... 0 to 120mA
A or B $V_{CC}$ OUT ..... 0 to 1A
Clock Frequency ..... 0 to 2MHz
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Junction Temperature ($T_J$) ..... +125°C
Package Thermal Resistance ($\theta_{JA}$)
SSOP ..... 90˚C/W
TSSOP ..... 83˚C/W

## Electrical Characteristics

$V_{CC3}$ IN = 3.3V, $V_{CC5}$ IN = 5.0V, $V_{PP}$ IN = 12V; $T_A$ = 25°C, **bold** indicates –40°C ≤ $T_A$ ≤ +85°C; unless noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **$V_{PP}$ Output** | | | | | | |
| $I_{PP}$ OUT Hi-Z | High Impedance Output Leakage Current | shutdown mode $V_{PP}$ OUT = 0V | | 1 | 10 | µA |
| $I_{PPSC}$ | Short Circuit Current Limit | $V_{PP}$ OUT = 0V, normal mode, **Note 4** | 120 | 260 | 400 | mA |
| $R_O$ | Switch Resistance | $V_{PP}$ OUT = 5V selected, $I_{PP}$ OUT = –100mA (sourcing) | | 1.6 | **5** | Ω |
| | | $V_{PP}$ OUT = 3.3V selected, $I_{PP}$ OUT = –100mA (sourcing) | | 1.3 | **5** | Ω |
| | | $V_{PP}$ OUT = 12V selected, $V_{PP}$ IN = 12V, $I_{PP}$ OUT = –100 mA (sourcing) | | 1.3 | **2.3** | Ω |
| | | $V_{PP}$ OUT = 0V [ground] selected, $I_{PP}$ OUT = 50µA (sinking) | | 2000 | **5000** | Ω |
| **$V_{PP}$ Switching Time** (See Figure 2) | | | | | | |
| $t_1$ | Output Turn-On Delay, **Note 5** | $V_{PP}$ OUT = Hi-Z to 10% of 3.3V, $R_L$ = 100Ω | | 1 | 100 | µs |
| $t_2$ | | $V_{PP}$ OUT = Hi-Z to 10% of 5V, $R_L$ = 100Ω | | 1 | 100 | µs |
| $t_3$ | | $V_{PP}$ OUT = Hi-Z to 10% of 12, RL = 100Ω | | 50 | 250 | µs |
| $t_4$ | Output Rise Time | $V_{PP}$ OUT = 10% to 90% of 3.3, $R_L$ = 100Ω | 10 | 100 | 500 | µs |
| $t_5$ | | $V_{PP}$ OUT = 10% to 90% of 5, $R_L$ = 100Ω | 10 | 250 | 1000 | µs |
| $t_6$ | | $V_{PP}$ OUT = 10% to 90% of 12, $R_L$ = 100Ω | 10 | 100 | 500 | µs |
| $t_7$ | Output Transition Time, **Note 5** | $V_{PP}$ OUT = 3.3V to 90% of 12V, $R_L$ = 100Ω | 10 | 100 | 500 | µs |
| $t_8$ | | $V_{PP}$ OUT = 5V to 90% of 12, $R_L$ = 100Ω | 10 | 100 | 500 | µs |
| $t_9$ | | $V_{PP}$ OUT = 12V to 90% of 3.3, $R_L$ = 100Ω | 10 | 100 | 500 | µs |
| $t_{10}$ | | $V_{PP}$ OUT = 12V to 90% of 5, $R_L$ = 100Ω | 10 | 250 | 1000 | µs |
| $t_{11}$ | Output Turnoff Fall Time | $V_{PP}$ OUT = 90% to 10% of 3.3, $R_L$ = 100Ω | | 1 | 500 | µs |
| $t_{12}$ | | $V_{PP}$ OUT = 90% to 10% of 5, $R_L$ = 100Ω | | 1 | 500 | µs |
| $t_{13}$ | | $V_{PP}$ OUT = 90% to 10% of 12, $R_L$ = 100Ω | | 1 | 500 | µs |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{14}$ | Output Turnoff Delay Time, **Notes 5, 7** | $V_{PP}$ OUT = 3.3V to Hi-Z, $R_L$ = 100Ω | | 1 | 50 | µs |
| $t_{15}$ | | $V_{PP}$ OUT = 5V to Hi-Z, $R_L$ = 100Ω | | 1 | 50 | µs |
| $t_{16}$ | | $V_{PP}$ OUT = 12V to Hi-Z, $R_L$ = 100Ω | | 1 | 50 | µs |
| **$V_{CC}$ Output** | | | | | | |
| $I_{CC\ OUT}$ Hi-Z | High Impedance Output Leakage Current | shutdown mode, $V_{CC}$ OUT = 0V | | 1 | 20 | µA |
| $I_{CCSC}$ | Short Circuit Current Limit | $V_{CC}$ OUT = 0, normal mode, $V_{CC3}$ or $V_{CC5}$ switches, **Note 4** | 1.0 | 2.0 | 3.0 | A |
| $R_O$ | Switch Resistance | $V_{CC}$ OUT = 3.3V selected, $I_{CC}$ OUT = –1A (sourcing) | | 120 | **150** | mΩ |
| | | $V_{CC}$ OUT = 5V selected, $I_{CC}$ OUT = –1A (sourcing) | | 85 | **120** | mΩ |
| | | $V_{CC}$ OUT = 0V [ground] selected, $I_{CC}$ OUT = 0.1mA (sinking) | | 2000 | **3900** | Ω |
| **$V_{CC}$ Switching Time** (See Figure 3) | | | | | | |
| $t_{17}$ | Output Turn-On Delay Time, **Note 5** | $V_{CC}$ OUT = 0V to 10% of 3.3, $R_L$ = 10Ω | | 250 | 500 | µs |
| $t_{18}$ | | $V_{CC}$ OUT = 0V to 10% of 5.0, $R_L$ = 10Ω | | 500 | 1000 | µs |
| $t_{19}$ | Output Rise Time | $V_{CC}$ OUT = 10% to 90% of 3.3V, $R_L$ = 10Ω | 750 | 1200 | 5000 | µs |
| $t_{20}$ | | $V_{CC}$ OUT = 10% to 90% of 5, $R_L$ = 10Ω | 1000 | 2200 | 5000 | µs |
| $t_{21}$ | Output Fall Time | $V_{CC}$ OUT = 90% to 10% of 3.3, $R_L$ = 10Ω | 100 | 550 | 1000 | µs |
| $t_{22}$ | | $V_{CC}$ OUT = 90% to 10% of 5.0, $R_L$ = 10Ω | 100 | 400 | 2000 | µs |
| $t_{23}$ | Output Turnoff Delay, **Notes 5, 6** | $V_{CC}$ OUT = 3.3V to 90% of 3.3V , $R_L$ = 10Ω | | 400 | 2000 | µs |
| $t_{24}$ | | $V_{CC}$ OUT = 5V to 90% of 5V, $R_L$ = 10Ω | | 400 | 2000 | µs |
| **Power Supply** | | | | | | |
| $I_{CC3}$ | $V_{CC3}$ IN Supply Current (3.3V) **Note 7** | $V_{CC}$ OUT = 5V or 3.3V, $I_{CC}$ OUT = 0 | | 120 | 200 | µA |
| | | $V_{CC}$ OUT = Hi-Z (sleep mode) | | 5 | 10 | µA |
| $I_{CC5}$ | $V_{CC5}$ IN Supply Current (5V) **Note 8** | $V_{CC}$ OUT = 5V or 3.3V, $I_{CC}$ OUT = 0 | | 25 | 50 | µA |
| | | $V_{CC}$ OUT = Hi-Z (sleep mode) | | 0.2 | 10 | µA |
| $I_{PP}$ IN | $V_{PP}$ IN Supply Current (12V) **Note 8** | $V_{PP}$ OUT = 0V, 3.3V, 5V, or Hi-Z; $I_{PP}$ OUT = 0 | | 1 | 10 | µA |
| | | $V_{PP}$ OUT = $V_{PP}$ IN | | 4 | 50 | µA |
| $V_{CC3}$ | Operating Input Voltage (3.3V) | **Note 7** | 3.0 | 3.3 | 5.5 | V |
| $V_{CC5}$ | Operating Input Voltage (5V) | **Note 8** | — | 5.0 | 5.5 | V |
| $V_{PP}$ | Operating Input Voltage (12V) | **Note 8, 9** | — | 12 | 13.2 | V |
| **Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Temperature | | | 145 | | °C |
| **Serial Interface DC Specifications** | | | | | | |
| $V_{IH}$ | Input Voltage: SDA, SCL, SLA pins | | $0.7V_{CC3}$IN | | 5.5 | V |
| $V_{IL}$ | Input Voltage: SDA, SCL, SLA pins | | –0.3 | | $0.3V_{CC3}$IN | V |
| $I_{IN}$ | Input Current | 0V < $V_{IN}$ < 5.5V | –1 | 0.2 | 1 | µA |
| **Flag** | | | | | | |
| $I_{FLG}$ | Flag Leakage Current | $V_{FLG}$ = 5V | | | 1 | µA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Serial Interface Timing Requirements** (See Figure 1), **Note 10** | | | | | | |
| $t_{HD:DAT}$ | SDA Hold Time | | 75 | | | ns |
| $t_{SU:DAT}$ | SDA Setup Time | data before clock | 75 | | | ns |
| $t_{SU:SLA}$ | Latch Setup Time | | 50 | | | ns |
| $t_{SU:RST\#}$ | Reset to Data Setup Time | RST# before data | 50 | | | ns |
| $t_W$ | Minimum Pulse Width | clock ($t_{W:CLK}$) | 50 | | | ns |
| | | latch ($t_{W:SLA}$) | 100 | | | ns |
| | | reset ($t_{W:RST}$) | 50 | | | ns |
| | | data ($t_{W:DA}$) | 50 | | | ns |

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** Devices are ESD sensitive. Handling precautions recommended.

**Note 4.** Output enabled into short circuit.

**Note 5.** Measurement is from the 50% point of the SLA rising edge.

**Note 6.** Measurement is from the Hi-Z- or 0V-state command to the beginning of the slope. Measurement does not apply when device is in current limit or thermal shutdown.

**Note 7.** $V_{CC3}$ IN powers all internal logic, bias, and drive circuitry, and is required for operation.

**Note 8.** $V_{PP}$ and $V_{CC5}$ IN are not required for operation.

**Note 9.** $V_{PP}$ IN must be either high impedance or greater than or approximately equal to the highest voltage $V_{CC}$ in the system. For example, if both 3.3V and 5V are connected to the MIC2564A, $V_{PP}$ IN must be either 5V, 12V, or high impedance.

**Note 10.** Guaranteed by design not production tested.

## Serial Control Timing Diagram

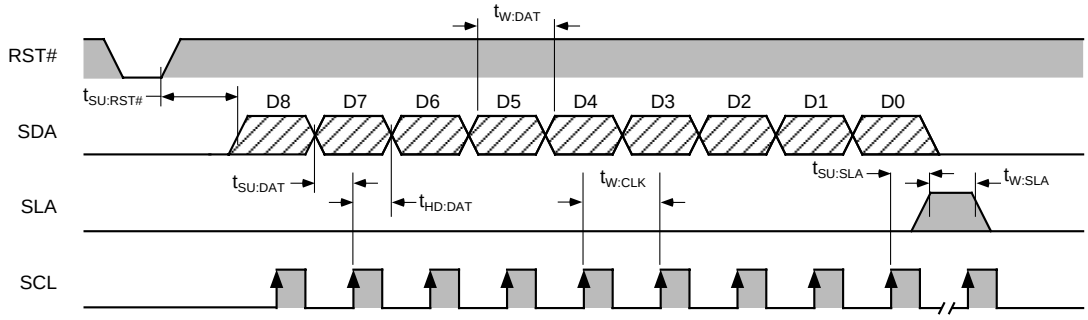



**Figure 1. Serial Control Timing Diagram**

The MIC2564A uses a three-wire serial interface to control $V_{CC}$ and $V_{PP}$ outputs for both sections A and B. The three control lines have thresholds compatible with both 3.3V and 5V logic families. Data (SDA) is clocked in on the rising clock edge. The clock signal may be continuous or it may halt after all data is clocked in.

## Output Timing Diagrams

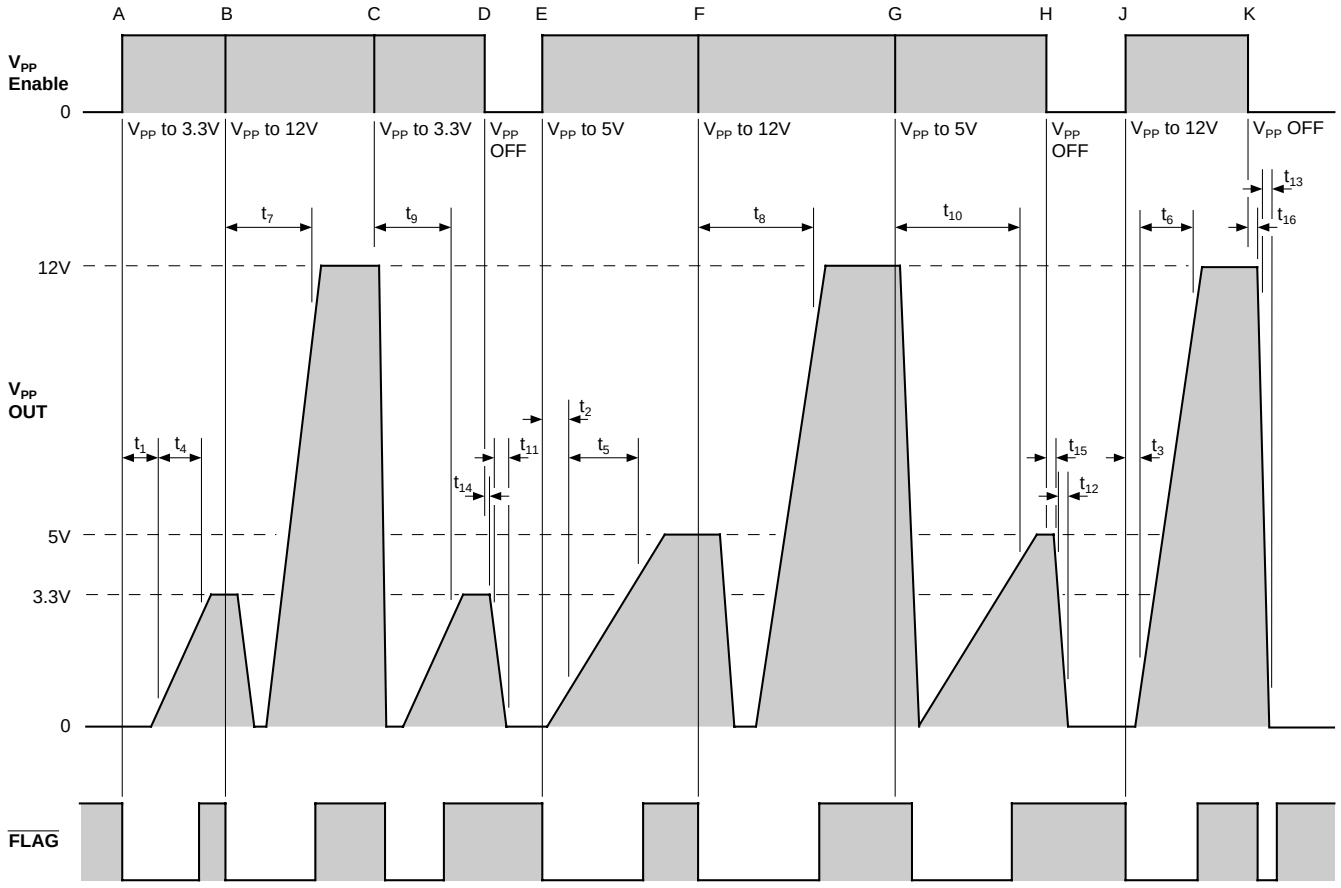



**Figure 2. $V_{PP}$ Timing Diagram**

$V_{PP}$ Enable is shown generically. $R_L$ = 100Ω. $C_L$ = negligible. Refer to the serial control timing diagrams for details.
At time **A**) $V_{PP}$ = 3.3V is selected, **B**) $V_{PP}$ is set to 12V, **C**) $V_{PP}$ = 3.3V (from 12V), **D**) $V_{PP}$ is disabled, **E**) $V_{PP}$ is programmed to 5V, **F**) $V_{PP}$ is set to 12V, **G**) $V_{PP}$ is programmed to 5V, **H**) $V_{PP}$ is disabled, **J**) $V_{PP}$ is set to 12V, **K**) $V_{PP}$ is again disabled.

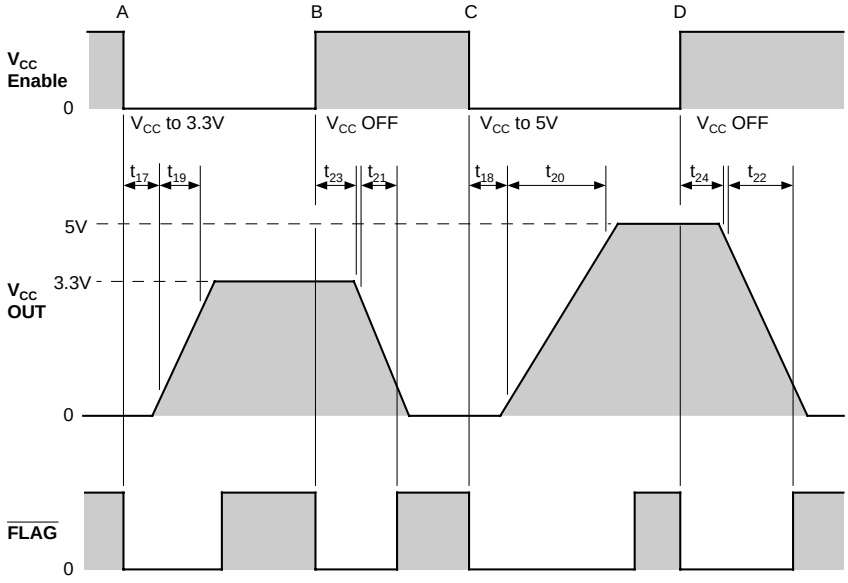



**Figure 3. $V_{CC}$ Timing Diagram**

$V_{CC}$ Enable is shown generically. $R_L$ = 10Ω. Refer to the serial control timing diagrams for specific control logic input.
At time **A**) $V_{CC}$ is programmed to 3.3V, **B**) $V_{CC}$ is disabled, **C**) $V_{CC}$ is programmed to 5V, **D**) $V_{CC}$ is disabled.

## MIC2564A-0 Logic Table

| D8 SHDN | D7 B $V_{CC}5$ | D6 B $V_{CC}3$ | D5 B $V_{PP\_VCC}$ | D4 B $V_{PP\_PGM}$ | D3 A $V_{CC}5$ | D2 A $V_{CC}3$ | D1 A $V_{PP\_VCC}$ | D0 A $V_{PP\_PGM}$ | B $V_{PP}$OUT | B $V_{CC}$OUT | A $V_{PP}$OUT | A $V_{CC}$OUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 1 | | | | | 0 | 0 | 0 | 0 | | | 0V* | 0V* |
| 1 | | | | | 0 | 0 | 0 | 1 | | | 12V† | 0V*† |
| 1 | | | | | 0 | 0 | 1 | 0 | | | 0V* | 0V* |
| 1 | | | | | 0 | 0 | 1 | 1 | | | Hi-Z | 0V* |
| 1 | | | | | 0 | 1 | 0 | 0 | | | 0V* | 3.3V |
| 1 | | | | | 0 | 1 | 0 | 1 | | | 12V | 3.3V |
| 1 | | | | | 0 | 1 | 1 | 0 | | | 3.3V | 3.3V |
| 1 | | | | | 0 | 1 | 1 | 1 | | | Hi-Z | 3.3V |
| 1 | | | | | 1 | 0 | 0 | 0 | | | 0V* | 5V |
| 1 | | | | | 1 | 0 | 0 | 1 | | | 12V | 5V |
| 1 | | | | | 1 | 0 | 1 | 0 | | | 5V | 5V |
| 1 | | | | | 1 | 0 | 1 | 1 | | | Hi-Z | 5V |
| 1 | | | | | 1 | 1 | 0 | 0 | | | 0V* | 0V* |
| 1 | | | | | 1 | 1 | 0 | 1 | | | 12V† | 0V† |
| 1 | | | | | 1 | 1 | 1 | 0 | | | 0V* | 0V* |
| 1 | | | | | 1 | 1 | 1 | 1 | | | Hi-Z | 0V* |
| 1 | 0 | 0 | 0 | 0 | | | | | 0V* | 0V* | | |
| 1 | 0 | 0 | 0 | 1 | | | | | 12V† | 0V*† | | |
| 1 | 0 | 0 | 1 | 0 | | | | | 0V* | 0V* | | |
| 1 | 0 | 0 | 1 | 1 | | | | | Hi-Z | 0V* | | |
| 1 | 0 | 1 | 0 | 0 | | | | | 0V* | 5V | | |
| 1 | 0 | 1 | 0 | 1 | | | | | 12V | 5V | | |
| 1 | 0 | 1 | 1 | 0 | | | | | 5V | 5V | | |
| 1 | 0 | 1 | 1 | 1 | | | | | Hi-Z | 5V | | |
| 1 | 1 | 0 | 0 | 0 | | | | | 0V* | 3.3V | | |
| 1 | 1 | 0 | 0 | 1 | | | | | 12V | 3.3V | | |
| 1 | 1 | 0 | 1 | 0 | | | | | 3.3V | 3.3V | | |
| 1 | 1 | 0 | 1 | 1 | | | | | Hi-Z | 3.3V | | |
| 1 | 1 | 1 | 0 | 0 | | | | | 0V* | 0V* | | |
| 1 | 1 | 1 | 0 | 1 | | | | | 12V† | 0V*† | | |
| 1 | 1 | 1 | 1 | 0 | | | | | 0V* | 0V* | | |
| 1 | 1 | 1 | 1 | 1 | | | | | Hi-Z | 0V* | | |

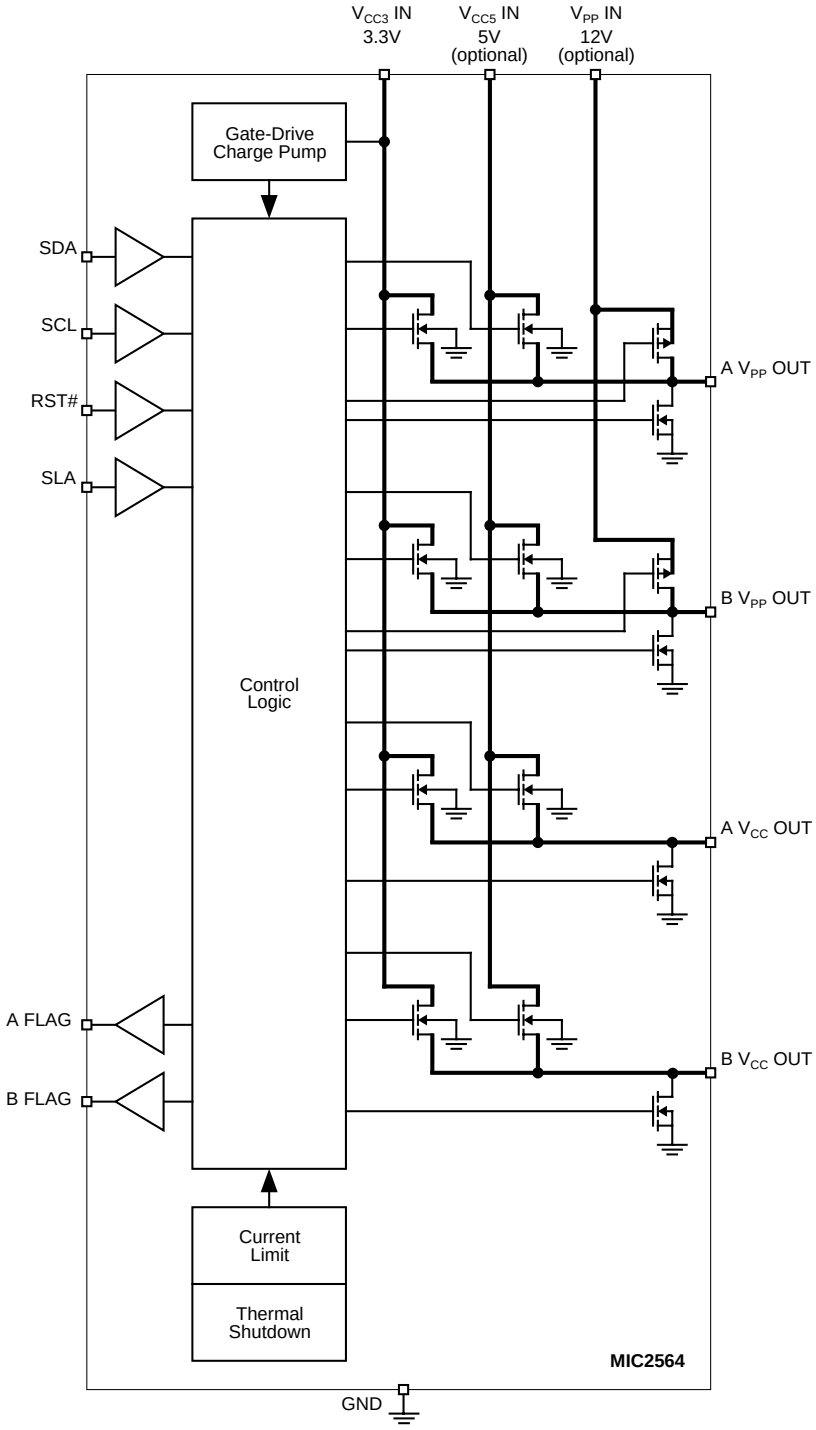
X = don't care, * clamped to ground, † illegal state per *The PC Card Specification*.

## MIC2564A-1 Logic Table

| D8 SHDN | D7 B $V_{CC}5$ | D6 B $V_{CC}3$ | D5 B $V_{PP\_VCC}$ | D4 B $V_{PP\_PGM}$ | D3 A $V_{CC}5$ | D2 A $V_{CC}3$ | D1 A $V_{PP\_VCC}$ | D0 A $V_{PP\_PGM}$ | B $V_{PP}$OUT | B $V_{CC}$OUT | A $V_{PP}$OUT | A $V_{CC}$OUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 1 | | | | | 0 | 0 | 0 | 0 | | | 0V* | 0V* |
| 1 | | | | | 0 | 0 | 0 | 1 | | | 12V† | 0V*† |
| 1 | | | | | 0 | 0 | 1 | 0 | | | 0V* | 0V* |
| 1 | | | | | 0 | 0 | 1 | 1 | | | Hi-Z | 0V* |
| 1 | | | | | 0 | 1 | 0 | 0 | | | 0V* | 3.3V |
| 1 | | | | | 0 | 1 | 0 | 1 | | | 12V | 3.3V |
| 1 | | | | | 0 | 1 | 1 | 0 | | | 3.3V | 3.3V |
| 1 | | | | | 0 | 1 | 1 | 1 | | | 5V | 3.3V |
| 1 | | | | | 1 | 0 | 0 | 0 | | | 0V* | 5V |
| 1 | | | | | 1 | 0 | 0 | 1 | | | 12V | 5V |
| 1 | | | | | 1 | 0 | 1 | 0 | | | 5V | 5V |
| 1 | | | | | 1 | 0 | 1 | 1 | | | 3.3V | 5V |
| 1 | | | | | 1 | 1 | 0 | 0 | | | 0V* | 0V* |
| 1 | | | | | 1 | 1 | 0 | 1 | | | 12V† | 0V† |
| 1 | | | | | 1 | 1 | 1 | 0 | | | 0V* | 0V* |
| 1 | | | | | 1 | 1 | 1 | 1 | | | Hi-Z | 0V* |
| 1 | 0 | 0 | 0 | 0 | | | | | 0V* | 0V* | | |
| 1 | 0 | 0 | 0 | 1 | | | | | 12V† | 0V*† | | |
| 1 | 0 | 0 | 1 | 0 | | | | | 0V* | 0V* | | |
| 1 | 0 | 0 | 1 | 1 | | | | | Hi-Z | 0V* | | |
| 1 | 0 | 1 | 0 | 0 | | | | | 0V* | 5V | | |
| 1 | 0 | 1 | 0 | 1 | | | | | 12V | 5V | | |
| 1 | 0 | 1 | 1 | 0 | | | | | 5V | 5V | | |
| 1 | 0 | 1 | 1 | 1 | | | | | 3.3V | 5V | | |
| 1 | 1 | 0 | 0 | 0 | | | | | 0V* | 3.3V | | |
| 1 | 1 | 0 | 0 | 1 | | | | | 12V | 3.3V | | |
| 1 | 1 | 0 | 1 | 0 | | | | | 3.3V | 3.3V | | |
| 1 | 1 | 0 | 1 | 1 | | | | | 5V | 3.3V | | |
| 1 | 1 | 1 | 0 | 0 | | | | | 0V* | 0V* | | |
| 1 | 1 | 1 | 0 | 1 | | | | | 12V† | 0V*† | | |
| 1 | 1 | 1 | 1 | 0 | | | | | 0V* | 0V* | | |
| 1 | 1 | 1 | 1 | 1 | | | | | Hi-Z | 0V* | | |

X = don't care, * clamped to ground, † illegal state per *The PC Card Specification*.

## Functional Diagram



## Applications Information

PC Card power control for two sockets is easily accomplished using the MIC2564A PC Card/CardBus power controller. Control commands from a three-wire (plus Reset) serial bus determine $V_{CC}$ and $V_{PP}$ output voltages and select standby or operate mode.

$V_{CC}$ outputs of 3.3V and 5V at the maximum allowable PC Card current are supported. The $V_{CC}$ outputs also support GND (0V) and high-impedance states. The $V_{PP}$ outputs support $V_{PP}$ (12V), $V_{CC}$ voltages (3.3V or 5V), GND (0V), or high impedance. When the $V_{CC}$ = Hi-Z (high impedance) condition is selected, the device switches into sleep mode and draws only leakage current.

Full protection during hot switching is provided which prevents feedback from the $V_{CC}$ output (for example, from the 5V supply into the 3.3V supply) by locking out the low voltage switch until the initial switch's gate voltage drops below 0.7V.

MIC2564A internal logic and MOSFET drive circuitry is powered from the $V_{CC3}$ input and internal charge-pump voltage multipliers. Switching speeds are carefully controlled to prevent damage to sensitive loads and meet all PC Card Specification timing requirements, including those for the CardBus option.

### Supply Bypassing

The MIC2564A is a switch and has no stability problems; however, supply bypass capacitors are recommended to reduce inductive transients and improve output ripple. As all internal device logic and comparison functions are powered from the $V_{CC3}$ input, the power supply quality on this line is the most important. Micrel recommends placing 1µF surface-mount ceramic (low ESR) capacitors from $V_{CC3}$ IN and $V_{CC5}$ IN pins to ground and two 0.1µF surface-mount ceramic capacitors, one from each $V_{PP}$ IN pin, to ground. Also, the $V_{CC}$ OUT and $V_{PP}$ OUT pins may use 0.01µF to 0.1µF capacitors for noise reduction and to reduce the chance of ESD (electrostatic discharge) damage.

### Power Status Feedback (Flags)

Two flag outputs monitor the $V_{CC}$ and $V_{PP}$ output voltages on both slot A and B, falling low when the voltage is not proper. Use of these open-drain flag outputs is optional; if they are used, a pull-up resistor to either the 3.3V or 5V supply is required. Unused flag outputs may be left open.

### PC Card Slot Implementation

The MIC2564A is designed for full compatibility with the Personal Computer Memory Card International Association (PCMCIA) PC Card Specification including the CardBus and Zoom Video (ZV) options.

When a PC card is initially inserted, it should receive $V_{CC}$ (3.3V ± 0.3V or 5.0V ±5%). The initial voltage is determined by a combination of mechanical socket keys and voltage sense pins. The card sends a handshaking data stream to the logic controller, which then determines if this card requires $V_{PP}$ and if the card is designed for dual $V_{CC}$. If the card is compatible with, and requires, a different $V_{CC}$ level, the logic controller commands the power controller to make this change by disabling $V_{CC}$, waiting at least 100ms, and then re-enabling the other $V_{CC}$ voltage.

If no card is inserted, or the system is in sleep mode, the logic controller commands the MIC2564A to shut down $V_{CC}$. This also places the switch into a shutdown (sleep) mode, where current consumption drops to nearly zero, with only tiny CMOS leakage currents flowing.

Internal device control logic, MOSFET drive and bias voltage is powered from $V_{CC3}$ IN. The high voltage bias is generated by an internal charge pump multiplier. Input logic threshold voltages are compatible with common PC Card logic controllers using either 3.3V or 5V supplies.

### *PC Card Voltage Regulation*

The MIC2564A has been designed to meet or exceed PC Card voltage regulation specifications. The on-resistance of the FET switches will meet regulation requirements at 600mA and 1A respectively for $V_{CC}$ = 5V ±3% and 3.3V ±3%.

### *Flash Memory Implementation*

When programming flash memory (standard +12V flash memories), the PC Card slot logic controller enables $V_{PP}$ on the MIC2564A, which connects $V_{PP}$ IN (nominally +12V) to $V_{PP}$ OUT. The low on-resistance of the MIC2564A switch allows using a small bypass capacitor on the $V_{PP}$ OUT pins, with the main filtering performed by a large filter capacitor on $V_{PP}$ IN. (Usually the main power supply filter capacitor is sufficient.) Using a small-value capacitor such as 0.1µF on the output causes little or no timing delays.

The $V_{PP}$ OUT transition from $V_{CC}$ to 12.0V typically takes 200µs. After programming is completed, the logic controller signals to the MIC2564A, which then reduces $V_{PP}$ OUT to the $V_{CC}$ level. Break-before-make switching action and controlled rise times reduce switching transients and lower current spikes through the switch.

### Output Current and Protection

The MIC2564A meets or exceeds all PCMCIA specifications. MIC2564A output switches are capable of passing the maximum current needed by any PC Card. For system and card protection, output currents are internally limited. For full system protection, long term (longer than a few milliseconds) output short circuits invoke overtemperature shutdown, protecting the MIC2564A, the system power supplies, the card socket pins, board traces, and the PC Card. Individual internal status registers for each slot indicate when power problems exist.

### Control Bus Interface Overview

The MIC2564A power controller communicates with a logic controller (host adapter) via a 3-wire serial interface. A fourth control line attaches to the system reset line (RST#) and places all MIC2564A switches in the high impedance (off) state. The reset function is active low.

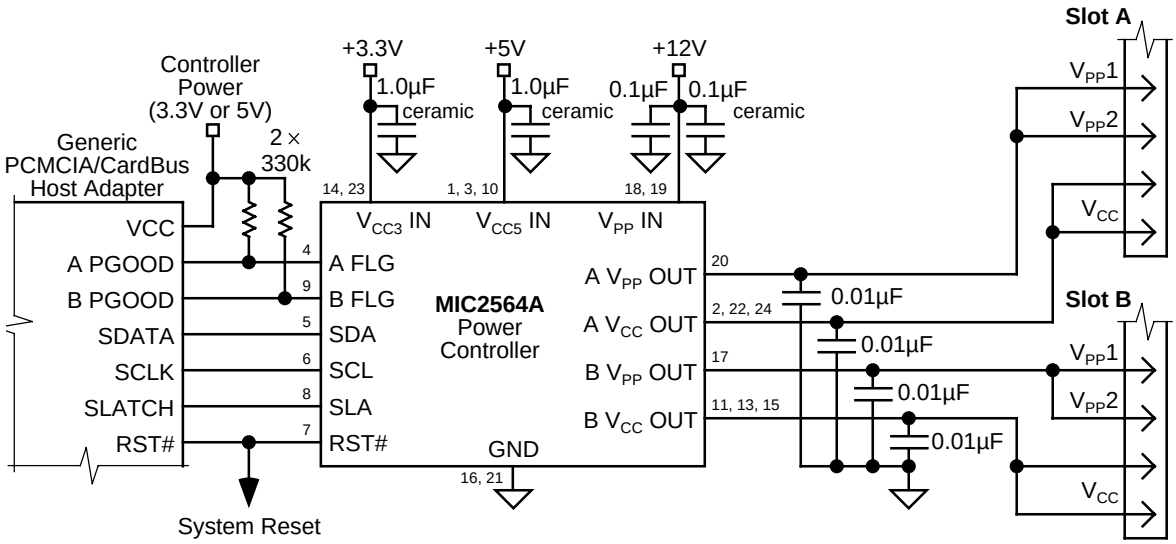



**Figure 4. Generic "3-Wire" Serial Control Interface**

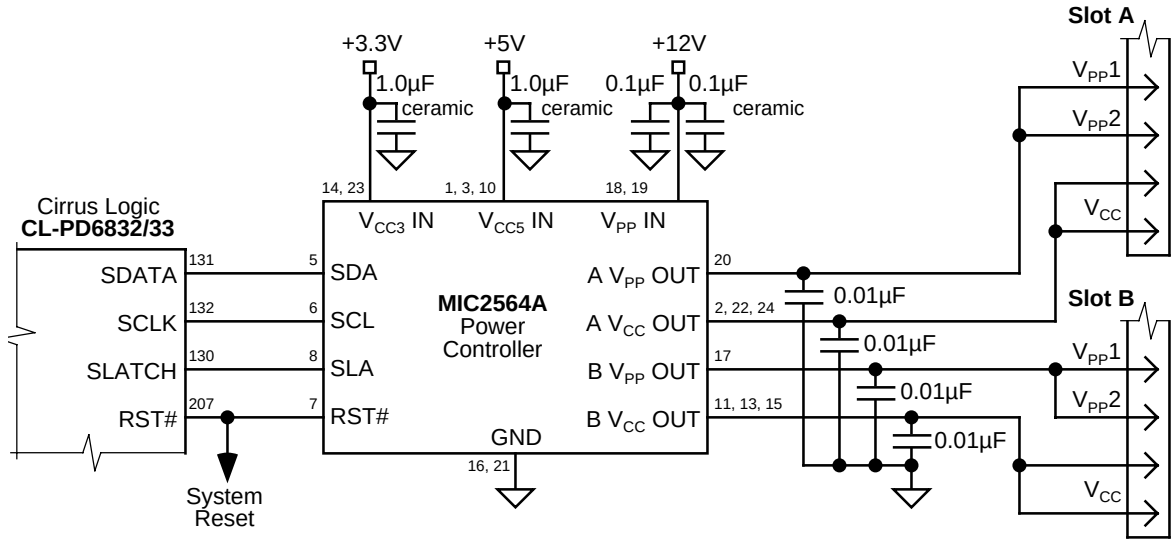



**Figure 5. Cirrus Logic CL-PD6832 and CL-PD6833 Interface**

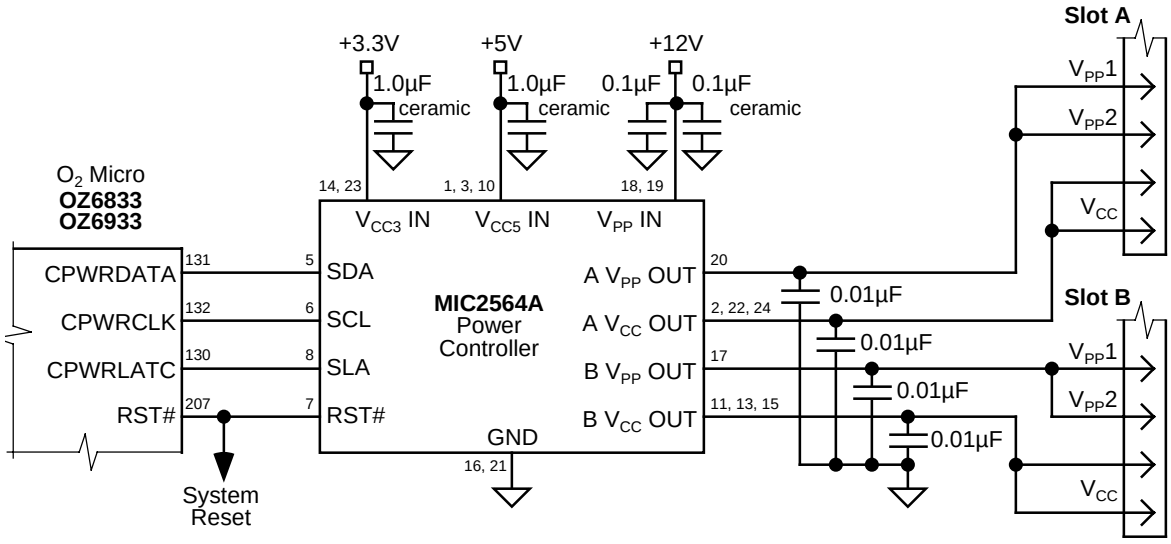



**Figure 6. $O_2$ Micro OZ6833 and OZ6933**

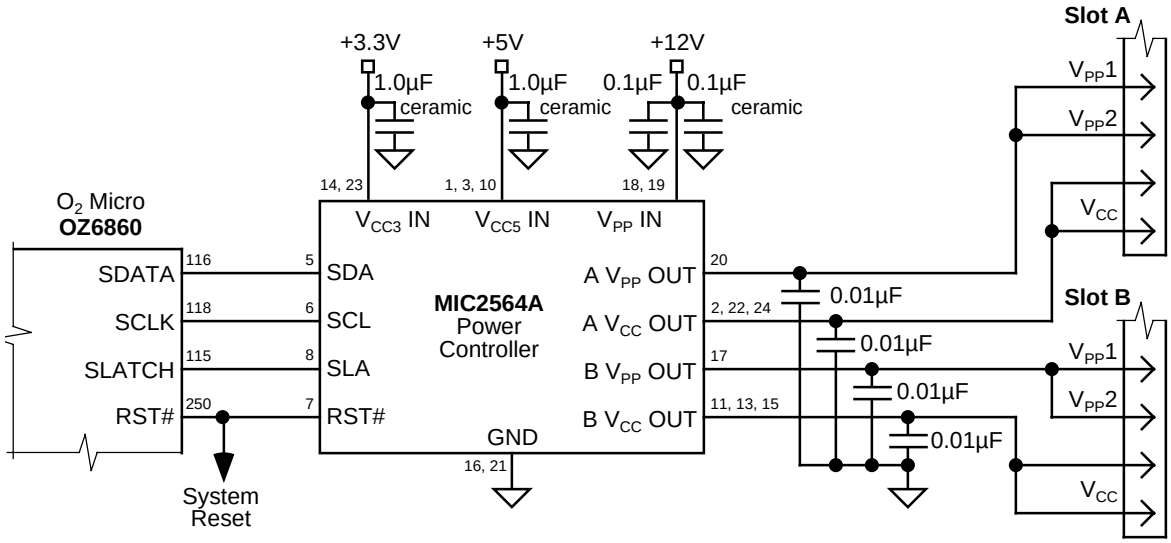
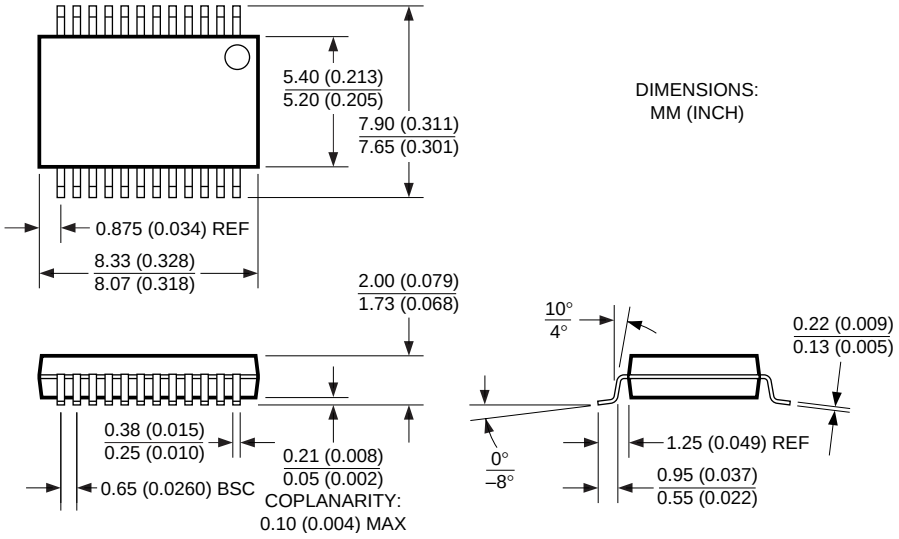
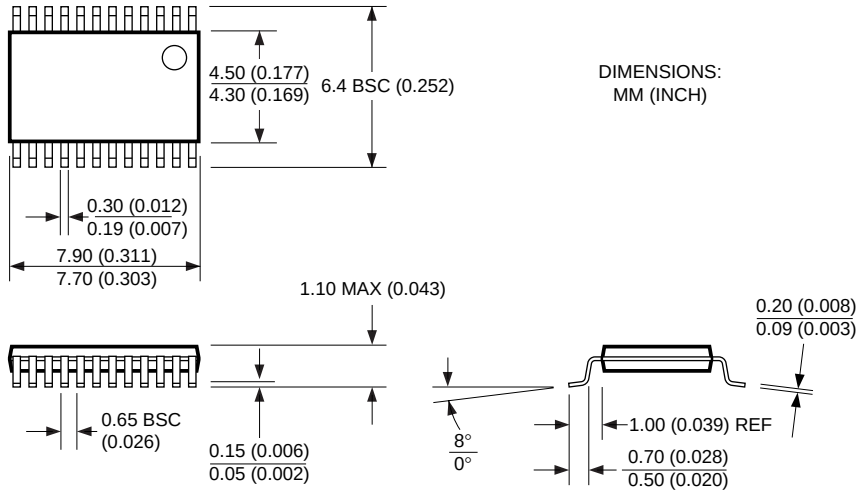



**Figure 7. $O_2$ Micro OZ6860**

## Package Dimensions




**24-pin SSOP (SM)**




**24-pin TSSOP (TM)**

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