Logic Controlled, 1 A, High-Side Load Switch with Reverse Current Blocking

Data Sheet **ADP198**

FEATURES

- Low RDS_{ON} of 50 mΩ @ 3.3 V (WLCSP only)
- Low input voltage range: 1.65 V to 6.5 V
- 1 A continuous operating current
- Built-in level shift for control logic that can be operated by 1.2 V logic
- Low 2.5 µA quiescent current @ V_{IN} = 2.8 V
- Low 1.1 µA shutdown current @ V_{IN} = 2.8 V
- Reverse current blocking
- Programmable start-up time
- Ultrasmall 1 mm × 1 mm, 4-ball, 0.5 mm pitch (WLCSP)
- Tiny 8-lead lead frame chip scale package (LFCSP)
  2.0 mm × 2.0 mm × 0.55 mm, 0.5 mm pitch

APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment

TYPICAL APPLICATION CIRCUITS

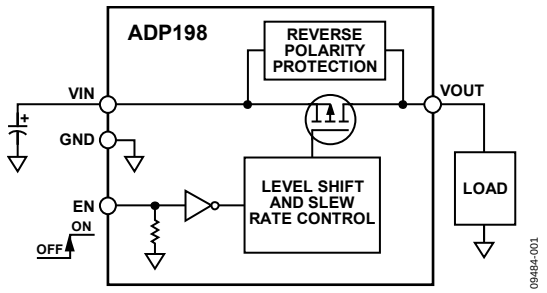

Figure 1. WLCSP

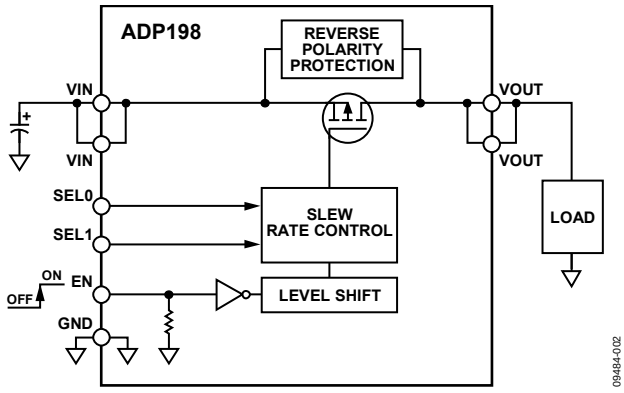

Figure 2. LFCSP

GENERAL DESCRIPTION

The ADP198 is a high-side load switch designed for operation between 1.65 V and 6.5 V that is protected against reverse current flow from output to input. A load switch provides power domain isolation, thereby helping to keep subsystems isolated and powered independently and enabling reduced power consumption. The ADP198 contains a low on-resistance P-channel MOSFET that supports more than 1 A of continuous load current. The low 2.5 µA quiescent current and ultralow shutdown current make the ADP198 ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the ADP198 compatible with modern processors and general-purpose input/output (GPIO) controllers. The LFCSP version also allows the user to program the start-up time to control the inrush current at turn on.

The ADP198 is available in an ultrasmall 1 mm × 1 mm, 4-ball, 0.5 mm pitch WLCSP. An 8-lead, 2 mm × 2 mm × 0.55 mm, 0.5 mm pitch LFCSP is also available.

Rev. B

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TABLE OF CONTENTS

REVISION HISTORY

11/11—Rev. A to Rev. B

Changes to WLCSP Turn-On Delay Time Parameter ... 3
Changes to Ordering Guide ... 16

10/11—Rev. 0 to Rev. A

Change to Features Section ... 1
Changes to Table 1, Specifications Section ... 3
Change to Ground Current Section ... 12
Changes to Enable Feature Section ... 13
Updated Outline Dimensions ... 16

10/11—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 2.8 V, EN = V_{IN}, I_{OUT} = 200 mA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +85°C	1.65		6.5	V
EN INPUT						
Threshold						
High	V_{IH}	$V_{IN} \leq 5$ V, T_J = −40°C to +85°C	1.2			V
		5 V < V_{IN}, T_J = −40°C to +85°C	1.3			V
Low	V_{IL}	1.65 V ≤ V_{IN} ≤ 6.5 V, T_J = −40°C to +85°C			0.43	V
Pull-Down Current	I_{EN}			500		nA
REVERSE BLOCKING						
V_{OUT} Current		V_{EN} = 0, V_{IN} = 0, V_{OUT} = 6.5 V		7		µA
		V_{EN} = 0, V_{IN} = 0, V_{OUT} = 6.5 V, T_J = −40°C to +85°C			13	µA
Hysteresis		$\lvert V_{IN} - V_{OUT} \rvert$		75		mV
CURRENT						
Quiescent Current	I_Q	I_{OUT} = 0 mA, T_J = −40°C to +85°C, includes EN pull-down current				
		V_{IN} = V_{OUT} = 2.8 V		2.5		µA
		V_{IN} = V_{OUT} = 6.5 V			20	µA
Off State Current	I_{OFF}	EN = GND		1.1		µA
		EN = GND, T_J = −40°C to +85°C			2	µA
		EN = GND, V_{OUT} = 0 V, T_J = −40°C to +85°C			2	µA
VIN to VOUT RESISTANCE	RDS_{ON}					
WLCSP		V_{IN} = 5 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		40		mΩ
		V_{IN} = 3.3 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		50	80	mΩ
		V_{IN} = 2.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		60		mΩ
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		130		mΩ
		V_{IN} = 1.65 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		180		mΩ
LFCSP		V_{IN} = 5 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		75	120	mΩ
		V_{IN} = 3.3 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		90		mΩ
		V_{IN} = 2.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		100		mΩ
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		120		mΩ
		V_{IN} = 1.65 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V		200		mΩ
VOUT TIME						
WLCSP						
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V, C_{LOAD} = 1 µF		7		µs
ADP198ACBZ-11-R7		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V, C_{LOAD} = 1 µF		460		µs
LFCSP						
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V, C_{LOAD} = 1 µF; SEL0 = L, SEL1 = L		7		µs
		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V, C_{LOAD} = 1 µF; SEL0 = H, SEL1 = L		90		µs
		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V, C_{LOAD} = 1 µF; SEL0 = L, SEL1 = H		195		µs
		V_{IN} = 3.6 V, I_{LOAD} = 200 mA, V_{EN} = 1.5 V, C_{LOAD} = 1 µF; SEL0 = H, SEL1 = H		460		µs

Timing Diagram

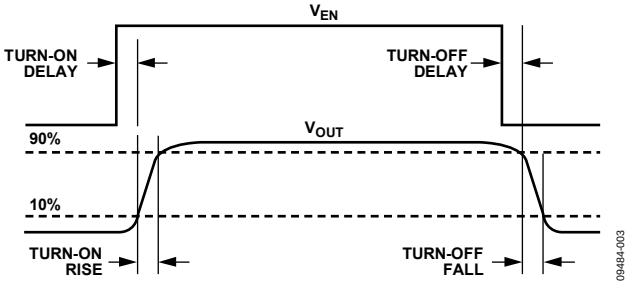


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND Pins	−0.3 V to +7 V
VOUT to GND Pins	−0.3 V to +7 V
EN to GND Pins	−0.3 V to +7 V
Continuous Drain Current	
T_A = 25°C	±1000 mA
T_A = 85°C	±1000 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP198 can be damaged if the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch PCB. Refer to JESD 51-7 and JESD 51-9 for detailed information regarding board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications.

Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8, JESD51-9, and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
4-Ball, 0.5 mm Pitch WLCSP	260	4	58.4	°C/W
8-Lead, 2 mm × 2 mm LFCSP	72.1	42.3	47.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

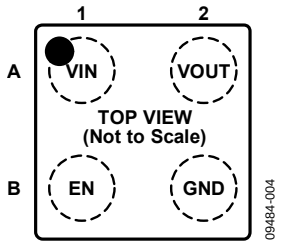
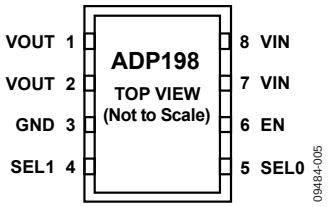


Figure 4. 4-Ball WLCSP Pin Configuration

Table 4. Pin Function Descriptions, WLCSP

Pin No.	Mnemonic	Description
A1	VIN	Input Voltage.
A2	VOUT	Output Voltage.
B1	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
B2	GND	Ground.



NOTES
1. THE EXPOSED PAD IS CONNECTED TO THE SUBSTRATE OF THE ADP198 AND MUST BE CONNECTED TO GROUND.

Figure 5. 8-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions, LFCSP

Pin No.	Mnemonic	Description
1	VOUT	Output Voltage. Connect Pin 1 and Pin 2 together.
2	VOUT	Output Voltage. Connect Pin 1 and Pin 2 together.
3	GND	Ground.
4	SEL1	Select Turn-On Time.
5	SEL0	Select Turn-On Time.
6	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
7	VIN	Input Voltage. Connect Pin 7 and Pin 8 together.
8	VIN	Input Voltage. Connect Pin 7 and Pin 8 together.
	EP	Exposed Pad. The exposed pad is connected to the substrate of the ADP198 and must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

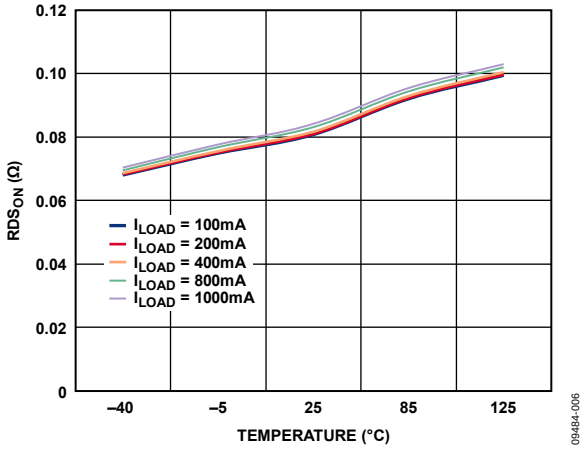


Figure 6. RDS_{ON} vs. Temperature, WLCSP

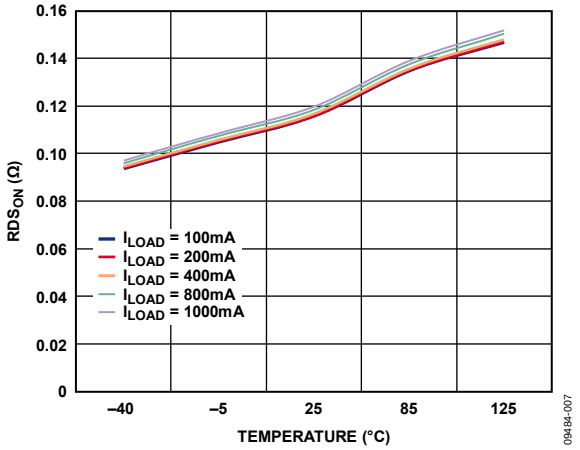


Figure 7. RDS_{ON} vs. Temperature, LFCSP

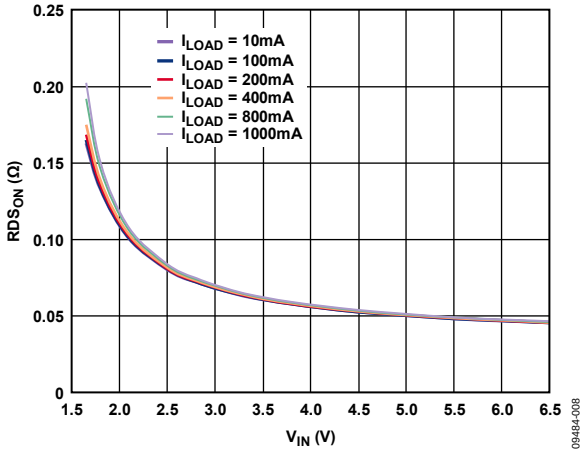


Figure 8. RDS_{ON} vs. Input Voltage (V_{IN}), WLCSP

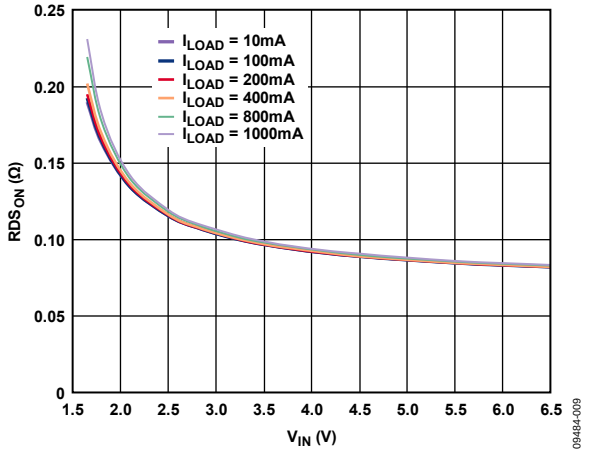


Figure 9. RDS_{ON} vs. Input Voltage (V_{IN}), LFCSP

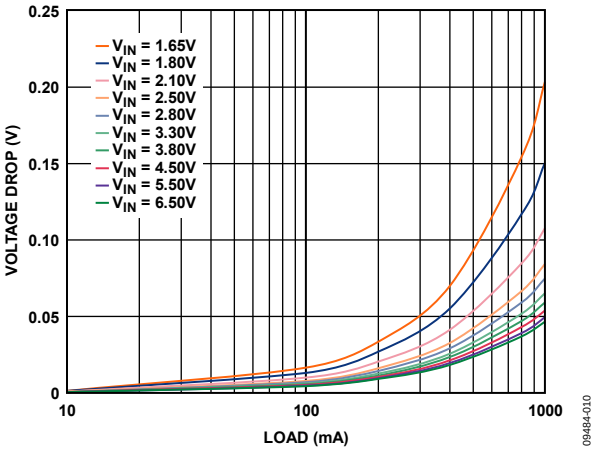


Figure 10. Voltage Drop vs. Load Current, WLCSP

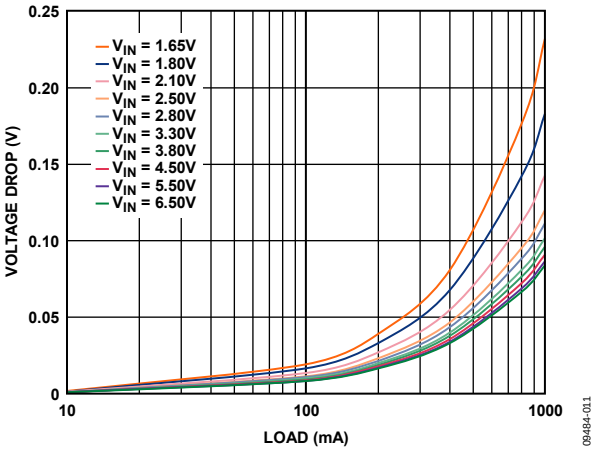


Figure 11. Voltage Drop vs. Load Current, LFCSP

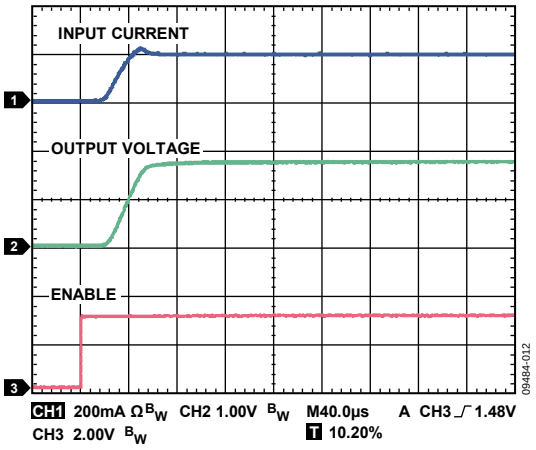


Figure 12. Typical Rise Time and Inrush Current, V_{IN} = 1.8 V, I_{LOAD} = 200 mA, Select Code 00

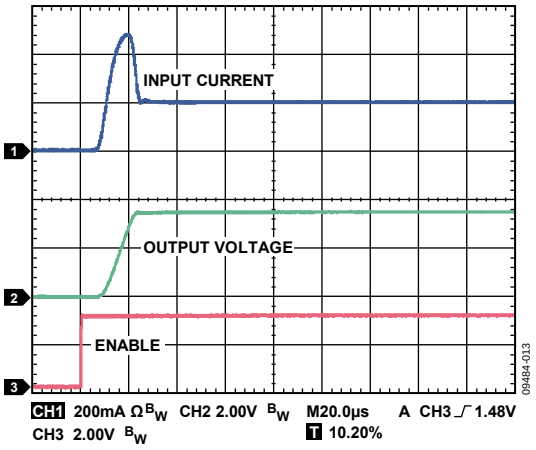


Figure 13. Typical Rise Time and Inrush Current, V_{IN} = 3.6 V, I_{LOAD} = 200 mA, Select Code 00

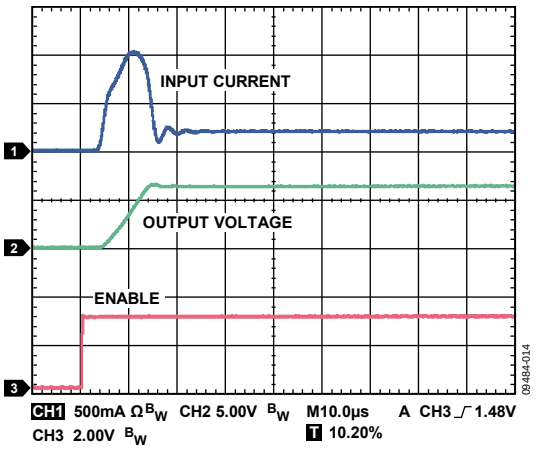


Figure 14. Typical Rise Time and Inrush Current, V_{IN} = 6.5 V, I_{LOAD} = 200 mA, Select Code 00

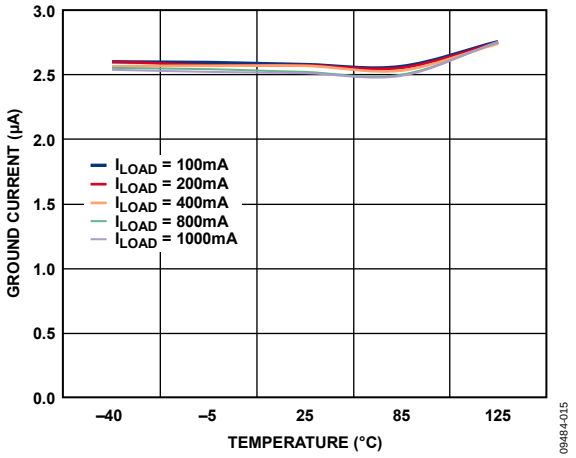


Figure 15. Ground Current vs. Temperature

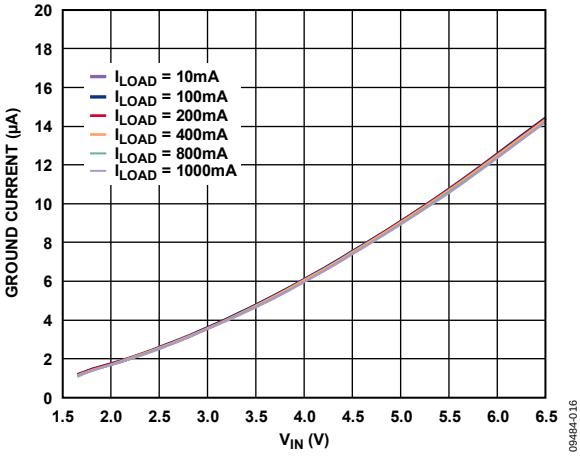


Figure 16. Ground Current vs. Input Voltage (V_{IN})

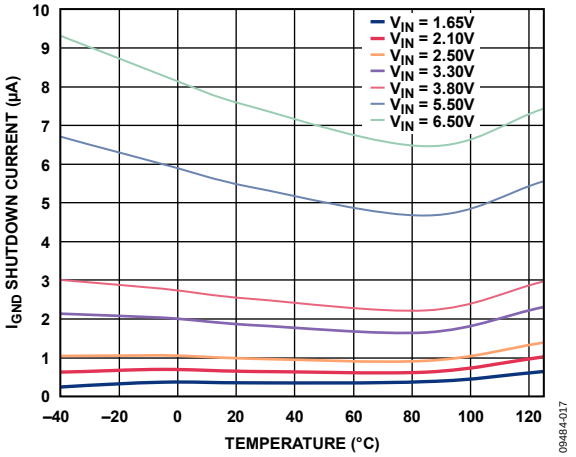


Figure 17. I_{GND} Shutdown Ground Current vs. Temperature, VOUT Open

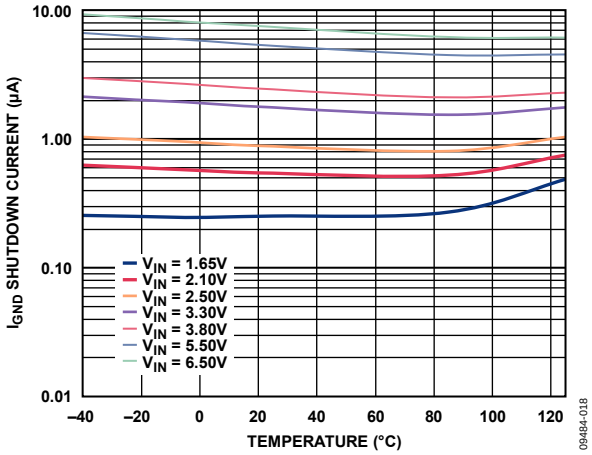


Figure 18. Shutdown Ground Current vs. Temperature, V_{OUT} = 0 V

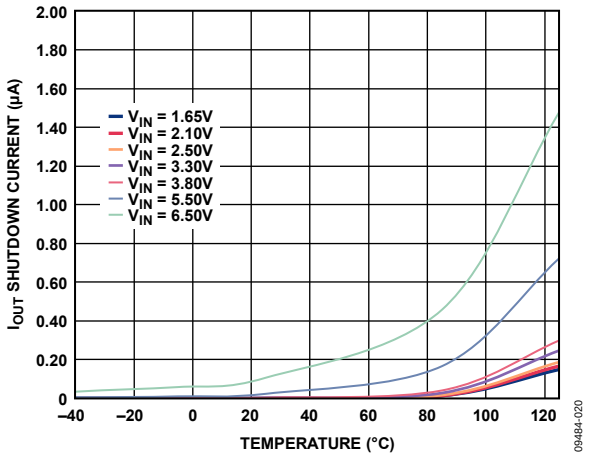


Figure 20. Reverse Input Shutdown Current vs. Temperature, V_{IN} = 0 V

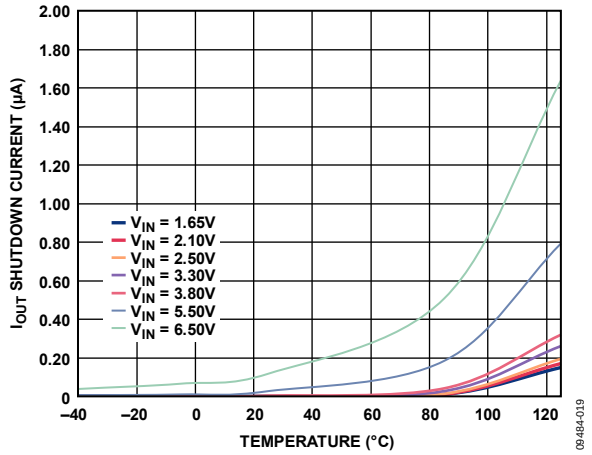


Figure 19. I_{OUT} Shutdown Current vs. Temperature, V_{OUT} = 0 V

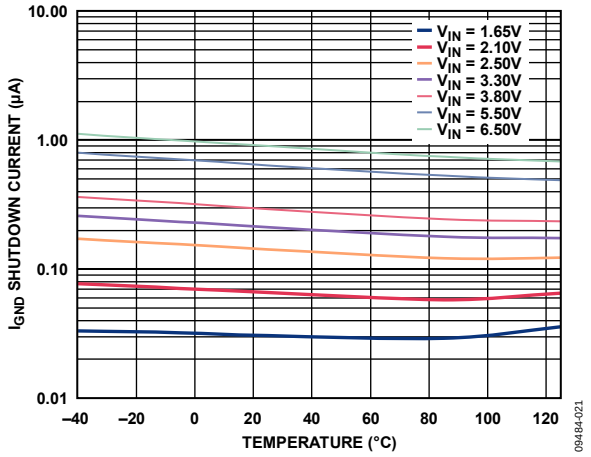


Figure 21. Reverse Shutdown Ground Current vs. Temperature, V_{OUT} = 0 V

THEORY OF OPERATION

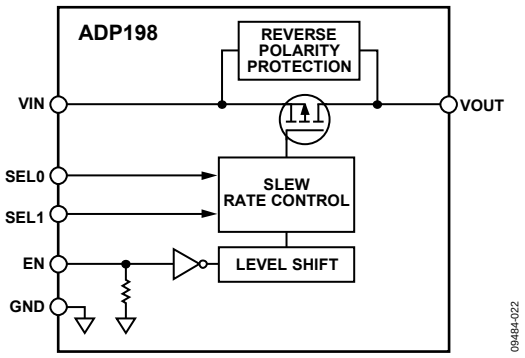


Figure 22. Functional Block Diagram

The ADP198 is a high-side PMOS load switch that is designed for supply operation between 1.65 V and 6.5 V. The PMOS load switch has a low on resistance of 50 mΩ at V_{IN} = 3.3 V and supports 1 A of continuous load current. The ADP198 features low quiescent current at 2.5 µA typical using a 2.8 V supply.

The enable input incorporates a nominal 4 MΩ pull-down resistor. SEL0 and SEL1 program the start-up time of the load switch to reduce inrush current when the switch is turned on.

The reverse current protection circuitry prevents current from flowing backwards through the ADP198 when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 75 mV, the body of the PFET is switched to VOUT and turned off or opened. In other words, the gate is connected to VOUT.

The packaging is a space-saving 1 mm × 1 mm, 4-ball WLCSP. The ADP198 is also available in a 2 mm × 2 mm × 0.55 mm, 0.5 mm pitch LFCSP.

APPLICATIONS INFORMATION

GROUND CURRENT

The major source for ground current in the ADP198 is an internal 4 MΩ pull-down resistor on the enable pin. Figure 23 shows the typical ground current when $V_{EN} = V_{IN}$ and varies from 1.65 V to 6.5 V.

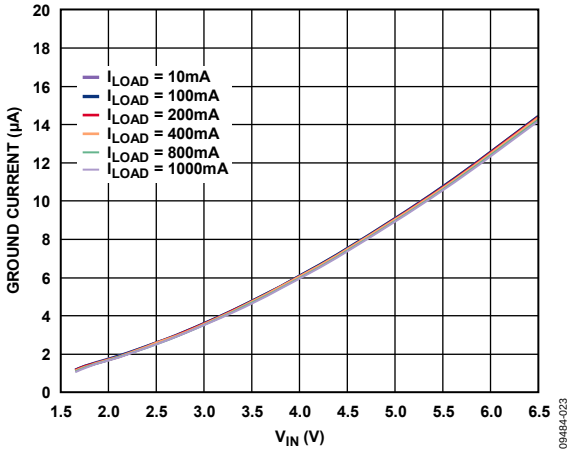


Figure 23. Ground Current vs. Load Current

As shown in Figure 24, an increase in quiescent current can occur when $V_{EN} \neq V_{IN}$. This is caused by the CMOS logic nature of the level shift circuitry as it translates a V_{EN} signal ≥1.2 V to a logic high. This increase is a function of the $V_{IN} - V_{EN}$ delta.

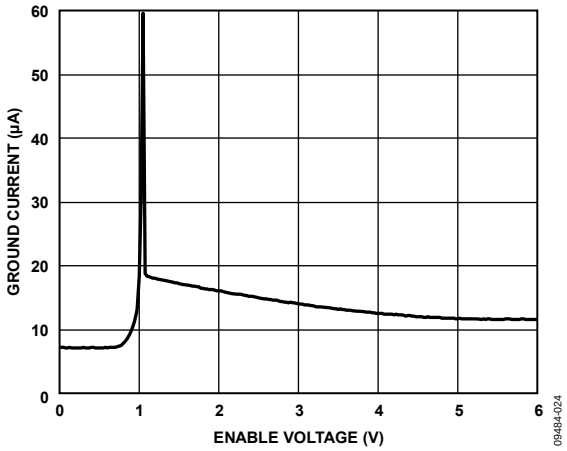


Figure 24. Typical Ground Current when $V_{EN} \neq V_{IN}$

ENABLE FEATURE

The ADP198 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 25, when a rising V_{EN} voltage crosses the active threshold, VOUT turns on. When a falling V_{EN} voltage crosses the inactive threshold, VOUT turns off.

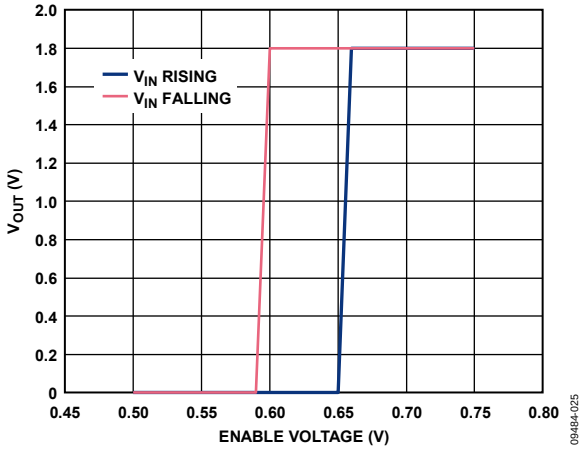


Figure 25. Typical EN Operation

As shown in Figure 25, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds derive from the V_{IN} voltage; therefore, these thresholds vary with the changing input voltage. Figure 26 shows the typical EN active/inactive thresholds when the input voltage varies from 1.65 V to 6.5 V.

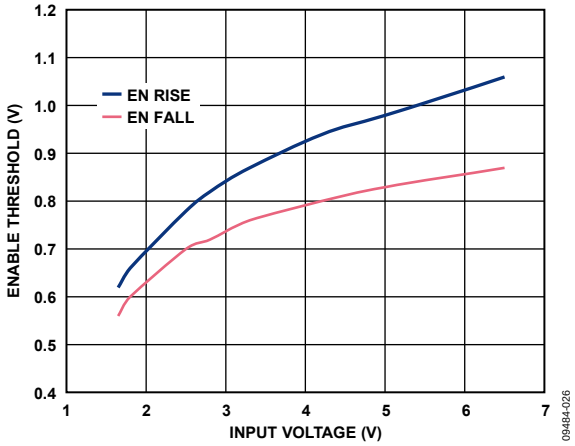


Figure 26. Typical EN Thresholds vs. Input Voltage (V_{IN})

TIMING

Turn-on delay is defined as the delta between the time that V_{EN} reaches >1.2 V and when V_{OUT} rises to ~10% of its final value. The ADP198 includes circuitry to have typical 10 µs turn-on delay at 3.6 V V_{IN} to limit the V_{IN} inrush current.

The rise time is defined as the delta between the time from 10% to 90% of V_{OUT} reaching its final value. It is dependent on the RC time constant where C = load capacitance (C_{LOAD}) and R = $RDS_{ON}||R_{LOAD}$. Because RDS_{ON} is usually smaller than R_{LOAD}, an adequate approximation for RC is $RDS_{ON} \times C_{LOAD}$. An input or load capacitor is not needed for the ADP198; however, capacitors can be used to suppress noise on the board. If significant load capacitance is connected, inrush current may be a concern.

Figure 27 through Figure 30 show the turn-on delay and output rise time for each of the four settings on SEL0 and SEL1.

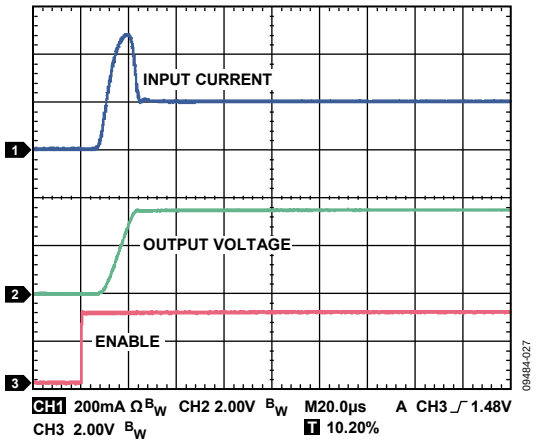


Figure 27. Typical Rise Time and Inrush Current, C_{LOAD} = 1 µF, V_{IN} = 3.6 V, I_{LOAD} = 200 mA, Code 00

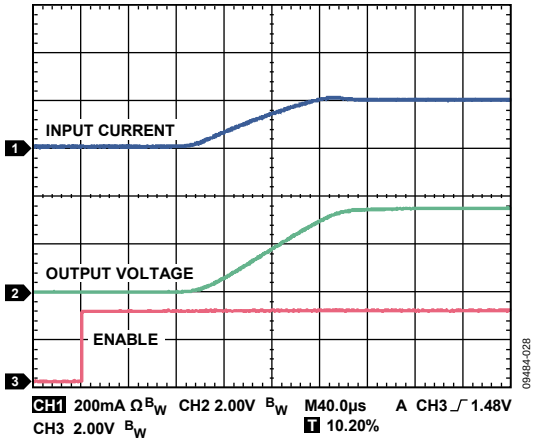


Figure 28. Typical Rise Time and Inrush Current, C_{LOAD} = 1 µF, V_{IN} = 3.6 V, I_{LOAD} = 200 mA, Code 01

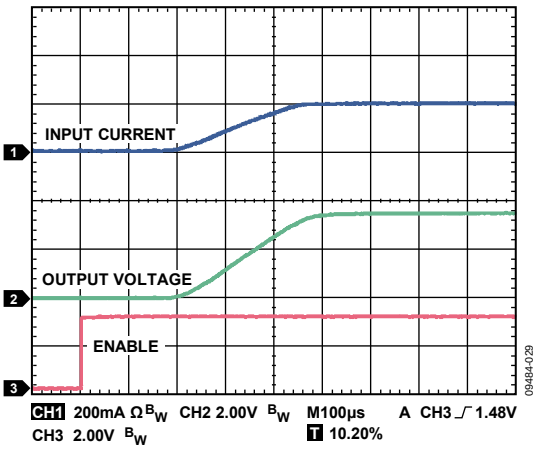


Figure 29. Typical Rise Time and Inrush Current, C_{LOAD} = 1 µF, V_{IN} = 3.6 V, I_{LOAD} = 200 mA, Code 10

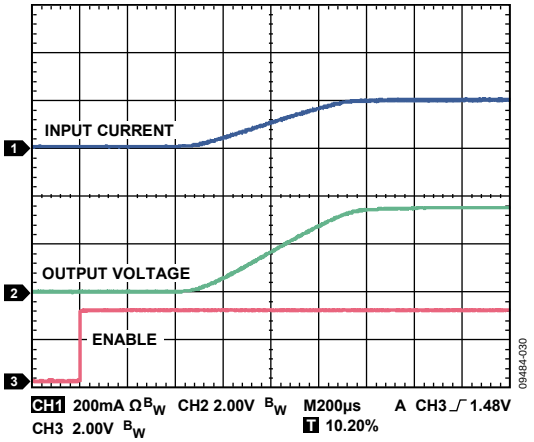


Figure 30. Typical Rise Time and Inrush Current, C_{LOAD} = 1 µF, V_{IN} = 3.6 V, I_{LOAD} = 200 mA, Code 11

The turn-off time is defined as the delta between the time from 90% to 10% of V_{OUT} reaching its final value. It is also dependent on the RC time constant.

Table 6. Start-Up Time Pin Settings

SEL0	SEL1	Start-Up Time (µs)
0	0	30
0	1	200
1	0	450
1	1	1100

DIODE OR'ing APPLICATIONS

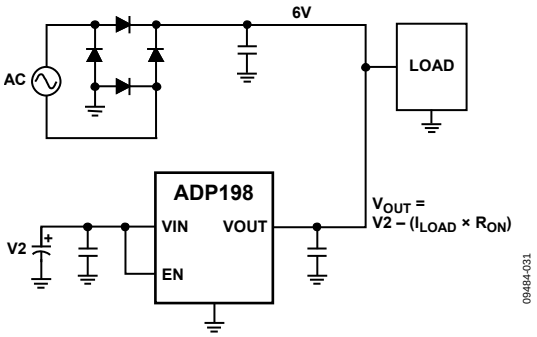


Figure 31. ADP198 in a Typical Diode OR'ing Application

Figure 31 shows an application wherein an ac power supply and battery are OR'ed together to provide a seamless transition from the primary (ac) supply to the secondary (V2) supply when the primary supply is disconnected. By connecting the enable input of the ADP198 to V2, the transition from ac power to battery power is automatic.

Figure 32 shows the forward voltage vs. the forward current characteristics of a Schottky diode and the ADP198. The low on resistance of the ADP198 makes it far superior to a Schottky diode in diode OR'ing applications.

In addition to low on resistance, the ADP198 reverse leakage current is much lower than a typical 1 A, 20 V Schottky rectifier. For example, at 85°C, the reverse current of a Schottky rectifier can be as high as 30 µA with only 2.5 V of reverse bias.

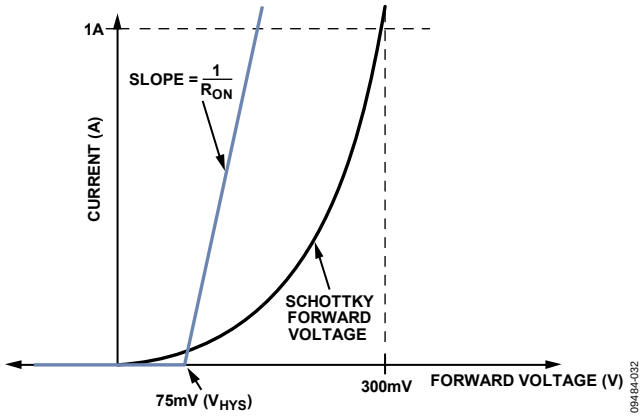


Figure 32. Forward Voltage vs. Forward Current of a Schottky Diode and ADP198

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

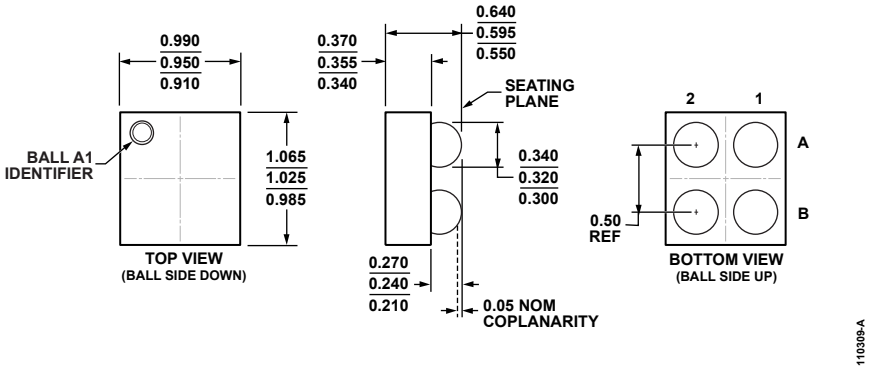


Figure 33. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-4)
Dimensions shown in millimeters

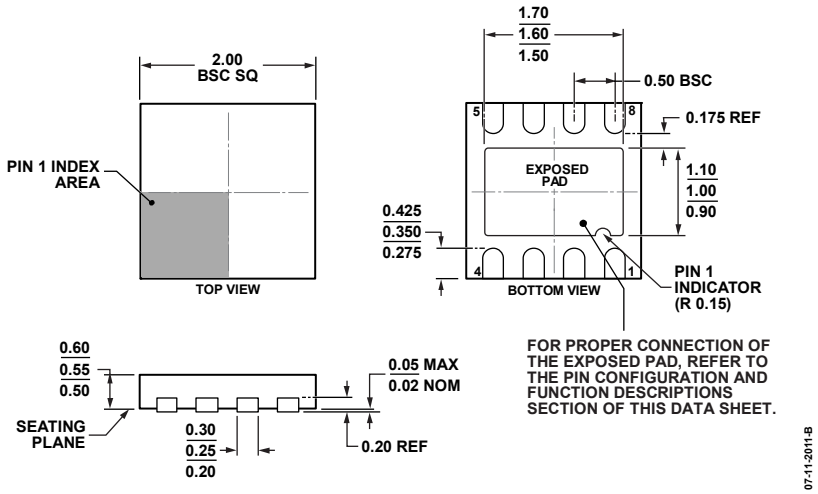


Figure 34. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Start-Up Time (µs)	Package Description	Package Option	Branding
ADP198ACBZ-R7	−40°C to +85°C	30	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-4	8C
ADP198ACBZ-11-R7	−40°C to +85°C	1000	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-4	2W
ADP198ACPZ-R7	−40°C to +85°C	Pin selectable: 30, 200, 450, and 1000	8-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	LJL
ADP198CP-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.