Multi-function I/O Drive

General Description

The SN7325 2-wire serial-interfaced peripheral features 16 I/O ports. Ports are divided into eight push pull I/Os and eight open-drain I/Os and transition detection.

Any of the 16 I/O ports can be configured as an input or an output. All I/O ports configured as inputs are continuously monitored for state changes (transition detection). State changes are indicated by the $\overline{INT}$ output. The interrupt is latched, allowing detection of transient changes. When the SN7325 is subsequently read through the serial interface, any pending interrupt is cleared.

The open-drain outputs are rated to sink 20mA at 0.26V headroom, and are capable of driving LEDs. The $\overline{RST}$ input clears the serial interface, terminating any I^2C communication to or from the SN7325. The SN7325 uses two address inputs to allow 4 I^2C slave addresses. The slave address also determines the power-up logic state for the I/O ports.

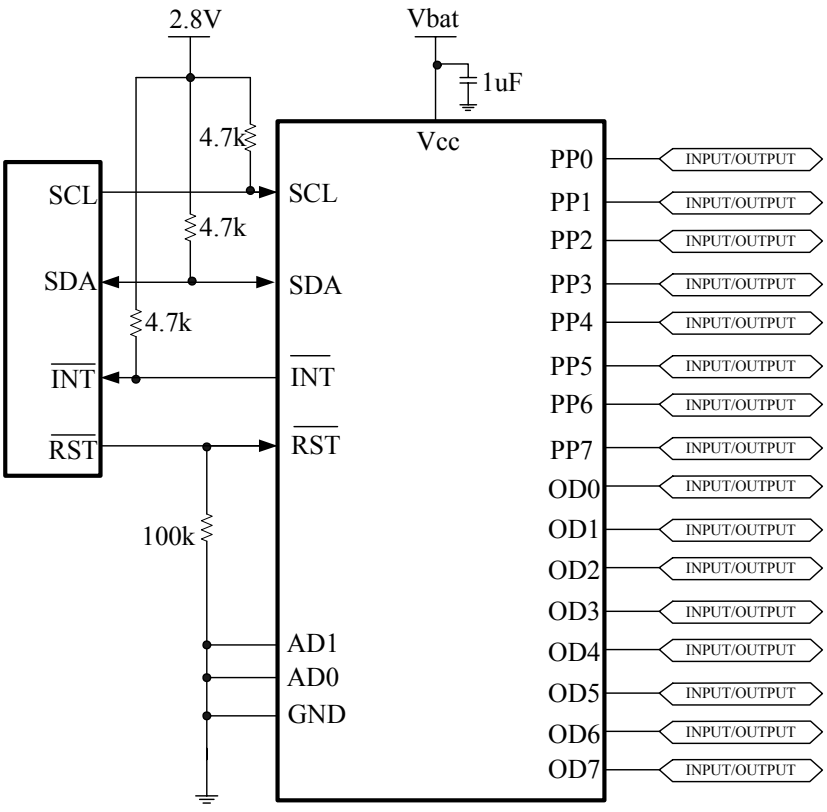
Features

- 400kHz I^2C Serial Interface
- 2.4V to 5.5V Operation
- 8 Push-Pull I/O ports
- 8 Open-Drain I/O Ports, Rated to 20mA Sink Current at 0.26V headroom
- Selectable I/O Port Power-Up Default Logic States
- $\overline{INT}$ Output Alerts Change on Inputs
- Low 0.3μA (typ) Standby Current
- -40°C to +125°C Temperature Range

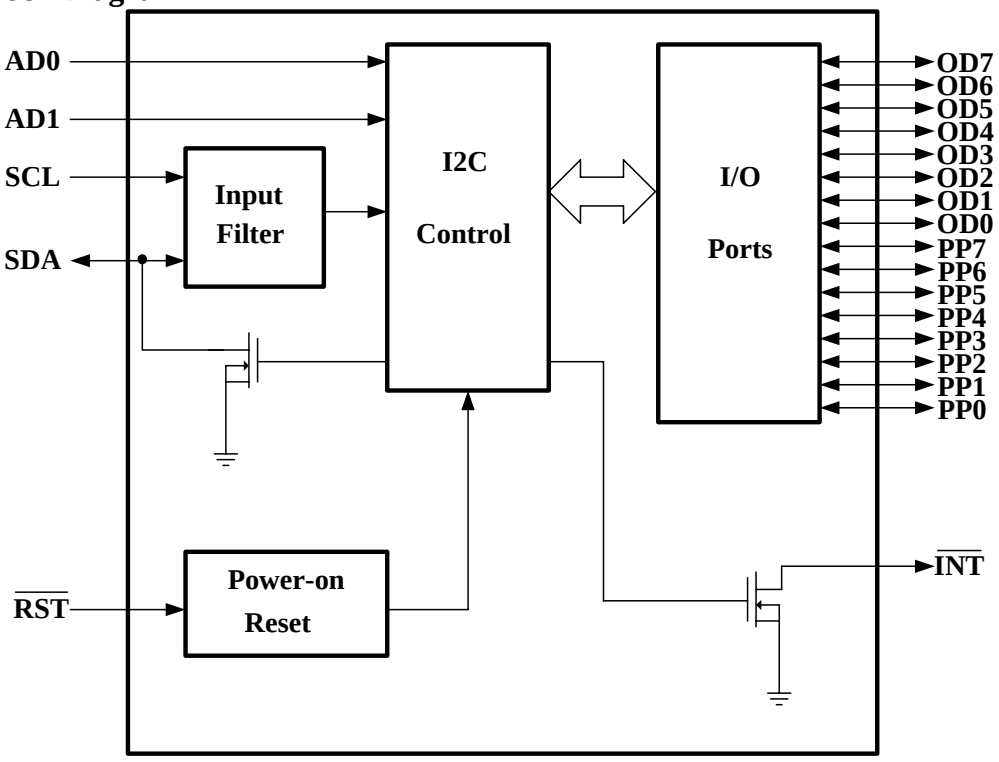
Applications

- Cell Phones
- Notebooks
- SAN/NAS
- Satellite Radio
- Servers
- Automotive

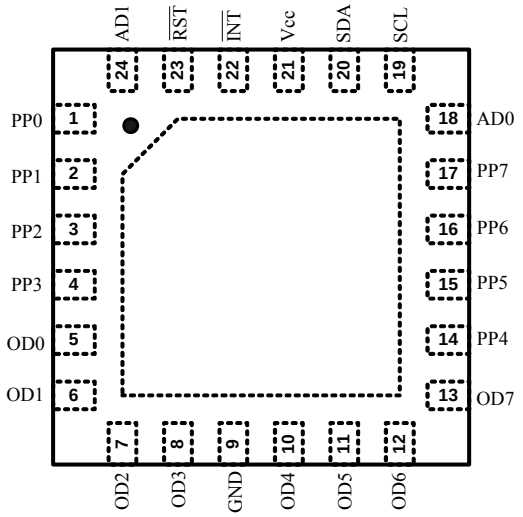
Typical Application Circuit



Functional Block Diagram



Pin Configurations

Package	Pin Configurations (Top View)
WQFN-24	

Pin Description

Pin	Pin	Description
1~4, 14~17	PP0~PP7	CMOS Push-Pull I/O Ports
5~8, 10~13	OD0~OD7	Open-Drain I/O Ports
9	GND	Ground
18,24	AD0,AD1	Address Inputs. Select device slave address with AD0 and AD1.
19	SCL	I^2C-Compatible Serial-Clock Input
20	SDA	I^2C-Compatible Serial-Data I/O
21	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with a ceramic capacitor of at least 0.1μF.
22	$\overline{INT}$	Interrupt Output, Active Low. $\overline{INT}$ is an open-drain output.
23	$\overline{RST}$	Reset Input, Active Low. Drive $\overline{RST}$ low to clear the 2-wire interface.

Absolute Maximum Ratings (All voltages referenced to GND)

Supply Voltage ……−0.3V to 6.0V

SCL, SDA, AD0, AD1, $\overline{RST}$, $\overline{INT}$, OD0-OD7…….
……−0.3V to 6V

PP0–PP7 .....−0.3V to (V_{CC} + 0.3V)

PP Source Output Current .....+100mA

PP, OD Sink Current 120mA

SDA Sink Current..... 10mA

$\overline{INT}$ Sink Current.....10mA

Continuous Power Dissipation (TA = 70°C)

24-Pin WQFN (derate 33.2mW/°C over 70°C) ……
……..……2.65W

Operating Temperature Range .....−40°C to +125°C

Junction Temperature.....150°C

Storage Temperature Range .....−65°C to 150°C

Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Ordering Information

Order Number	Package Type	Operating Temperature range
SN7325A424E	WQFN-24	-40 °C to +125°C

SN7325 □ □ □ □

- □: Environmental Code
  E: Lead Free
- □: Pin Code
  24: 24pins
- □: Package Type
  4: WQFN, 4mm×4mm
- □: Temperature Code
  A: Automotive, -40°C to +125°C

Electrical Characteristics

(V_{CC} = 2.4V to 5.5V, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = 25°C.) (Note 1)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	T_A = −40°C to +125°C		2.4		5.5	V
V_{POR}	Power-On-Reset Voltage	V_{CC} falling, Temp = −40°C				2.35	V
		V_{CC} falling, Temp = −20°C				2.3	
I_{STB}	Standby Current (Interface Idle)	SCL and SDA and other digital inputs at V_{CC}	T_A = −40°C to +125°C		0.3	1.9	µA
I+	Supply Current (Interface Running)	f_{SCL}=400kHz; other digital inputs at V_{CC}	T_A = −40°C to +125°C		8	20	µA
V_{IH}	Input High-Voltage SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7, PP0~PP7			1.4			V
V_{IL}	Input Low-Voltage SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7, PP0~PP7					0.4	V
I_{IH}, I_{IL}	Input Leakage Current SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7, PP0~PP7	SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7, PP0~PP7 at VCC or GND.		-0.2		+0.2	µA
C_{IN}	Input Capacitance SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7, PP0~PP7	(Note3)			10		pF
V_{OL}	Output Low Voltage, PP0~PP7, OD0~OD7	V_{CC} = 2.5V, I_{SINK} = 10mA				200	mV
		V_{CC} = 3.3V, I_{SINK} = 15mA				240	
		V_{CC} = 5.0V, I_{SINK} = 20mA				250	
V_{OH}	Output High Voltage PP0~PP7	V_{CC} = 2.5V, I_{SOURCE} = 5mA		V_{CC} −316			mV
		V_{CC} = 3.3V, I_{SOURCE} = 5mA		V_{CC} −213			
		V_{CC} = 5.0V, I_{SOURCE} = 10mA		V_{CC} −289			
V_{OLSDA}	Output Low-Voltage SDA	I_{SINK} = 6mA				180	mV
$V_{OL\overline{INT}}$	Output Low-Voltage $\overline{INT}$	I_{SINK} = 5mA				180	mV

Timing Characteristics

(V_{CC} = 2.4V to 5.5V, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = 25°C.) (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SCL}	Serial-Clock Frequency				400	kHz
t_{BUF}	Bus Free Time Between a STOP and a START Condition		1.3			µs
$t_{HD, STA}$	Hold Time (Repeated) START Condition		0.6			µs
$t_{SU, STA}$	Repeated START Condition Setup Time		0.6			µs
$t_{SU, STO}$	STOP Condition Setup Time		0.6			µs
$t_{HD, DAT}$	Data Hold Time	(Note 2)			0.9	µs
$t_{SU, DAT}$	Data Setup Time		100			ns
t_{LOW}	SCL Clock Low Period		1.3			µs
t_{HIGH}	SCL Clock High Period		0.7			µs
t_R	Rise Time of Both SDA and SCL Signals, Receiving	(Note 4)		20 + 0.1Cb	300	ns
t_F	Fall Time of Both SDA and SCL Signals, Receiving	(Note 4)		20 + 0.1Cb	300	ns
$t_{F, TX}$	Fall Time of SDA Transmitting	(Note 4)		20 + 0.1Cb	250	ns
t_{SP}	Pulse Width of Spike Suppressed	(Note 5)		50		ns
C_b	Capacitive Load for Each Bus Line				400	pF
t_W	$\overline{RST}$ Pulse Width		500			ns
$t_{\overline{RST}}$	$\overline{RST}$ Rising to START Condition Setup Time		1			µs

Port and Interrupt $\overline{INT}$ Timing Characteristic

(V_{CC} = 2.4V to 5.5V, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = 25°C.) (Note 3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Untis
Port Output Data Valid	t_{PV}	$C_L \leq$ 100pF			4	µs
Port Input Setup Time	t_{PSU}	$C_L \leq$ 100pF	0			µs
Port Input Hold Time	t_{PH}	$C_L \leq$ 100pF	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	$C_L \leq$ 100pF			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	$C_L \leq$ 100pF			4	µs

Note 1: All parameters are tested at T_A = 25°C. Specifications over temperature are guaranteed by design.
Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 3: Guaranteed by design.
Note 4: Cb = total capacitance of one bus line in pF. $I_{SINK} \leq$ 6mA. t_R and t_F measured between 0.3 × V_{CC} and 0.7× V_{CC}.
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Table 1 Power up default state for I/O Ports

Pin connection		Port Power Up Default															
AD1	AD0	PP 7	PP 6	PP 5	PP 4	PP 3	PP 2	PP 1	PP 0	OD 7	OD 6	OD 5	OD 4	OD 3	OD 2	OD 1	OD 0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GND	V_{CC}	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
V_{CC}	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
V_{CC}	V_{CC}	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Table 2 Command byte register

Command byte address(hex)	function	Power-up default	Protocol
00	Input port A (OD0~OD7)	XXXX XXXX	R
01	Input port B (PP0~PP7)	XXXX XXXX	R
02	Output port A	Refer to table1	R/W
03	Output port B	Refer to table1	R/W
04	Port A configuration	0000 0000	R/W
05	Port B configuration	0000 0000	R/W
06	Port A interrupt control	0000 0000	R/W
07	Port B interrupt control	0000 0000	R/W

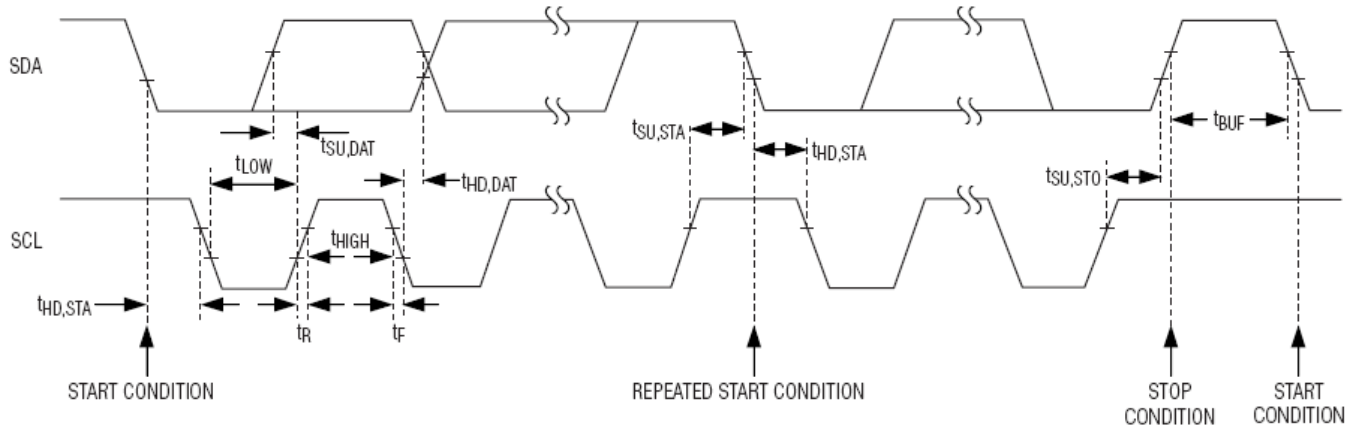


Figure 1. 2-Wire Serial Interface Timing Details

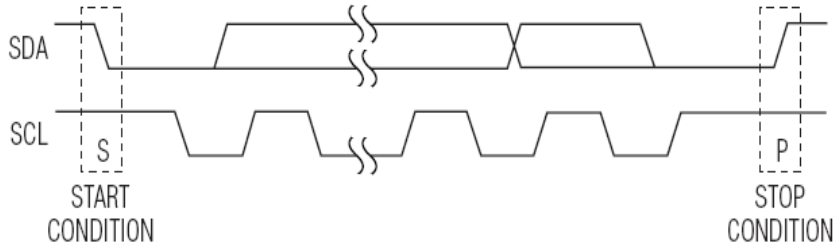


Figure 2. START and STOP Conditions

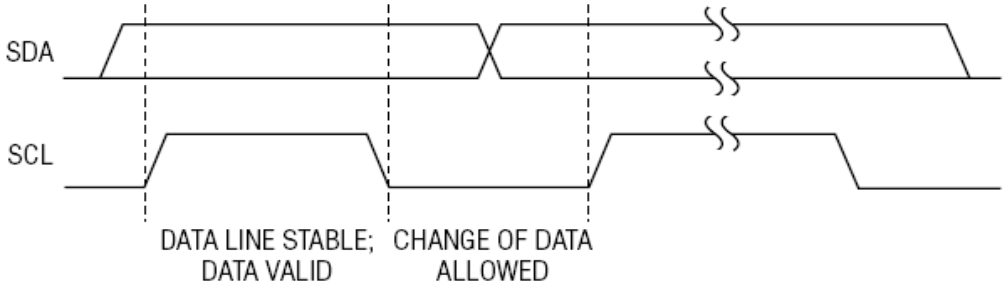


Figure 3. Bit Transfer

Detailed Description

Functional Overview

The SN7325 is a Multi-function I/O driver operating from a +2.4V to 5.5V supply with eight push-pull and eight open-drain I/O ports. Each open-drain and push-pull port is rated to sink 20mA at 0.26V headroom, and the entire device is rated to sink 320mA at 0.26V headroom into all ports combined. The outputs drive loads connected to supplies up to +5.5V.

The SN7325 is set to four I^2C slave addresses using the address select inputs AD0 and AD1, and is accessed over an I^2C serial interface up to 400 kHz. The $\overline{RST}$ input clears the serial interface in case of a bus lockup, terminating any serial transaction to or from the SN7325.

The SN7325 consists of input, output port registers, configuration registers and interrupt control register. All I/O ports offer latching transition detection when configured as inputs. All input ports are continuously monitored for changes.

A latching interrupt output, $\overline{INT}$, is programmed to flag logic changes on ports used as inputs. Data changes on any input port forces $\overline{INT}$ to a logic-low. Changing the I/O port level through the serial interface does not cause an interrupt. The interrupt output $\overline{INT}$ is cleared successfully by reading the corresponding input/output ports.

Ports default to logic-high or logic-low on power-up in groups of four (see Table 1).

Initial Power-Up

On power-up, the transition detection logic is reset, and $\overline{INT}$ is reset. The power-up default states of the 16 I/O ports are set according to the I2C slave address selection inputs, AD0 and AD1 (see Table 1). For I/O ports used as inputs, ensure that the default states are logic-high so that the I/O ports power up in the high impedance state.

Power-On Reset

The SN7325 contains an integral power-on-reset (POR) circuit that ensures all registers are reset to a known state on power-up. When VCC rises above VPOR (2.3V max), the POR circuit releases the registers and 2-wire interface for normal operation. When VCC drops to less than VPOR, the SN7325 resets all register contents to the POR defaults.

$\overline{RST}$ Input

The active-low $\overline{RST}$ input voids any I2C transaction involving the SN7325, forcing the SN7325 into the I2C STOP condition. A reset does not affect the interrupt output.

Standby Mode

When the serial interface is idle, the SN7325 automatically enters standby mode, drawing minimal supply current.

I/O Port Input Transition Detection

All I/O ports configured as inputs are monitored for changes since the expander was last accessed through the serial interface. The open-drain interrupt output, $\overline{INT}$, activates when one of the port pins changes states and only when the pin is configured as an input. The interrupt deactivates when the input/output register is read. A pin configured as an output does not cause an interrupt. Each 8-bit port register is read independently; therefore, an interrupt caused by port A (OD0~OD7) is not cleared by a read of port B (PP0~PP7)'s register.

Changing an I/O from an output to an input may cause a false interrupt to occur if the state of that I/O does not match the content of output port register. The SN7325 has interrupt control register to avoid false interrupt by setting the interrupt control register bit high firstly, when the I/O state is stable, clear the interrupt control register to enable the input transition detection function.

Accessing the SN7325

Serial Addressing

The SN7325 operates as a slave that sends and receives data through a 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to and from the SN7325, and generates the SCL clock that synchronizes the data transfer (see Figure 1).

SDA operates as both an input and an open-drain output. A pull up resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pull up resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the SN7325's 7-bit slave addresses plus R/W bits, 1 or more data bytes, and finally a STOP condition (see Figure 2).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (see Figure 2)

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

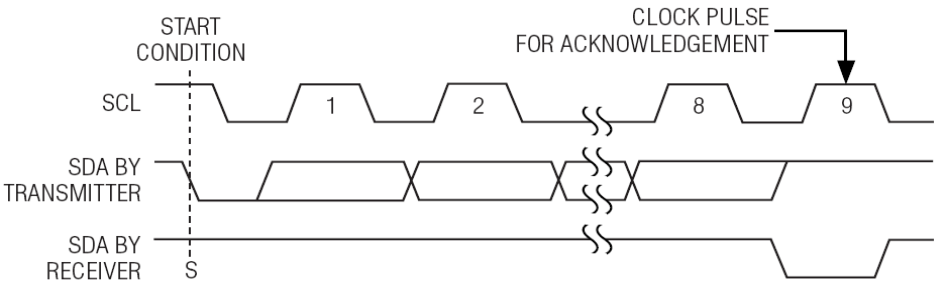


Figure 4. Acknowledge

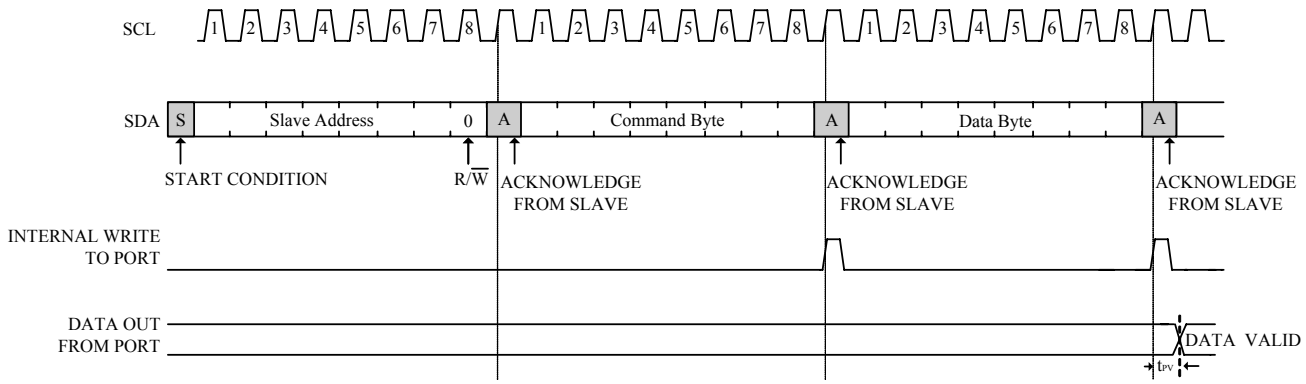


Figure 5.Writing to the SN7325

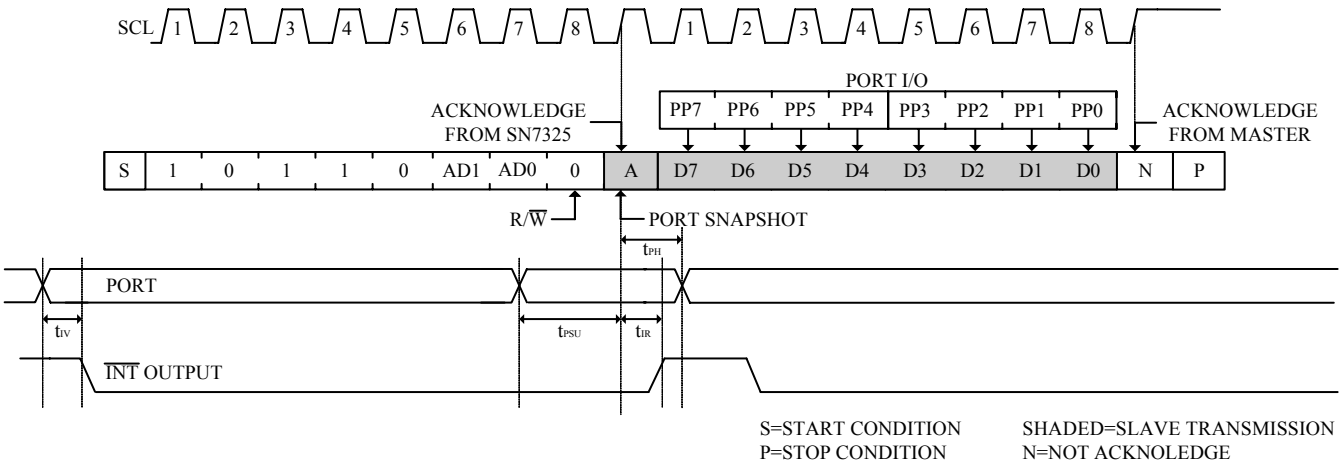


Figure 6.Reading I/O Ports of SN7325

Slave Address

The SN7325 has a 7-bit slave address. The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. Set this bit low for a write command and high for a read command.

The complete slave address is:

A6	A5	A4	A3	A2	A1	A0
1	0	1	1	0	AD1	AD0

Data Bus Transaction

The command byte is the first byte to follow the 8-bit device slave address during a write transmission (see Table 2). The command byte is used to determine which of the following registers are written or read.

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (see Figure 4). Each byte transferred effectively requires 9bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the SN7325, the device generates the acknowledge bit because the SN7325 is the recipient. When the SN7325 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Configuration Registers

The configuration registers configure the directions of the I/O pins. Set the bit in the respective configuration register to enable the corresponding port as an input. Clear the bit in the configuration register to enable the corresponding port as an output.

Interrupt Control Registers

The interrupt control registers control the interrupt function of I/O ports when the I/O port used as input. Set the bit in the respective interrupt control register to disable the corresponding port's interrupt function. Clear the bit in the interrupt control register to enable the corresponding port's interrupt function.

Writing to Port Registers

Transmit data to the SN7325 by sending the device slave address and setting the LSB to a logic zero. The command byte is sent after the address and determines which registers receive the data following the command byte.

A write to either output port groups of the SN7325 starts with the master transmitting the group's slave address with the R/$\overline{W}$ bit set low. The master can now transmit one or more bytes of data. The SN7325 acknowledges these subsequent bytes of data and updates the corresponding group's ports with each new byte until the master issues a STOP condition (Figure 5).

Reading Port Registers

To read the device data, the bus master must first send the SN7325 address with the R/$\overline{W}$ bit set to zero, followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the SN7325 address with the R/$\overline{W}$ bit set to 1. Data from the register defined by the command byte is then sent from the SN7325 to the master.

The SN7325 acknowledges the slave address, and samples the ports during the acknowledge bit. $\overline{INT}$ desserts during the slave address acknowledge. When the master reads one byte from the I/O ports of the SN7325 and subsequently issues a STOP condition (Figure 6), the SN7325 transmits the current port data, clears the change flags, and resets the transition detection. $\overline{INT}$ desserts during the slave acknowledge. The new snapshot data is the current port data transmitted to the master, and therefore, port changes occurring during the transmission are detected.

Port Output Signal-Level Translation

The open-drain output architecture allows for level translation to higher or lower voltages than the SN7325's supply. Each of the push-pull output ports has protection diodes to V+ and GND. When a port output is driven to a voltage higher than V+ or lower than GND, the appropriate protection diode clamps the output to a diode drop above V+ or below GND. When the SN7325 is powered down (V+ = 0V), every output port's protection diodes to V+ and GND continue to appear as a diode clamp from each output to GND (Figure 7). Each of the I/O ports OD0~OD7 has a protection diode to GND (Figure 8). When a port is driven to a voltage lower than GND, the protection diode clamps the port to a diode drop below GND. To obtain a high voltage , Open-Drain I/O Ports should connect an resistance to Vcc(Figure 8).

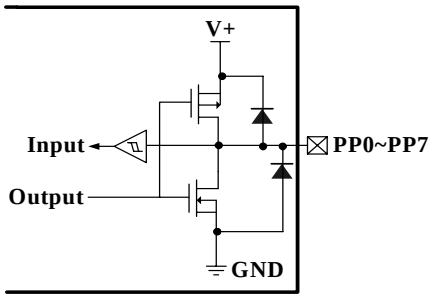


Figure 7.SN7325 Push-Pull I/O Ports Structure

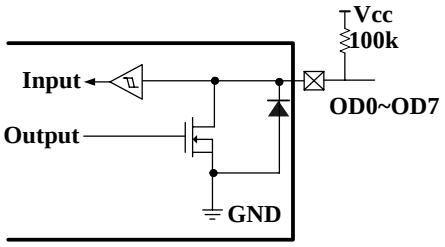
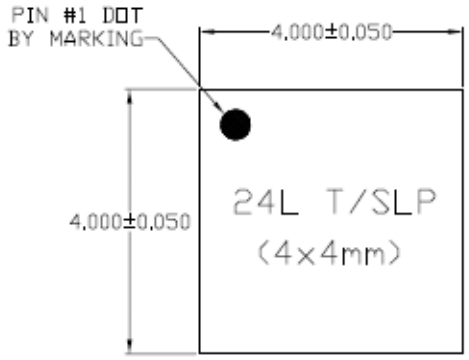


Figure 8.SN7325 Open-Drain I/O Ports Structure

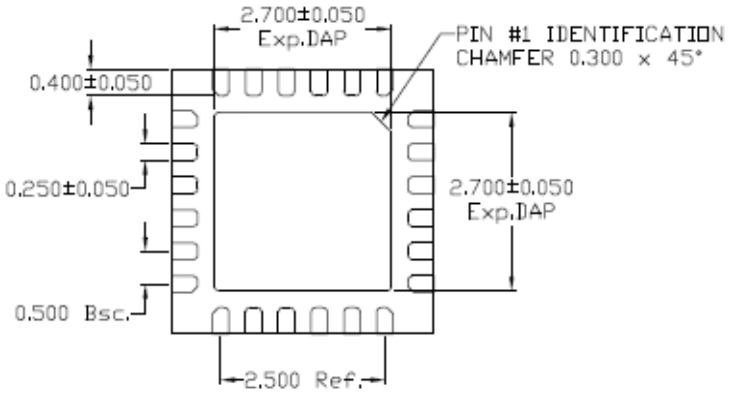
Package Information:

WQFN-24

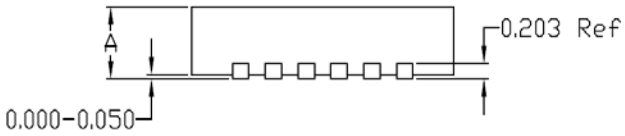
Top View



Bottom View



Side View



		TSLP
A	MAX	0.800
	NOM	0.750
	MIN	0.700