FAIRCHILD
SEMICONDUCTOR ™

December 2000

**QFET™**

FQD4N20L / FQU4N20L
200V LOGIC N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, and motor control.

Features

- 3.2A, 200V, $R_{DS(on)}$ = 1.35Ω @V_{GS} = 10 V
- Low gate charge (typical 4.0 nC)
- Low Crss (typical 6.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirement allowing direct operation from logic drivers

D-PAK
FQD Series

I-PAK
FQU Series
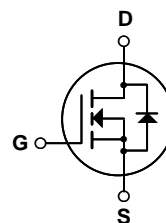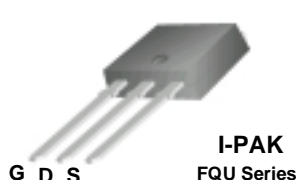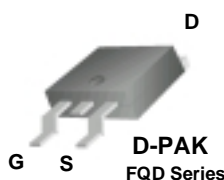
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FQD4N20L / FQU4N20L	Units
V_{DSS}	Drain-Source Voltage			200	V
I_D	Drain Current	- Continuous (T_C = 25°C)		3.2	A
		- Continuous (T_C = 100°C)		2.02	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	12.8	A
V_{GSS}	Gate-Source Voltage			± 20	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	52	mJ
I_{AR}	Avalanche Current		(Note 1)	3.2	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *			2.5	W
	Power Dissipation (T_C = 25°C)			30	W
	- Derate above 25°C			0.24	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	4.17	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

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Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.16	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 160$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 1.6$ A	--	1.10	1.35	Ω
		$V_{GS} = 5$ V, $I_D = 1.6$ A		1.13	1.40	
g_{FS}	Forward Transconductance	$V_{DS} = 25$ V, $I_D = 1.6$ A (Note 4)	--	3.0	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	240	310	pF
C_{oss}	Output Capacitance		--	36	45	pF
C_{rss}	Reverse Transfer Capacitance		--	6	8	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100$ V, $I_D = 3.8$ A, $R_G = 25$ Ω	--	7	25	ns
t_r	Turn-On Rise Time		--	70	150	ns
$t_{d(off)}$	Turn-Off Delay Time		--	15	40	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	40	90	ns
Q_g	Total Gate Charge	$V_{DS} = 160$ V, $I_D = 3.8$ A, $V_{GS} = 5$ V	--	4.0	5.2	nC
Q_{gs}	Gate-Source Charge		--	1.0	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	1.9	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.2	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12.8	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 3.2$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 3.8$ A,	--	90	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F / dt = 100$ A/μs (Note 4)	--	0.25	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 7.6mH, $I_{AS} = 3.2$A, $V_{DD} = 50$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 3.8$A, di/dt ≤ 300A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature
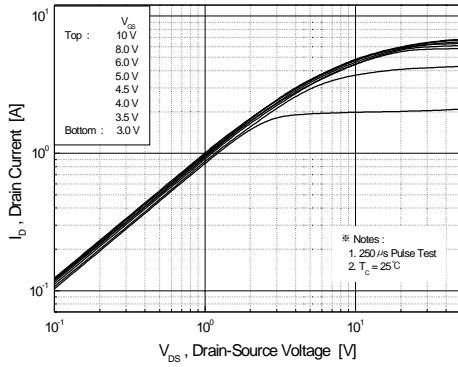
Typical Characteristics
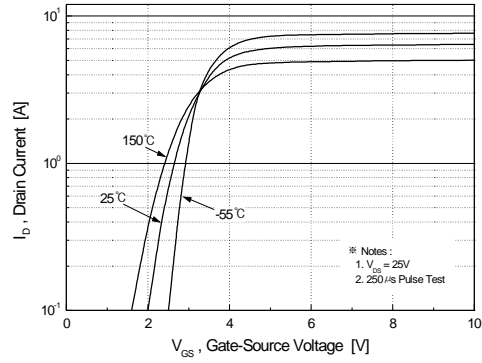

Figure 1. On-Region Characteristics

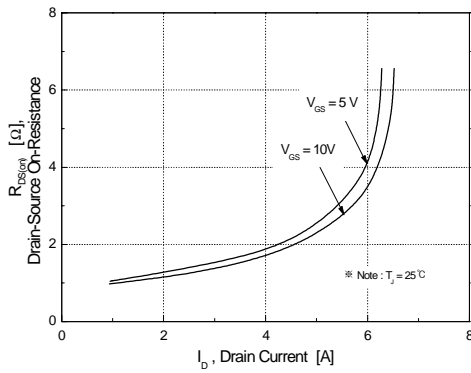**Figure 2. Transfer Characteristics**

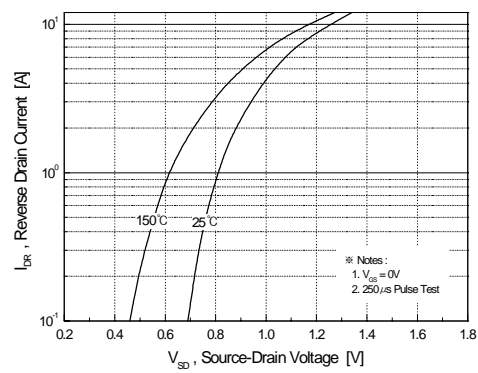**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

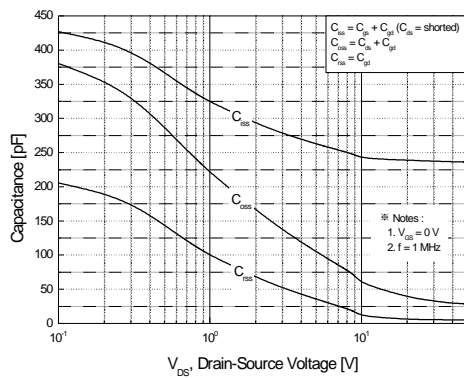**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**
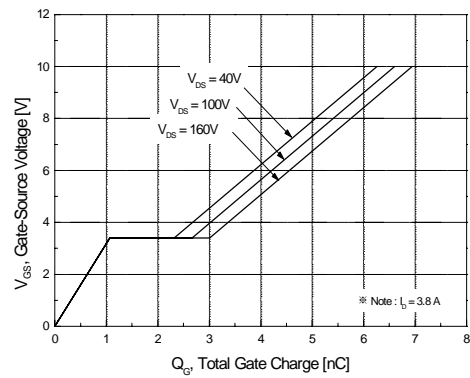

Figure 5. Capacitance Characteristics

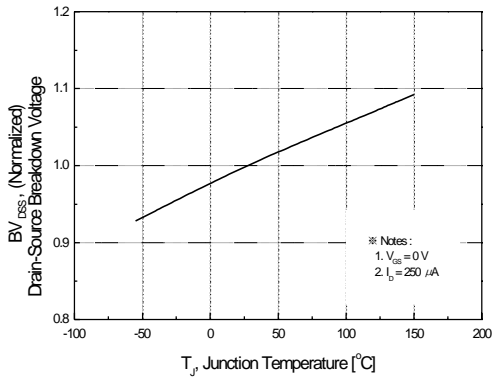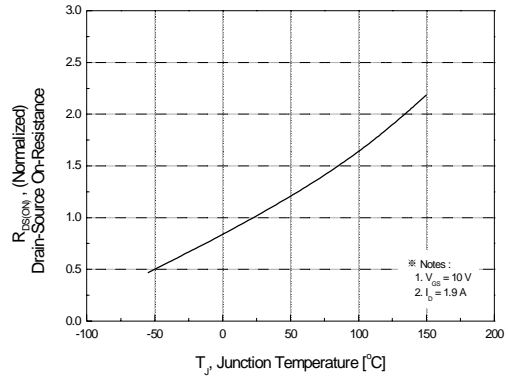**Figure 6. Gate Charge Characteristics**

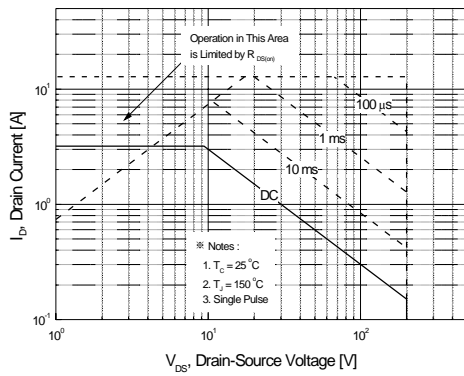©2000 Fairchild Semiconductor International

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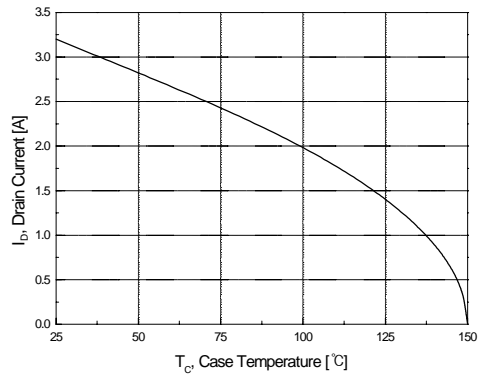# Typical Characteristics (Continued)

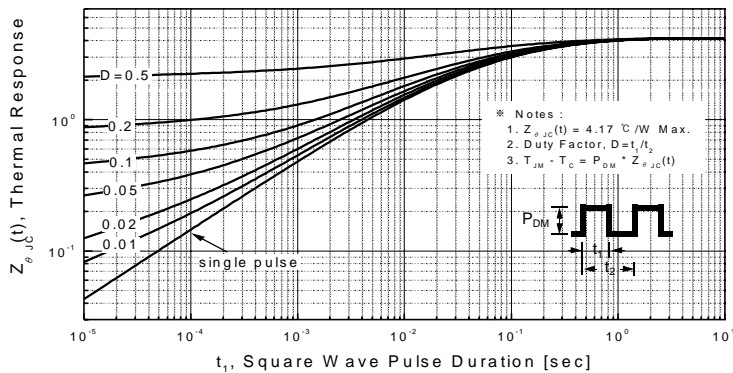**Figure 7. Breakdown Voltage Variation vs. Temperature**

Figure 8. On-Resistance Variation vs. Temperature

Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

Same Type as DUT

12V 200nF 50KΩ 300nF

V_{GS}

DUT

3mA

V_{DS}

V_{GS}

5V

Q_g

Q_{gs} Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

R_L

V_{DS}

V_{GS}

R_G

5V

DUT

V_{DD}

V_{DS}

90%

V_{GS}

10%

$t_{d(on)}$ t_r

t_{on}

$t_{d(off)}$ t_f

t_{off}
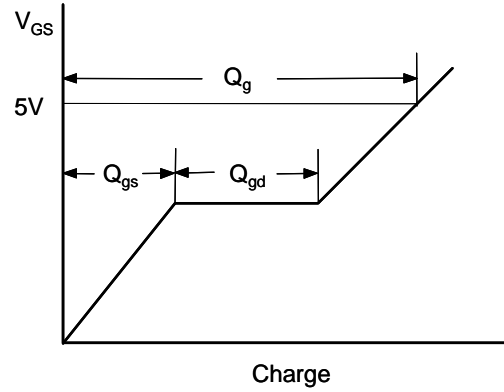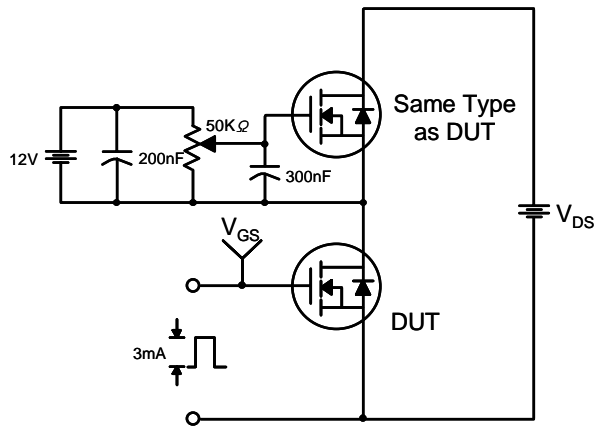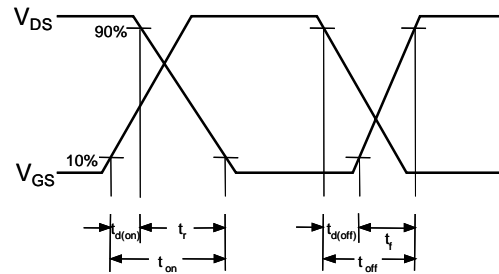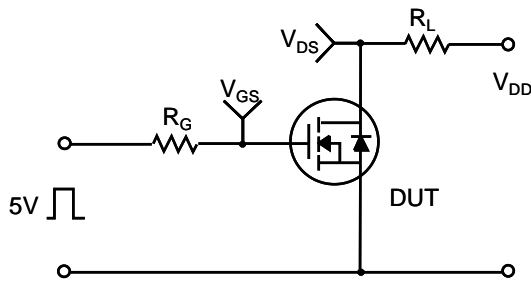
Unclamped Inductive Switching Test Circuit & Waveforms

L

V_{DS}

I_D

R_G

10V

t_p

DUT

V_{DD}

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD}

$V_{DS}(t)$

t_p

Time

Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

+

−

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

DPAK

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Package Dimensions (Continued)

IPAK

6.60 ±0.20

5.34 ±0.20

(0.50)   (4.34)   (0.50)

0.60 ±0.20

0.80 ±0.10

MAX0.96

0.76 ±0.10

0.70 ±0.20

6.10 ±0.20

1.80 ±0.20

9.30 ±0.30

2.30TYP
[2.30±0.20]

2.30TYP
[2.30±0.20]

2.30 ±0.20

0.50 ±0.10

16.10 ±0.30

0.50 ±0.10
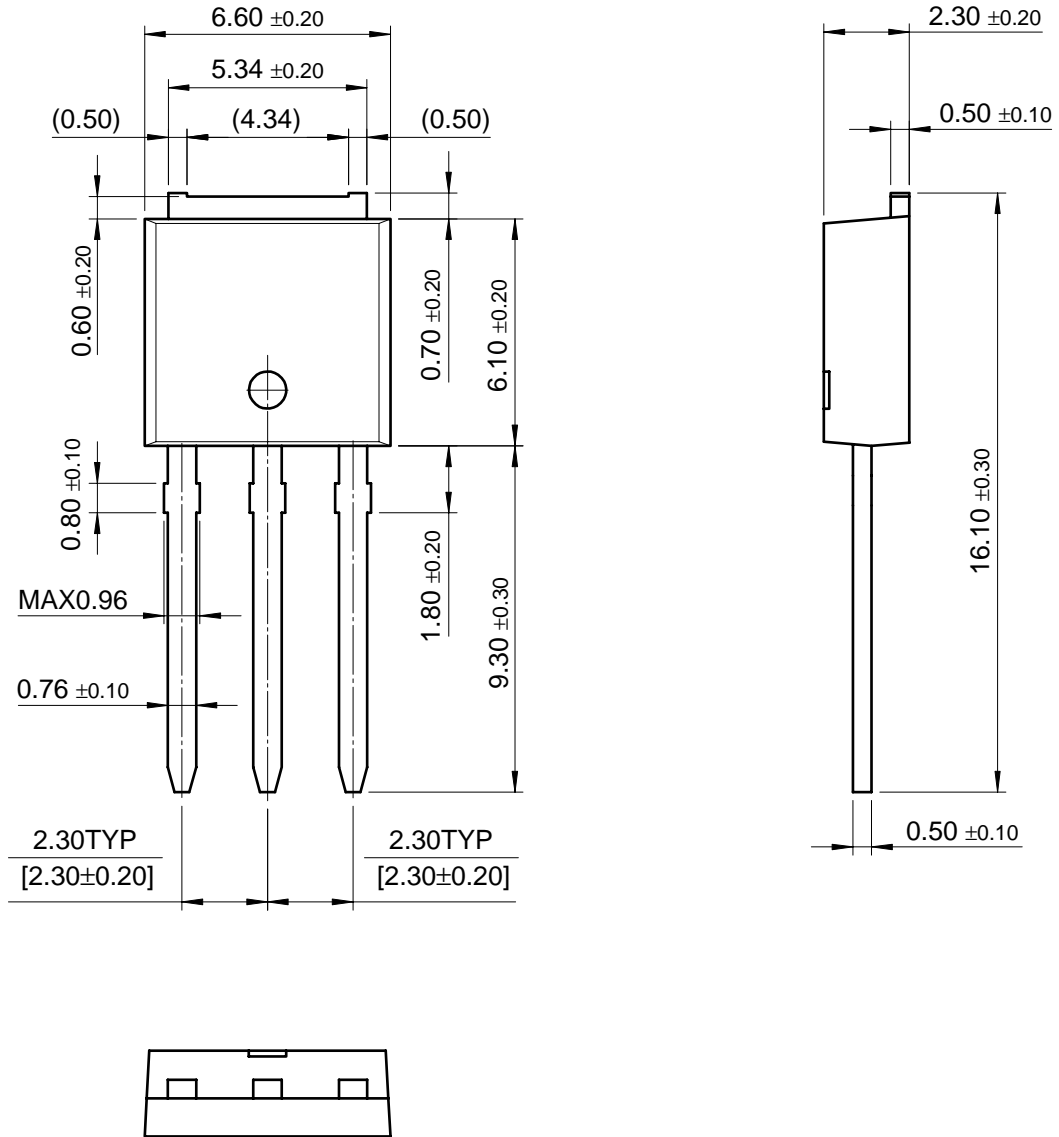
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E^{2}CMOS™	PowerTrench$^®$	VCX™
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FACT Quiet Series™	QS™	
FAST$^®$	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	

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