



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	Order Number / Package	
			TO-236AB*	Die
300V	25Ω	2.4V	TN2130K1	TN2130ND

Product marking for SOT-23: <div style="border: 1px solid black; padding: 2px; display: inline-block;">N1T*</div> where * = 2-week alpha date code
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\*Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>iss</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain

### Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

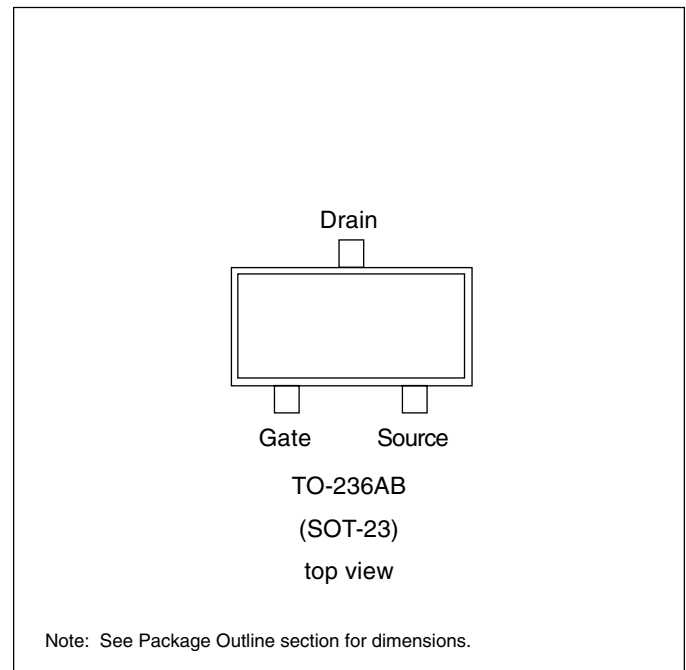
\* Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Option



11/12/01

Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: <http://www.supertex.com>. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-236AB	85mA	200mA	0.36W	200	350	85mA	200mA

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

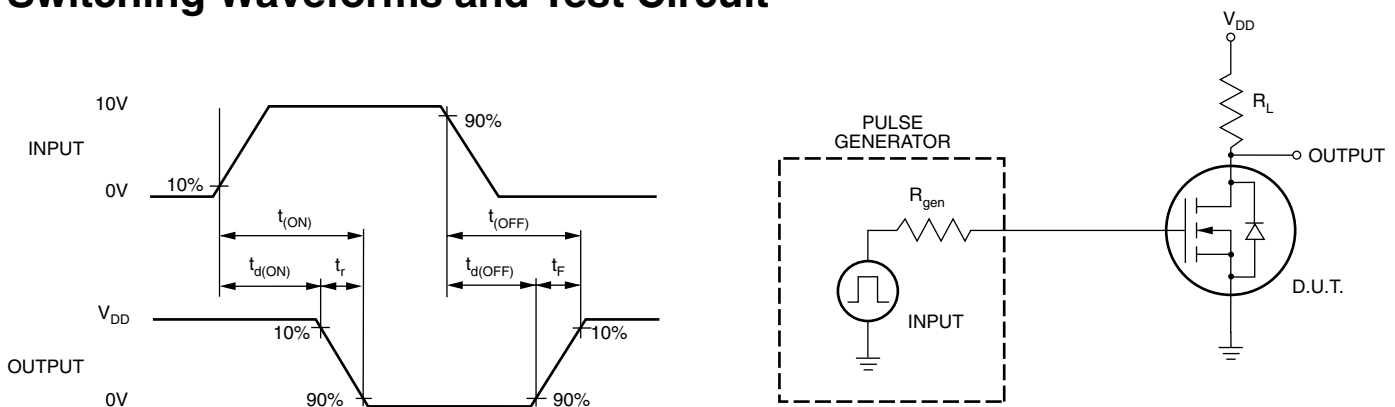
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	300			V	$I_D = 1\text{mA}$ , $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{GS} = V_{DS}$ , $I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.5	mV/ $^\circ\text{C}$	$I_D = 1\text{mA}$ , $V_{GS} = V_{DS}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current			10	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = \text{Max Rating}$
				100	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	250			mA	$V_{GS} = 10\text{V}$ , $V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			25	$\Omega$	$V_{GS} = 4.5\text{V}$ , $I_D = 120\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/ $^\circ\text{C}$	$V_{GS} = 4.5\text{V}$ , $I_D = 120\text{mA}$
$G_{FS}$	Forward Transconductance		250		m $\Omega$	$V_{DS} = 25\text{V}$ , $I_D = 100\text{mA}$
$C_{ISS}$	Input Capacitance			50	pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance			15		
$C_{RSS}$	Reverse Transfer Capacitance			5		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25\text{V}$ , $I_D = 120\text{mA}$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			7		
$t_{d(OFF)}$	Turn-OFF Delay Time			12		
$t_f$	Fall Time			15		
$V_{SD}$	Diode Forward Voltage Drop			1.8	V	$I_{SD} = 120\text{mA}$ , $V_{GS} = 0\text{V}$
$t_{rr}$	Reverse Recovery Time		400		ns	$I_{SD} = 120\text{mA}$ , $V_{GS} = 0\text{V}$

### Notes:

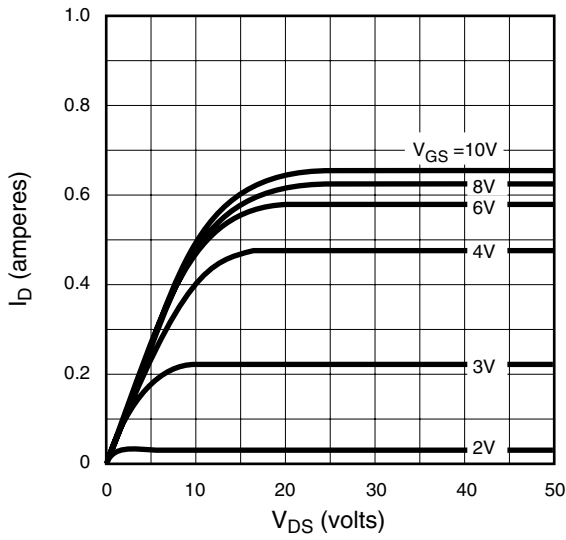
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

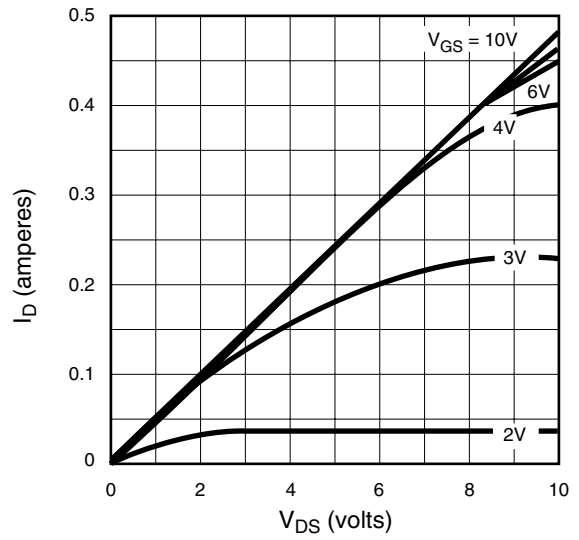


# Typical Performance Curves

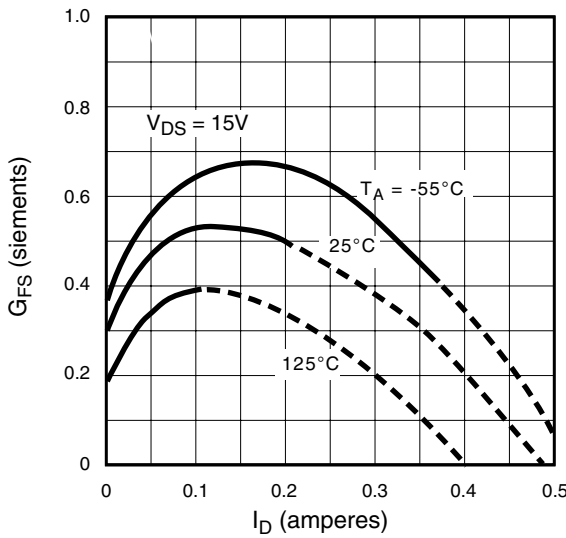
Output Characteristics



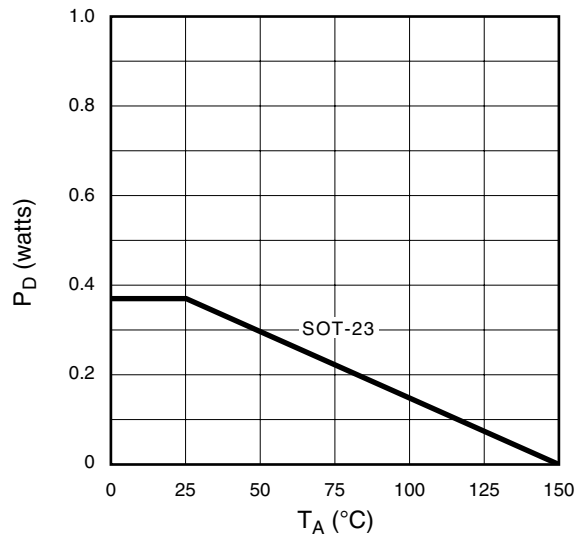
Saturation Characteristics



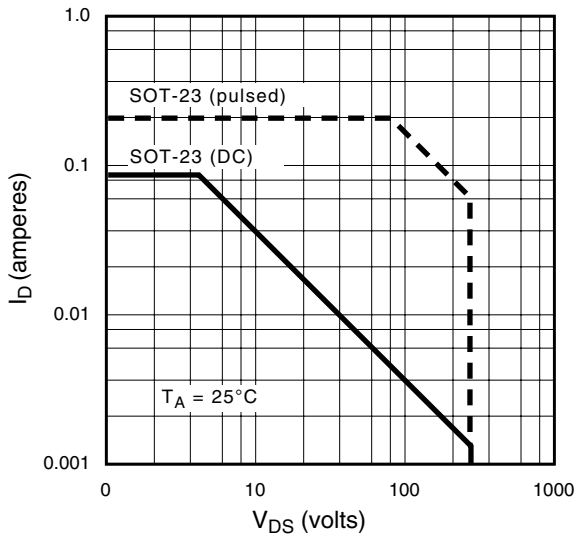
Transconductance vs. Drain Current



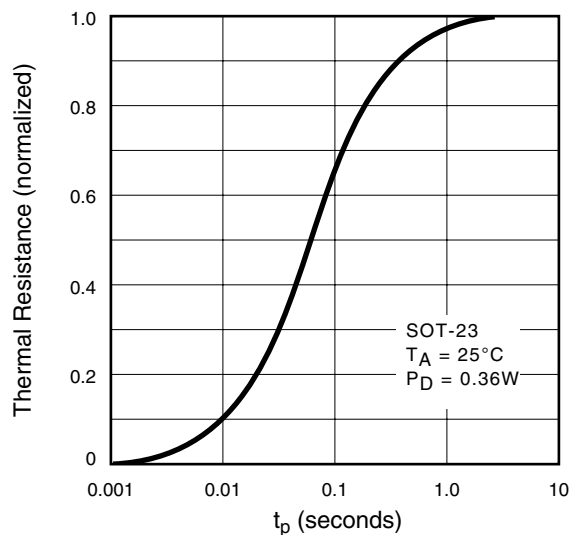
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



# Typical Performance Curves

