



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	Order Number / Package		
			TO-236AB*	TO-92	Die
60V	2.5Ω	2.0V	TN2106K1	TN2106N3	TN2106ND

Product marking for SOT-23: N1L* where * = 2-week alpha date code
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\*Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>iss</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

### Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

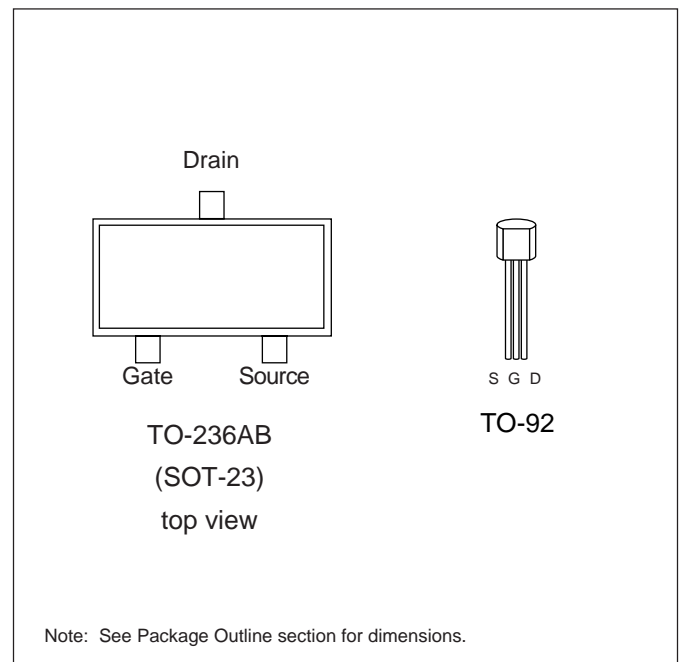
\* Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



# Thermal Characteristics

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation @ T <sub>A</sub> = 25°C	θ <sub>jc</sub> °C/W	θ <sub>ja</sub> °C/W	I <sub>DR</sub> *	I <sub>DRM</sub>
TO-236AB	0.28A	0.8A	0.36W	200	350	0.28A	0.8A
TO-92	0.30A	1.0A	0.74W	125	170	0.30A	1.0A

\* I<sub>D</sub> (continuous) is limited by max rated T<sub>j</sub>.

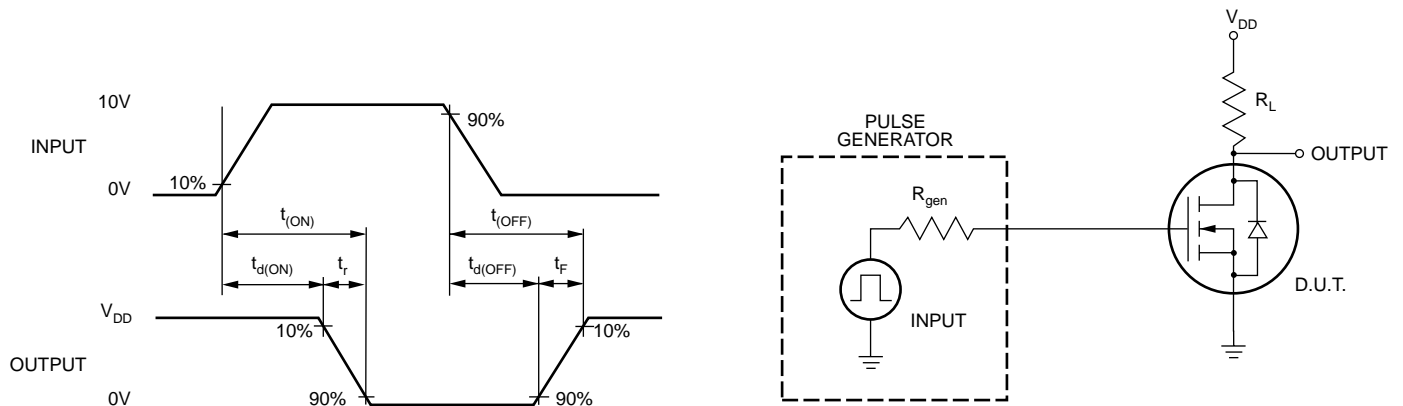
# Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60			V	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0V
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.6		2.0	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with Temperature		-3.8	-5.5	mV/°C	I <sub>D</sub> = 1mA, V <sub>GS</sub> = V <sub>DS</sub>
I <sub>GSS</sub>	Gate Body Leakage		0.1	100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			1	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Max Rating
				100	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0.8 Max Rating T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	ON-State Drain Current	0.6			A	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance			5.0	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 200mA
				2.5	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 500mA
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with Temperature		0.70	1.0	%/°C	V <sub>GS</sub> = 10V, I <sub>D</sub> = 500mA
G <sub>FS</sub>	Forward Transconductance	150	400		mS	V <sub>DS</sub> = 25V, I <sub>D</sub> = 500mA
C <sub>ISS</sub>	Input Capacitance		35	50	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz
C <sub>OSS</sub>	Common Source Output Capacitance		17	25		
C <sub>RSS</sub>	Reverse Transfer Capacitance		7	8		
t <sub>d(ON)</sub>	Turn-ON Delay Time		3	5	ns	V <sub>DD</sub> = 25V I <sub>D</sub> = 0.5A R <sub>GEN</sub> = 25Ω
t <sub>r</sub>	Rise Time		5	8		
t <sub>d(OFF)</sub>	Turn-OFF Delay Time		6	9		
t <sub>f</sub>	Fall Time		5	8		
V <sub>SD</sub>	Diode Forward Voltage Drop		1.2	1.8	V	I <sub>SD</sub> = 0.5A, V <sub>GS</sub> = 0V
t <sub>rr</sub>	Reverse Recovery Time		400		ns	I <sub>SD</sub> = 0.5A, V <sub>GS</sub> = 0V

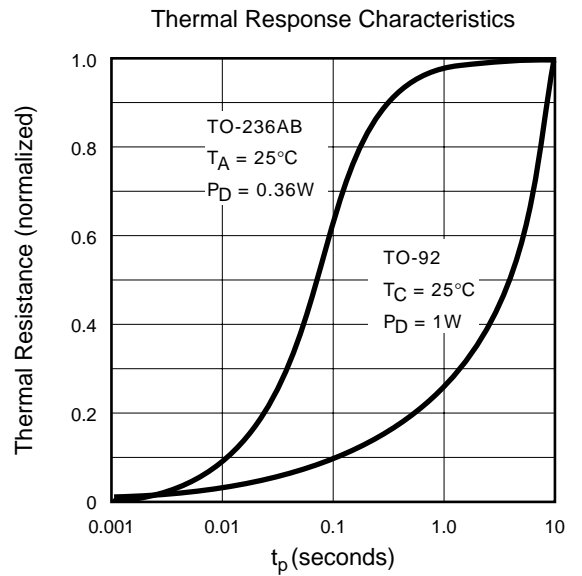
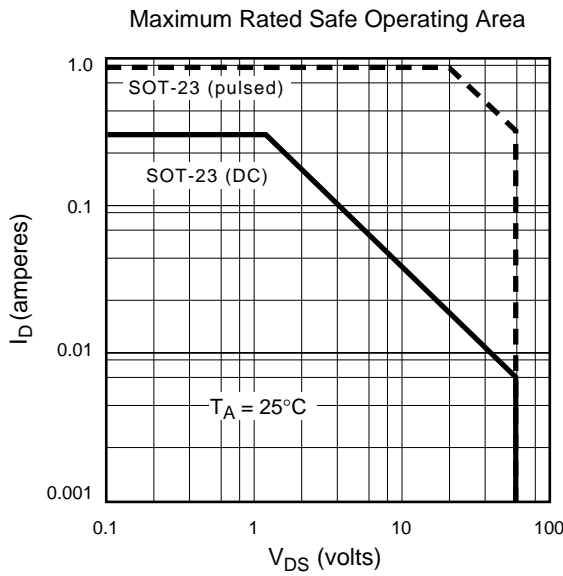
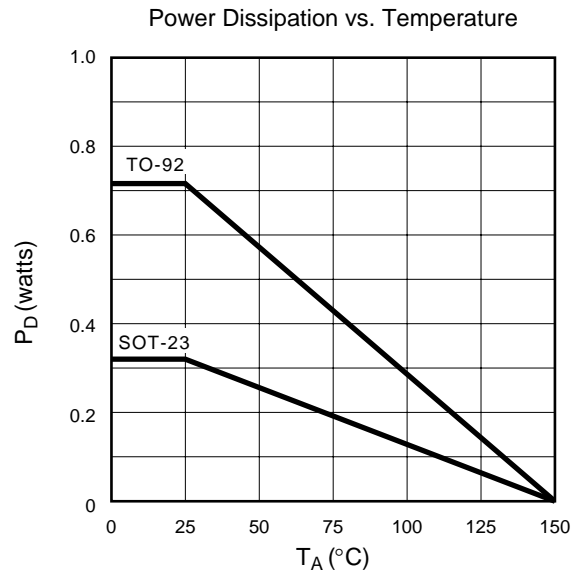
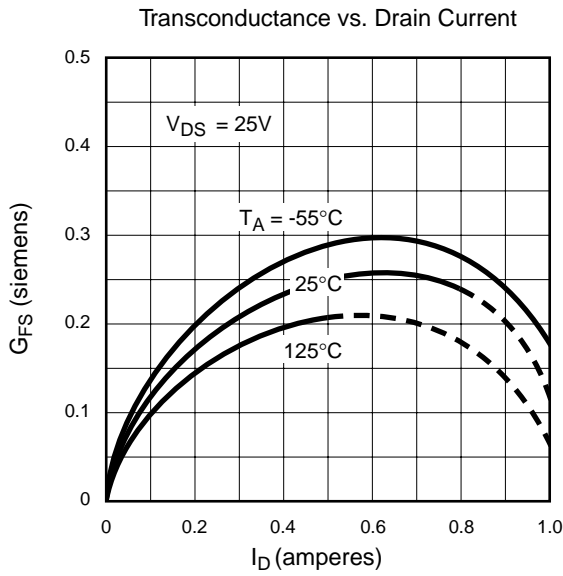
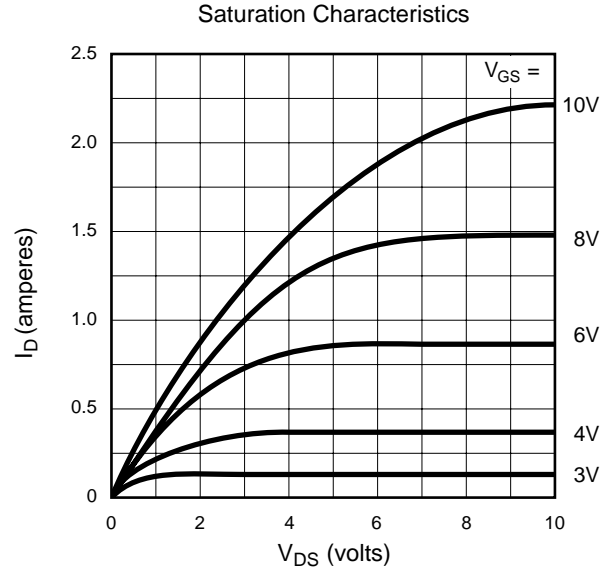
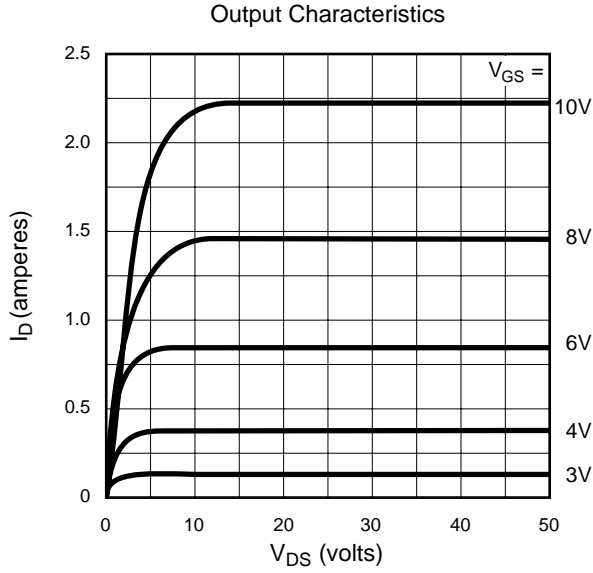
**Notes:**

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

# Switching Waveforms and Test Circuit

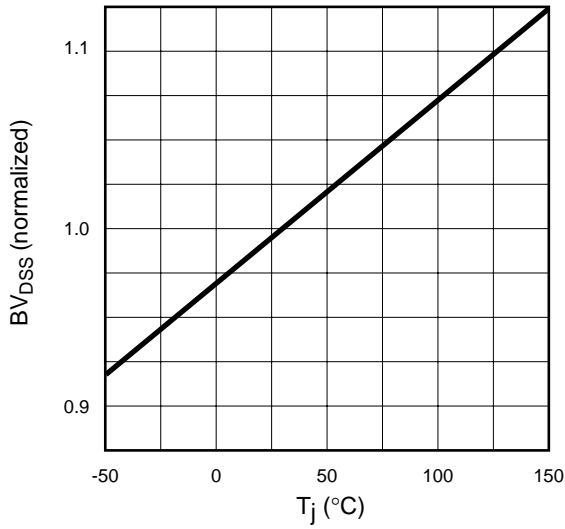


# Typical Performance Curves

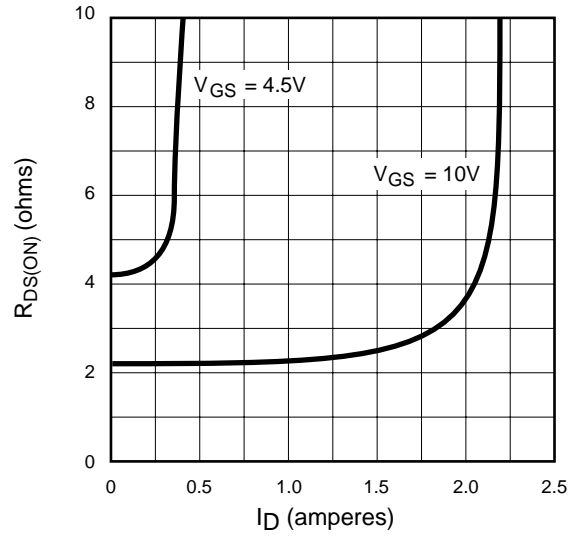


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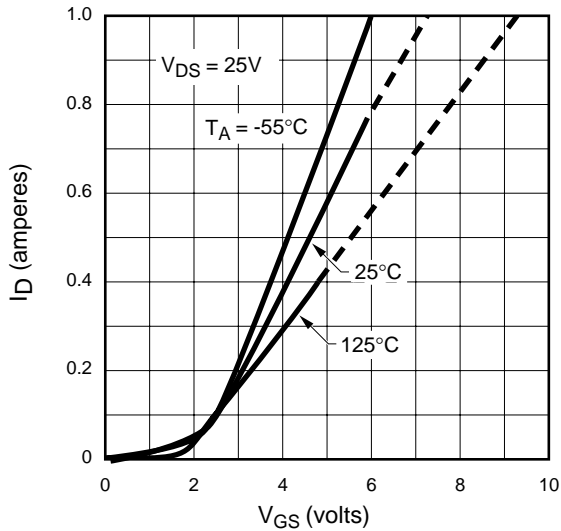
BV<sub>DSS</sub> Variation with Temperature



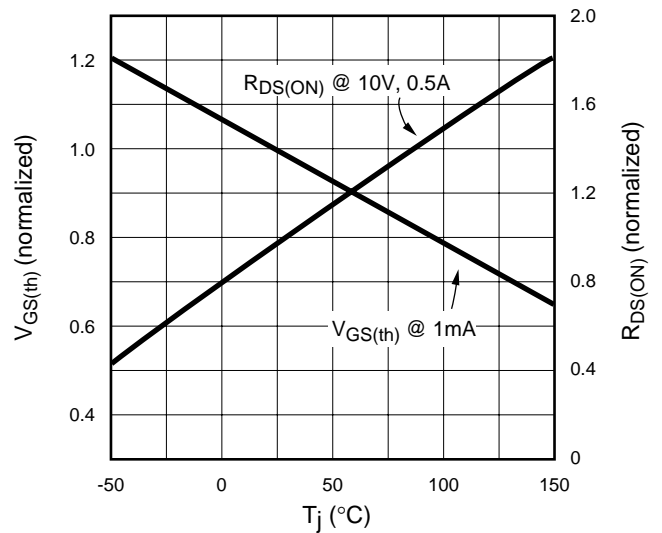
On-Resistance vs. Drain Current



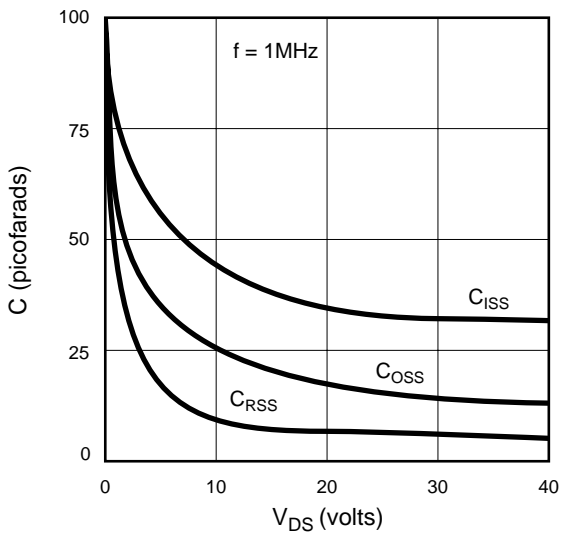
Transfer Characteristics



V<sub>GS(th)</sub> and R<sub>DS(ON)</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

