

## N-Channel Enhancement-Mode Vertical DMOS FETs

#### **Ordering Information**

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub> (max)	Order Number / Package				
BV <sub>DGS</sub>		TO-92	TO-236AB*	Die <sup>†</sup>		
60V	$4.0\Omega$	VN2106N3	_	_		
100V	4.0Ω	_	VN2110K1	VN2110ND		

<sup>&</sup>lt;sup>†</sup>MIL visual screening available

# Product marking for SOT-23: N1A\* where \* = 2-week alpha date code

#### **Features**

- ☐ Commercial and Military versions available
- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- ☐ High input impedance and high gain

#### **Applications**

- Motor controls
- → Amplifiers
- Power supply circuits
- Converters
- Switches
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

## **Absolute Maximum Ratings**

$BV_{DSS}$
$BV_{DGS}$
± 20V
-55°C to +150°C
300°C

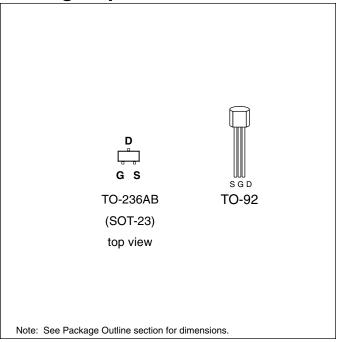
<sup>\*</sup> Distance of 1.6 mm from case for 10 seconds.

## **Advanced DMOS Technology**

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

#### **Package Options**



<sup>\*</sup>Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

#### **Thermal Characteristics**

Package	I <sub>D</sub> (continuous) <sup>†</sup>	I <sub>D</sub> (pulsed)	Power Dissipation*	$\theta_{\sf jc}$	$ heta_{\sf ja}$	I <sub>DR</sub> †	I <sub>DRM</sub>
			@ T <sub>C</sub> = 25°C	°C/W	°C/W		
TO-92	0.3A	1.0A	1.0W	125	170	0.3A	1.0A
TO-236AB	0.2A	0.8A	$0.36W (T_A = 25^{\circ}C)$	200	350	0.2A	0.8A

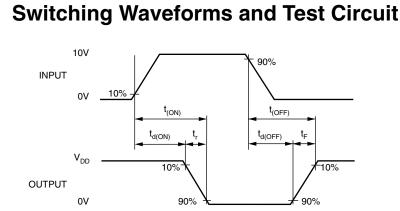
 $<sup>{}^{\</sup>dagger}I_{_{D}}$  (continuous) is limited by max rated  $T_{_{i}}$ .

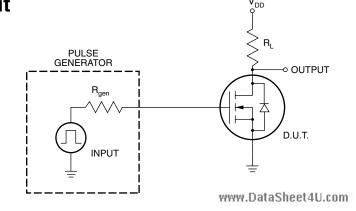
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Тур	Max	Unit	Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	VN2110 VN2106	100 60			V	$I_D = 1$ mA, $V_{GS} = 0$ V	
V <sub>GS(th)</sub>	Gate Threshold Voltage		0.8		2.4	٧	$V_{GS} = V_{DS}$ , $I_D = 1mA$	
$\Delta V_{GS(th)}$	Change in V <sub>GS(th)</sub> with Tempe		-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}$ , $I_D = 1mA$		
I <sub>GSS</sub>	Gate Body Leakage		0.1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$		
ww.DossSheet4U	Sheet4U. Zero Gate Voltage Drain Current				1	μΑ	$V_{GS} = 0V$ , $V_{DS} = Max$ Rating	
					100	μΑ	$V_{GS} = 0V$ , $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I <sub>D(ON)</sub>	ON-State Drain Current	0.6			А	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V		
R <sub>DS(ON)</sub>	Static Drain-to-Source			4.5	6.0	Ω	$V_{GS} = 5V$ , $I_D = 75mA$	
	ON-State Resistance		3.0	4.0	Ω	$V_{GS} = 10V, I_D = 500mA$		
$\Delta R_{DS(ON)}$	Change in R <sub>DS(ON)</sub> with Temp		0.70	1.0	%/°C	$V_{GS} = 10V, I_D = 500mA$		
G <sub>FS</sub>	Forward Transconductance	150	400		mប៊	$V_{DS} = 25V, I_{D} = 0.5A$		
C <sub>ISS</sub>	Input Capacitance  Common Source Output Capacitance			35	50	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz	
C <sub>OSS</sub>				13	25			
C <sub>RSS</sub>	Reverse Transfer Capacitano	e		4	5			
t <sub>d(ON)</sub>	Turn-ON Delay Time Rise Time Turn-OFF Delay Time			3	5	ns	$V_{DD} = 25V$ $I_{D} = 0.6A$ $R_{GEN} = 25\Omega$	
t <sub>r</sub>				5	8			
t <sub>d(OFF)</sub>				6	9			
t <sub>f</sub>	Fall Time			5	8			
V <sub>SD</sub>	Diode Forward Voltage Drop			1.2	1.8	V	$I_{SD} = 0.6A, V_{GS} = 0V$	
t <sub>rr</sub>	Reverse Recovery Time			400		ns	$I_{SD} = 0.6A, V_{GS} = 0V$	

#### Notes

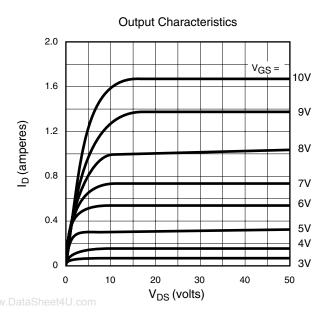
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test:  $300\mu s$  pulse, 2% duty cycle.)
- ${\it 2.} \quad {\it All A.C. parameters sample tested.}$

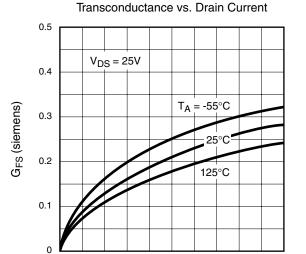




<sup>\*</sup> Total for package.

# **Typical Performance Curves**





0.4

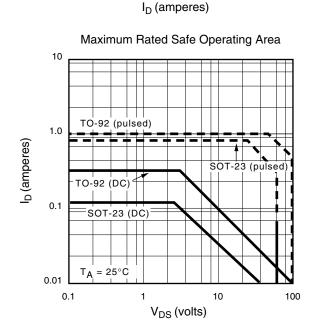
0.6

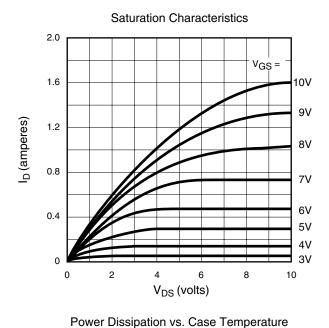
0.8

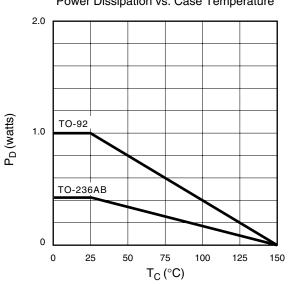
1.0

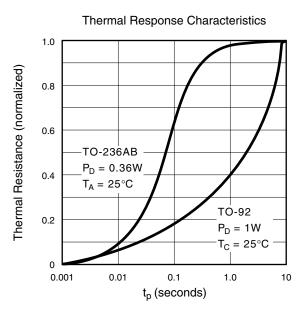
0.2

0

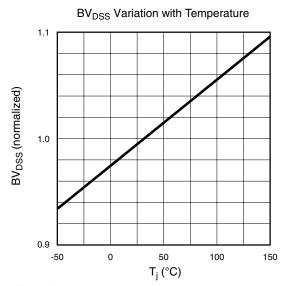








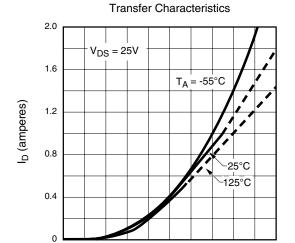
# **Typical Performance Curves**



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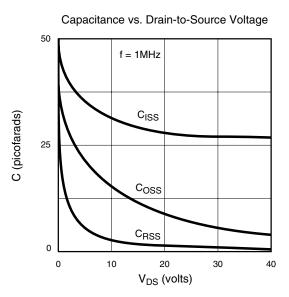
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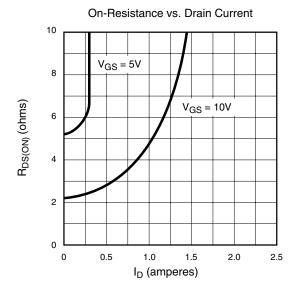
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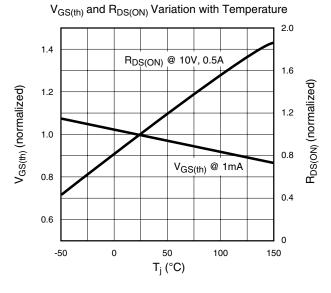


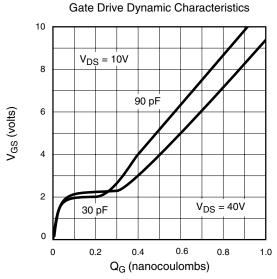
V<sub>GS</sub> (volts)

10









11/12/01